Name: Khoi Nguyen

Class: ECE 5780

Post lab 2

1. Why can't you use both pins PA0 and PC0 for external interrupts at the same time?
   a. As each EXTI line can only be connected to one GPIO pin at a time, multiple EXTI lines cannot be connected to a single GPIO pin.
   b. We can't use both pins PA0 and PC0 for external interrupts at the same time because they would both map to EXTI line 0.
   c. Since each EXTI line only allows for one selection, choosing PA0 for EXTI0 means PC0 for EXTI0 cannot be chosen simultaneously.
2. What software priority level gives the highest priority? What level gives the lowest?
   a. The highest priority is given by the level 0 and the lowest priority is given by the level 3.
3. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?
   a. Each IPR register contains four 8-bit regions
   b. Only the upper two bits from these regions are implemented, giving four possible configurable priority levels (0-3)
4. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.
   a. The latency between pushing the Discovery board button and the LED change is roughly 2.5ms
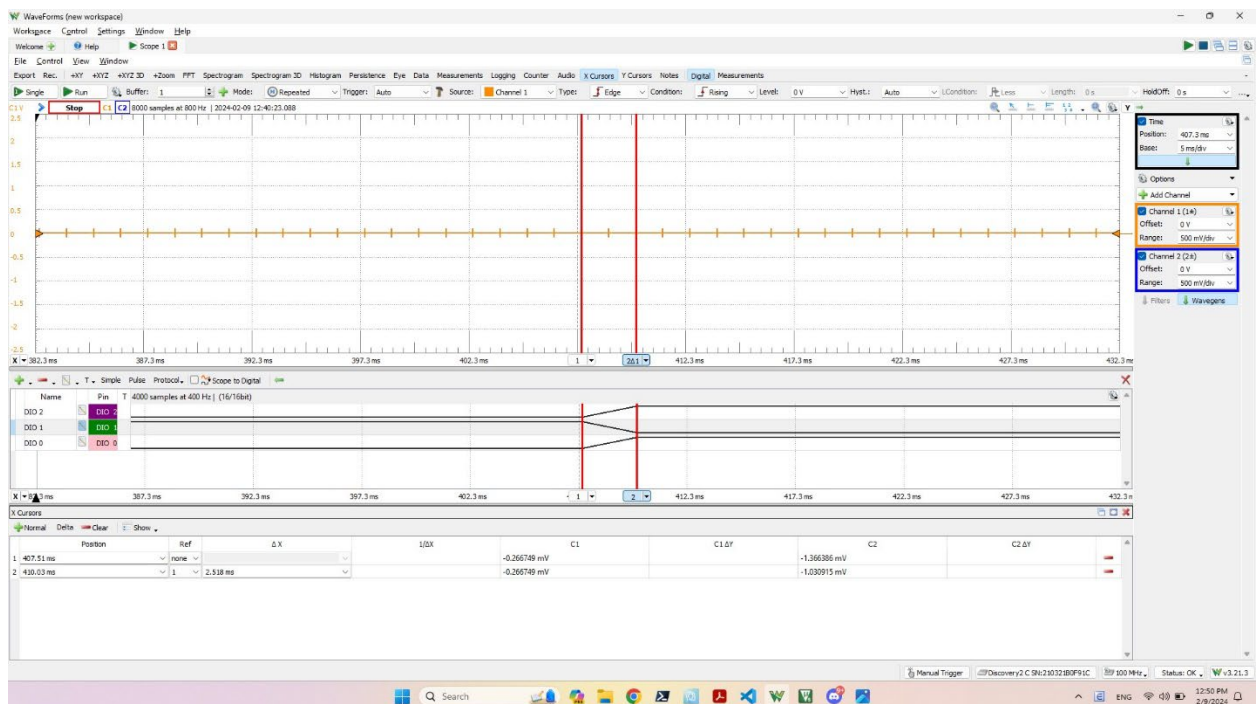
5. Why do you need to clear status flag bits in peripherals when servicing their interrupts?
    a. Clearing the status flag bits of peripherals when servicing their interrupts is necessary to acknowledge the handling of the interrupt.
    b. If the status flag is not cleared, the interrupt will remain active and cause the ISR to be repeatedly called, which may lead to a continuous loop, preventing the execution of the main program.

Github repo link for this lab2: https://github.com/kenzend94/ECE_5780/tree/main/Lab2