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Class: ECE 5780

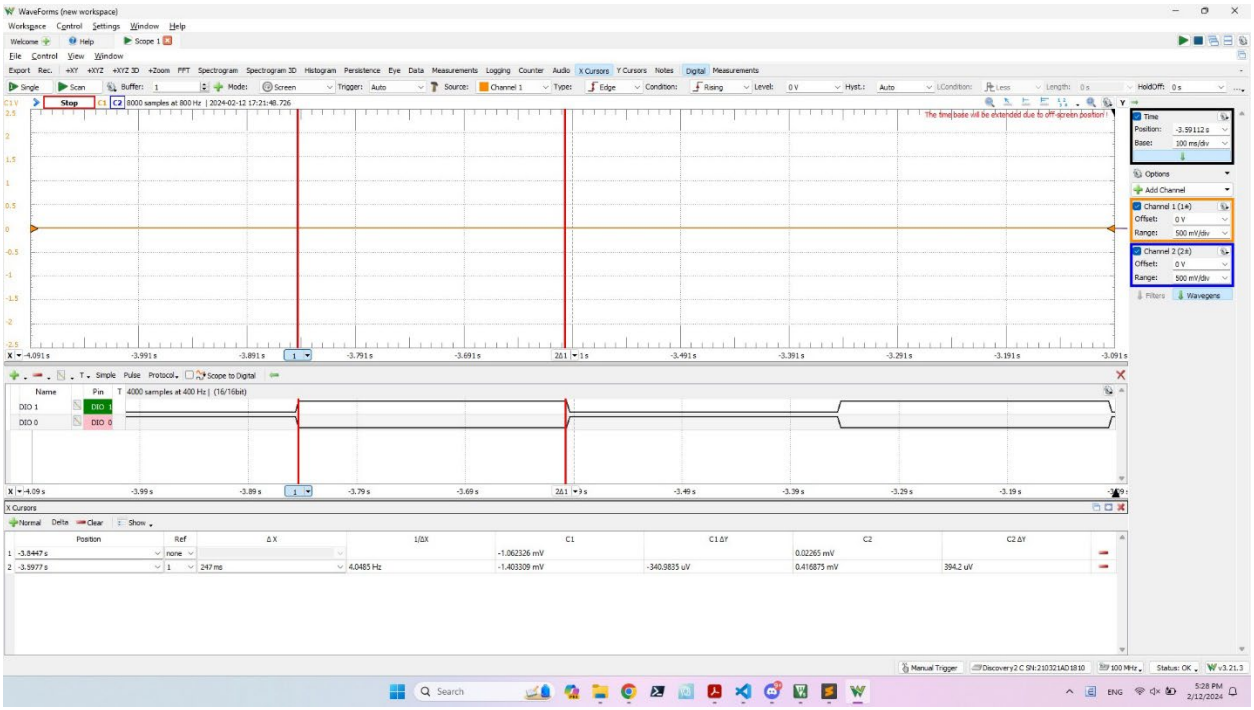
Post lab 3

Github repo: https://github.com/kenzend94/ECE_5780

1. Using a timer clock source of 8 MHz, calculate PSC and ARR values to get a 60 Hz interrupt.
   a. $PSC = \frac{f_{CLK}}{ARR * f_{TARGET}} - 1 = 79$
   b. $ARR = \frac{f_{CLK}}{(PSC+1) * f_{TARGET}} = \frac{8MHz}{(79+1) * 60Hz} \approx 1666.67 \approx 1667$
2. Look through the Table 13 "STM32F072x8/xB pin definitions" in the chip datasheet and list all pins that can have the timer 3 capture/compare channel 1 alternate function.
   a. • If the pin is included on the LQFP64 package that we are using, list the alternate function number that you would use to select it.

Pin number (LQFP64)	Pin name (function upon reset)
56	PB4
37	PC6
22	PA6
-	PE3

3. List your measured value of the timer UEV interrupt period from first experiment.



a. The measured value of the timer UEV interrupt period is 247ms

b. $PSC = \frac{f_{CLK}}{ARR * f_{TARGET}} - 1 = 8000 - 1 = 7999$

c. $ARR = \frac{f_{CLK}}{(PSC+1) * f_{TARGET}} = \frac{8MHz}{8000 * 4Hz} = 250$

d. So I measured 247ms is roughly 4Hz

4. Describe what happened to the measured duty-cycle as the CCRx value increased in PWM mode 1.

   a. $Duty\ cycle = \frac{CCRx}{ARR} * 100\%$

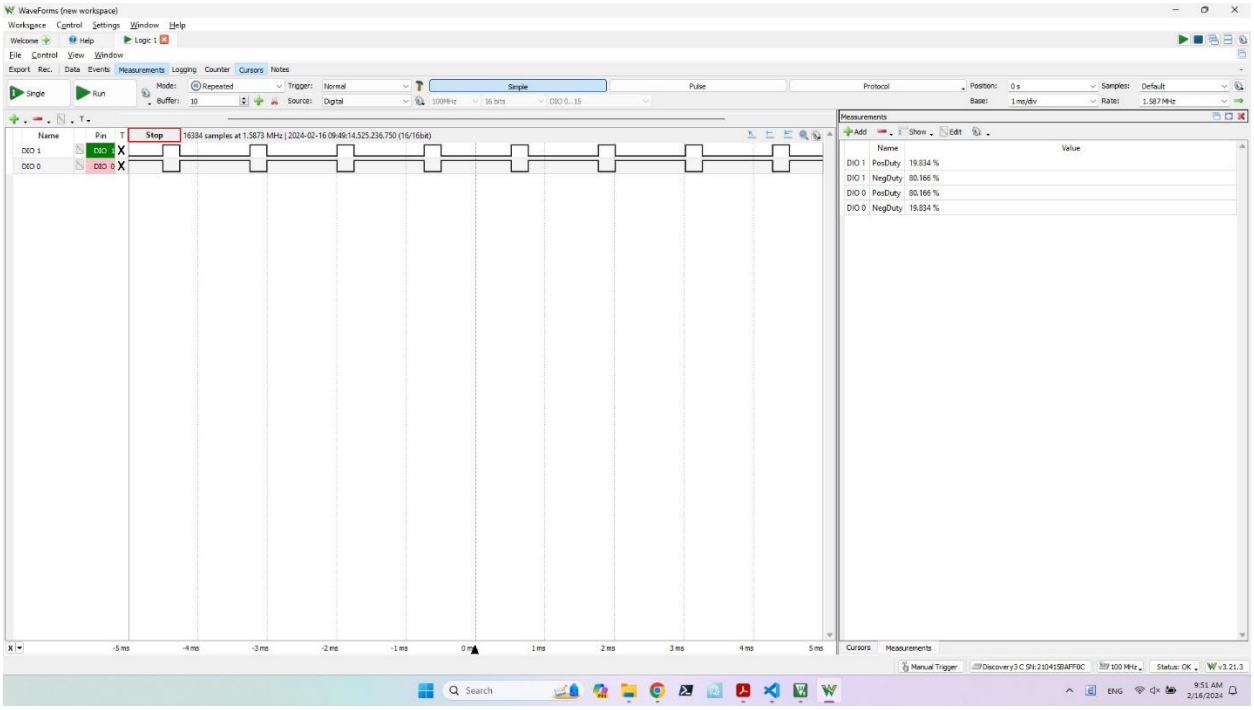
   b. If CCRx value increase then the duty cycle is gonna increase also.

5. Describe what happened to the measured duty-cycle as the CCRx value increased in PWM mode 2.

   a. $Duty\ cycle = \left(1 - \frac{CCRx}{ARR}\right) * 100$

   b. If CCRx value increase then the duty cycle is gonna decrease.

6. Include at least one logic analyzer screenshot of a PWM capture.



   a. As you can see in the right of the screenshot, the positive duty is roughly 20% and negative duty is roughly 80% as opposite.

7. What PWM mode is shown in figure 3.6 of the lab manual (PWM mode 1 or 2)?

   a. Based on the datasheet,

      i. 110: PWM mode 1 - In upcounting, channel 1 is active as long as TIMx_CNT<TIMx_CCR1 else inactive. In downcounting, channel 1 is inactive (OC1REF='0') as long as TIMx_CNT>TIMx_CCR1 else active (OC1REF='1').

ii. 111: PWM mode 2 - In upcounting, channel 1 is inactive as long as TIMx_CNT<TIMx_CCR1 else active. In downcounting, channel 1 is active as long as TIMx_CNT>TIMx_CCR1 else inactive.

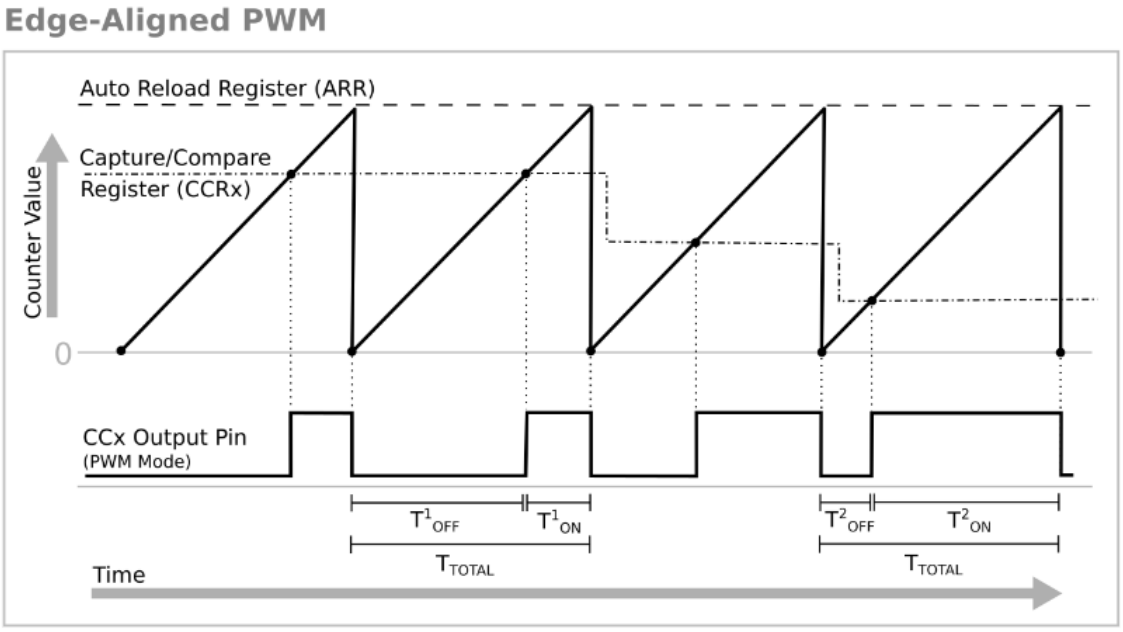


Figure 3.6: Edge-aligned PWM mode and output pin state.

b. We can see that Output is low when counter value < CCRx, and high when counter value > CCRx. So based on that, it should be PWM mode 2.