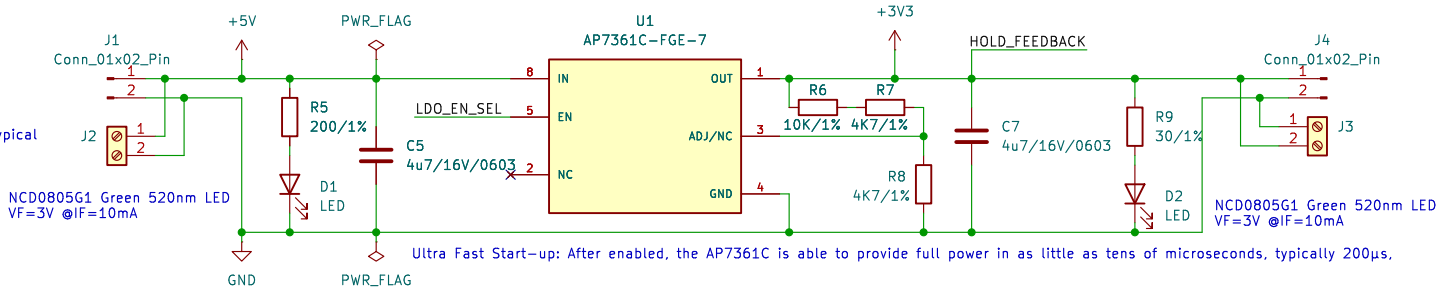
POWER SUPPLY (LDO)

AP7361C-FGE-7 -- Features
- Wide Input Voltage Range: 2.2V to 6.0V
- Fixed Output Voltage: 3.3V
- Output Voltage Accuracy: ±1%
- Very Low Dropout Voltage (3.3V): 360mV at 1A Typical
- Low Quiescent Current (IQ): 60µA Typical



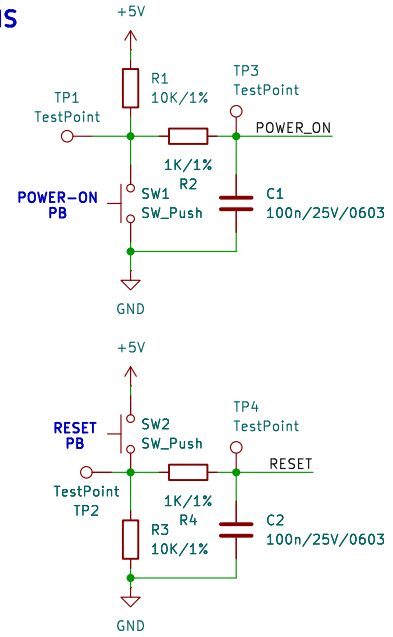
PROJECT DESCRIPTION:

This project features a power supply circuit centered on the AP7361C LDO regulator. It converts a 2.2V to 6.0V input into a stable 3.3V output with ±1% accuracy.

To manage power, SW1 (POWER ON) and SW2 (RESET) pulses are debounced by a 74LVC2G14 inverter. A 74AHCT32 OR gate creates a latch, while a 74HCT08 AND gate acts as a kill switch to maintain Enable signal only if the latch is active and RESET is not pressed.

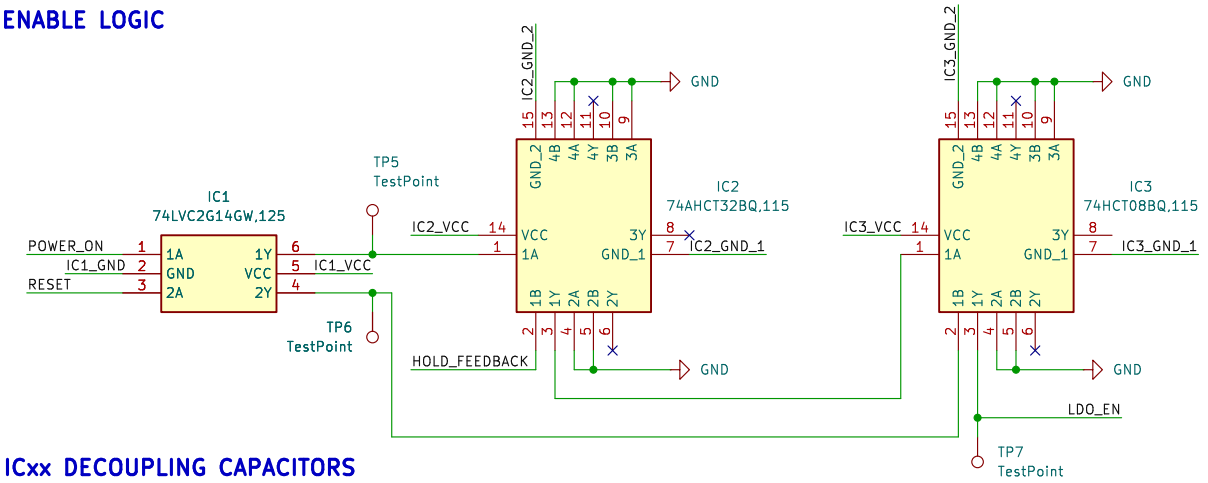
2 green LEDs (D1, D2) provide visual feedback status for the +5V and +3V3 rails.

PUSH-BUTTONS

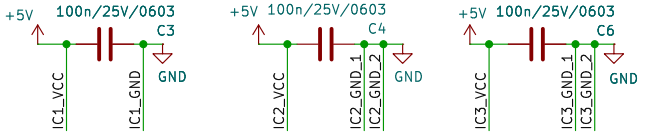


© How to debounce a button (Hardware approach)
© Digital Electronics: Debouncing a Push Button Switch (SPST)

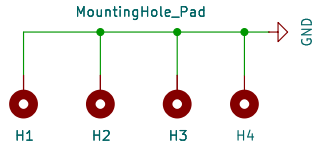
ENABLE LOGIC



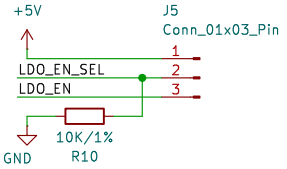
ICxx DECOUPLING CAPACITORS



MECHANICAL



ENABLE SELECTOR (JUMPER)



Author: Kepa ODRIOZOLA

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Size: A4	Date: 2026-01-25	**Rev: 1.0**
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