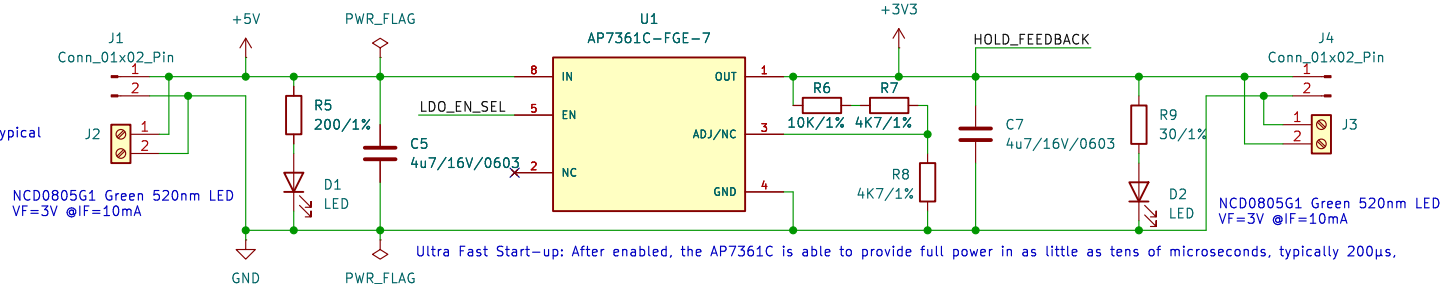


AP7361C—FGE-7 -- Features

- Wide Input Voltage Range: 2.2V to 6.0V
- Fixed Output Voltage: 3.3V
- Output Voltage Accuracy: $\pm 1\%$
- Very Low Dropout Voltage (3.3V): 360mV at 1A Typical
- Low Quiescent Current (I_Q): 60 μ A Typical



This project features a power supply circuit centered on the AP7361C LDO regulator. It converts a 2.2V to 6.0V input into a stable 3.3V output with $\pm 1\%$ accuracy.

2 green LEDs (D1, D2) provide visual feedback status for the +5V and +3V3 rails.

The image contains two circuit diagrams for the ATmega328P microcontroller.

Top Diagram: Power-On Reset (POR) Circuit

- Power Source:** +5V
- Test Points:** TP1 (TestPoint), TP3 (TestPoint)
- Components:**
 - R1: 10K/1% (Pull-up resistor)
 - R2: 1K/1% (Push-button resistor)
 - C1: 100n/25V/0603 (Capacitor)
 - SW1: SW_Push (Push-button)
- Connections:**
 - +5V is connected to R1.
 - R1 is connected to TP1 and the node between R2 and C1.
 - R2 is connected to TP3 and the node between R1 and C1.
 - C1 is connected to the node between R2 and R1, and to GND.
 - SW1 is connected to the node between R2 and C1, and to GND.
 - The node between R2 and C1 is connected to POWER_ON.
 - GND is connected to the bottom of C1 and SW1.

Bottom Diagram: Reset Push Button (PB) Circuit

- Power Source:** +5V
- Test Points:** TP2 (TestPoint), TP4 (TestPoint)
- Components:**
 - R3: 10K/1% (Pull-up resistor)
 - R4: 1K/1% (Push-button resistor)
 - C2: 100n/25V/0603 (Capacitor)
 - SW2: SW_Push (Push-button)
- Connections:**
 - +5V is connected to R3.
 - R3 is connected to TP2 and the node between R4 and C2.
 - R4 is connected to TP4 and the node between R3 and C2.
 - C2 is connected to the node between R4 and R3, and to GND.
 - SW2 is connected to the node between R4 and C2, and to GND.
 - The node between R4 and C2 is connected to RESET.
 - GND is connected to the bottom of C2 and SW2.

- @@ How to debounce a button (Hardware approach)
- @@ Digital Electronics: Debouncing a Push Button Switch (SPST)

ENABLE LOGIC

The Enable Logic schematic shows three ICs: IC1 (74LVC2G14GW,125), IC2 (74AHCT32BQ,115), and IC3 (74HCT08BQ,115). IC1 is a hex inverter with inputs POWER_ON (1), IC1_GND (2), and RESET (3). Its output (1Y) is connected to IC2_VCC (1) and IC2_GND_1 (7). IC2 is a NAND gate with inputs IC2_VCC (1) and IC2_GND_1 (7). Its output (8) is connected to IC3_VCC (14) and IC3_GND_1 (7). IC3 is a NAND gate with inputs IC3_VCC (14) and IC3_GND_1 (7). Its output (8) is connected to LDO_EN. Test points TP5, TP6, and TP7 are indicated.

The diagram shows a horizontal green line representing a common ground or power rail. Four vertical green lines connect this rail to four circular mounting holes labeled H1, H2, H3, and H4. The holes are red with white centers. A red arrow points to the right end of the horizontal line, labeled GND.

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