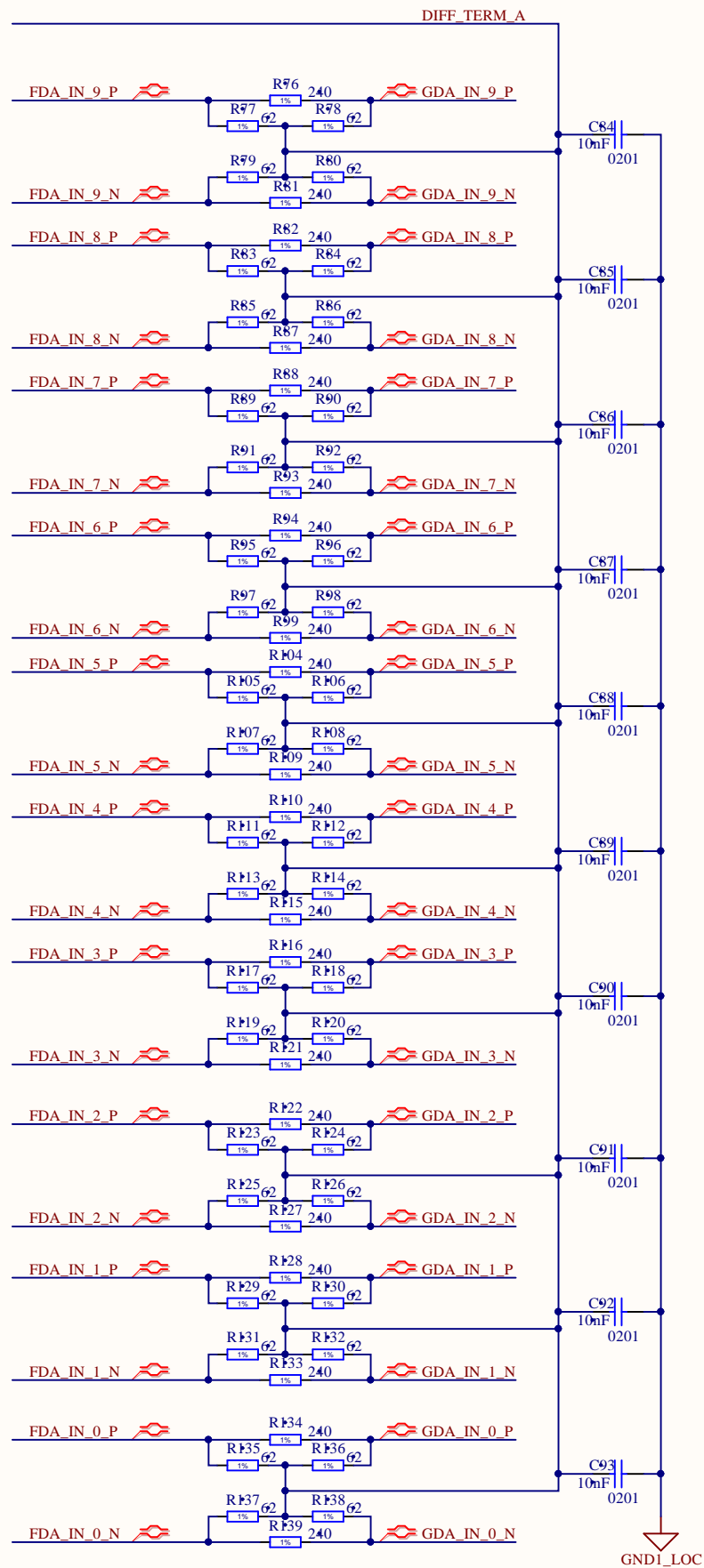


THE NETS ON THIS PAGE SHOULD COMPLETELY INDEPENDENT OF THE OTHER SCHEMATIC PAGES!!!!



A

A

B

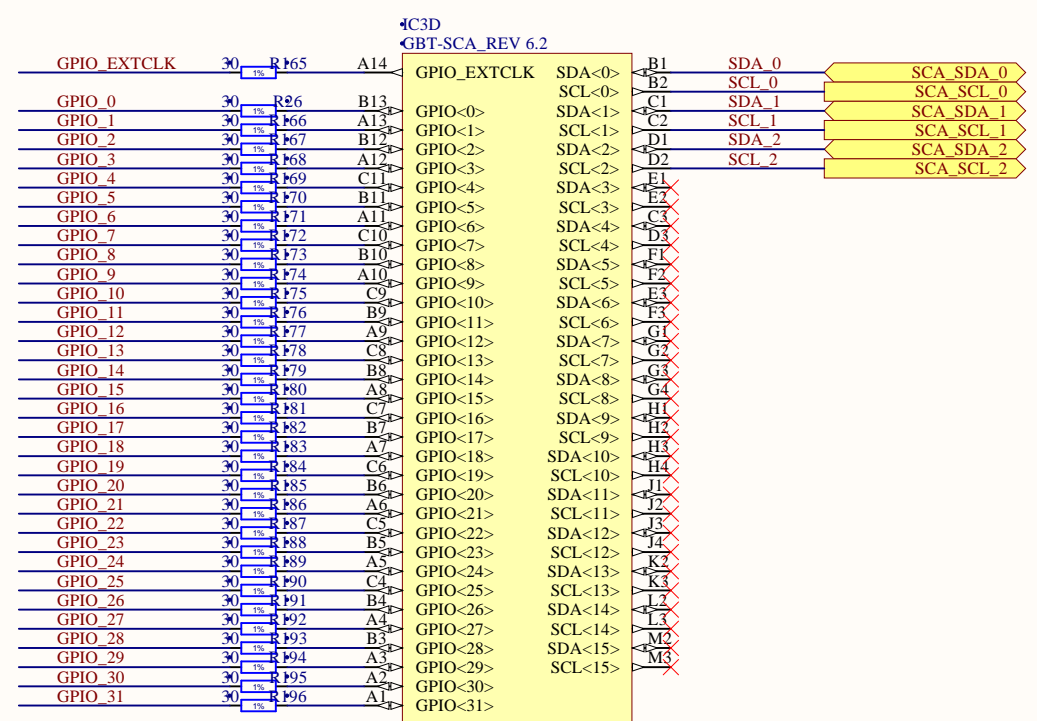
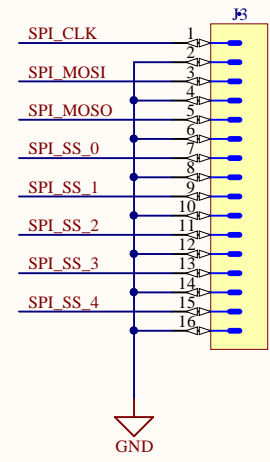
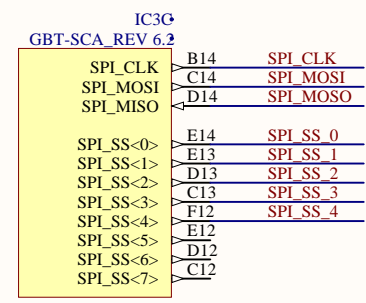
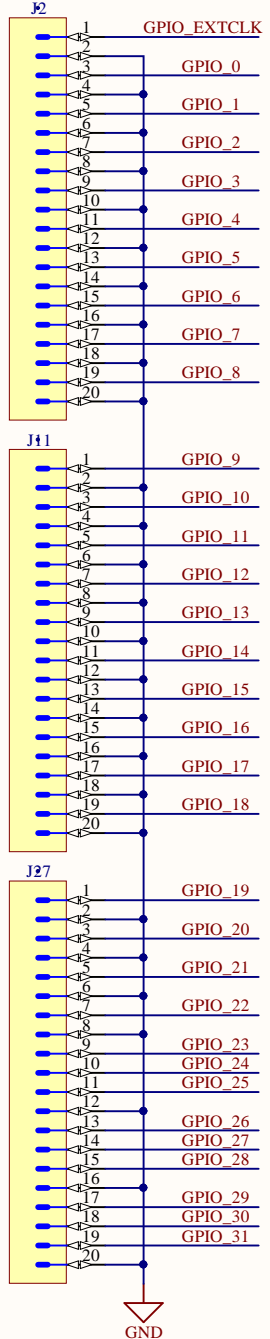
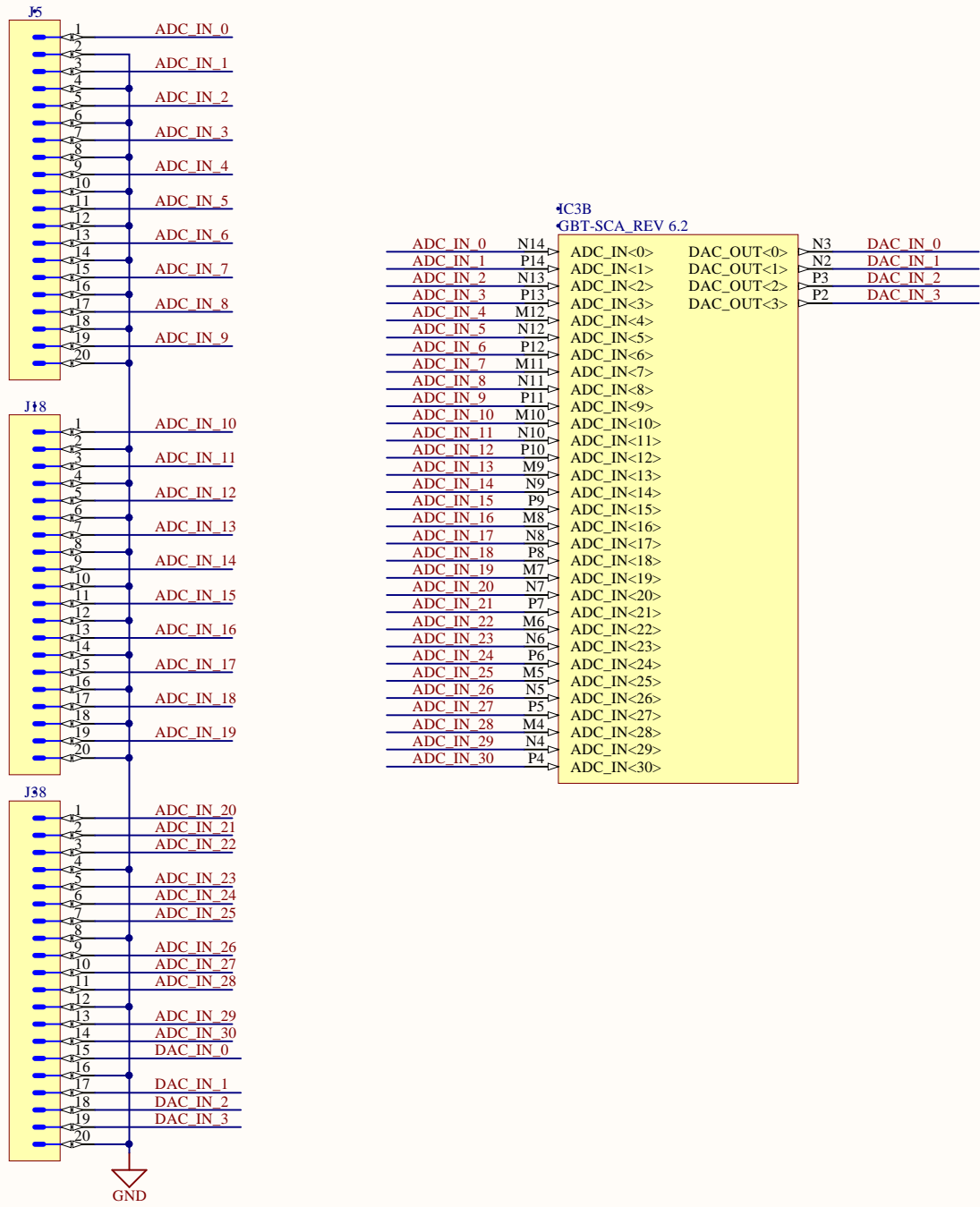
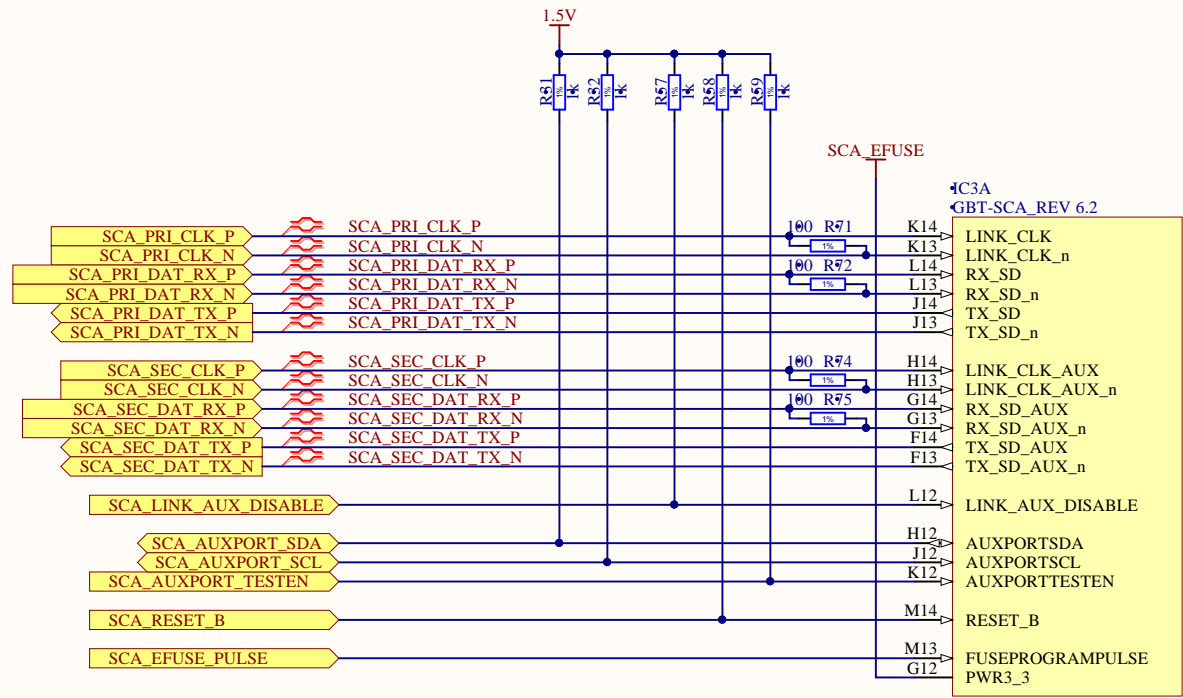
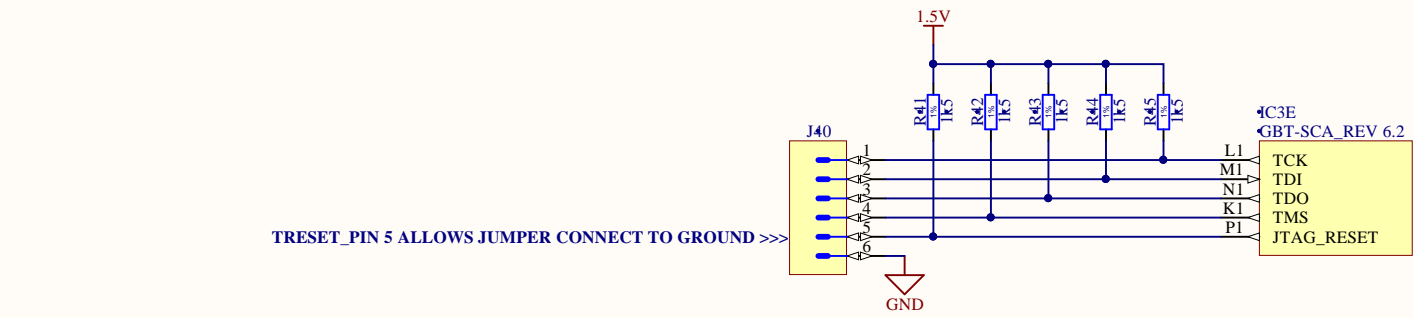
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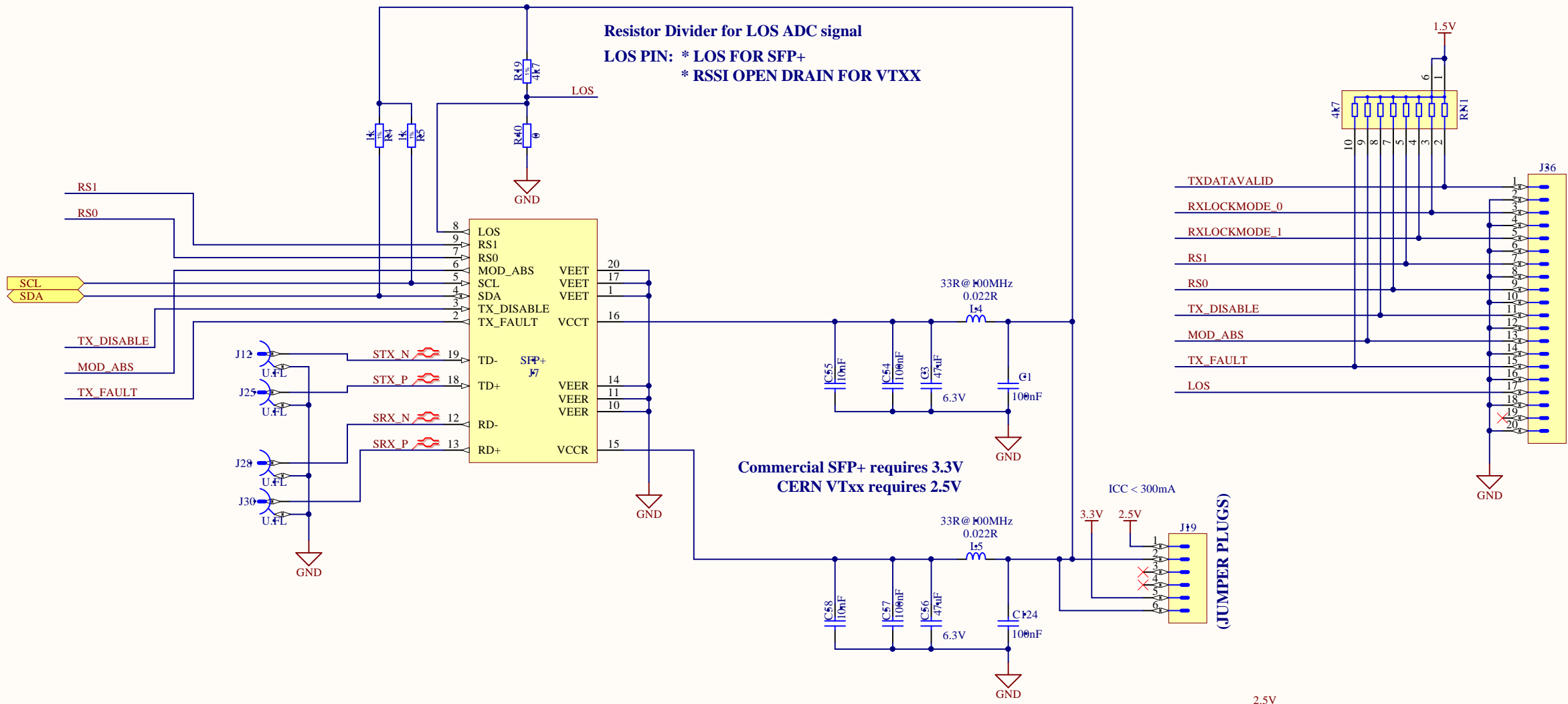
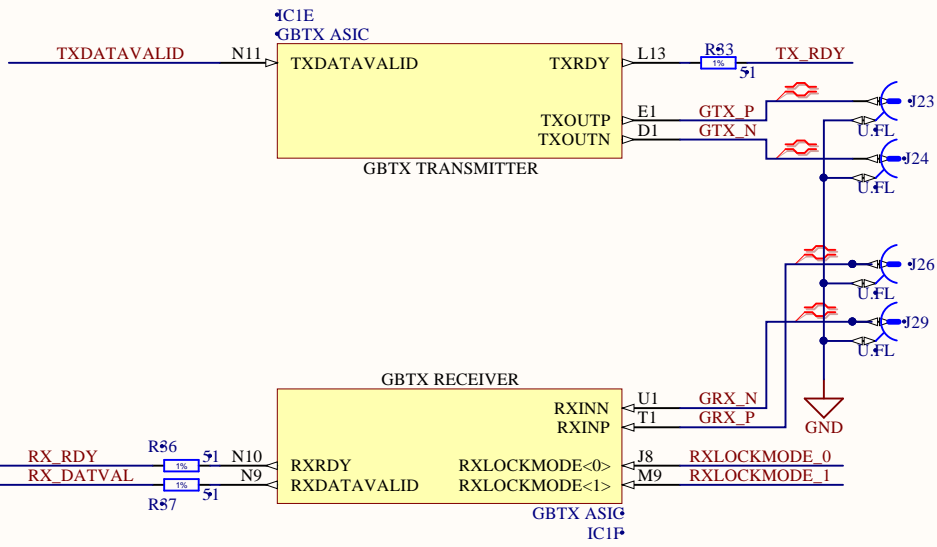
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4 Pin assignment and function

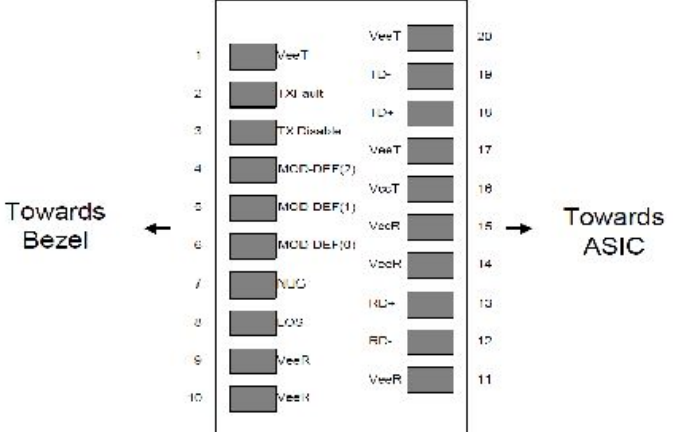
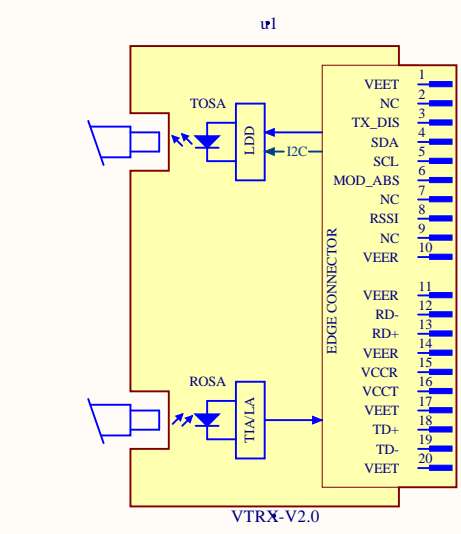


Figure 3. Pin assignment

Pin number	Name	Function	Plug sequence*	Note
1	VeeT	Transmitter ground	1	
2	TXFault	Transmitter fault indication	3	
3	TXDisable	Transmitter disable input	3	Module disables on high or open
4	MOD-DEF2	Module definition 2	3	2 wire serial ID and interface
5	MOD-DEF1	Module definition 1	3	2 wire serial ID and interface
6	MOD-DEF0	Module definition 0	3	Grounded internally via 100ohm
7	NUC	No user connection	3	Reserved for future use
8	LOS	Loss of signal indication	3	
9	VeeR	Receiver ground	1	
10	VeeR	Receiver ground	1	
11	VeeR	Receiver ground	1	
12	RD-	Negative receiver Data out	3	
13	RD+	Positive receiver Data out	3	
14	VeeR	Receiver ground	1	
15	VccR	Receiver power	2	
16	VccT	Transmitter power	2	
17	VeeT	Transmitter ground	1	
18	TD+	Positive transmitter Data in	3	
19	TD-	Negative transmitter Data in	3	
20	VeeT	Transmitter ground	1	

*Plug sequence: Pin engagement sequence during hot plugging.

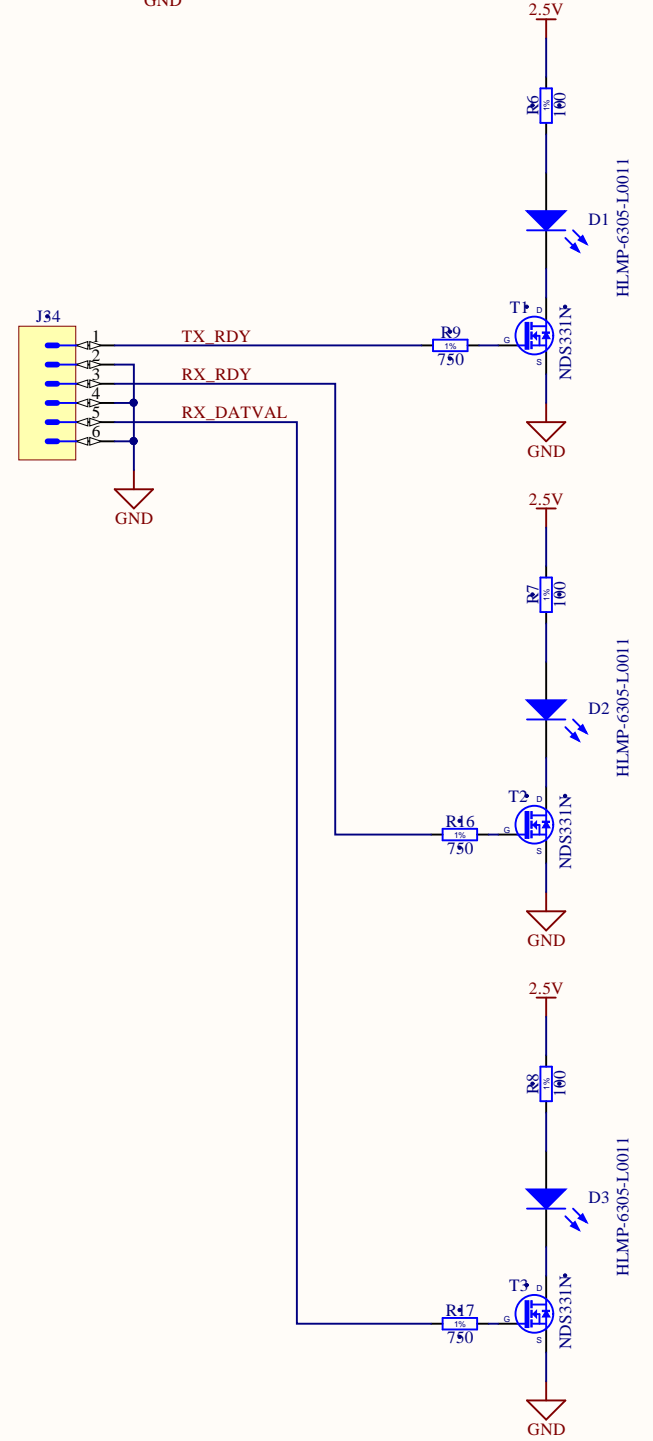


SFP+ Connector can be populated with several options:

- 1) VTTx
- 2) VTRx
- 3) Industry std SFP+ Tx/Rx
- 4) Copper SFP+ interface cable

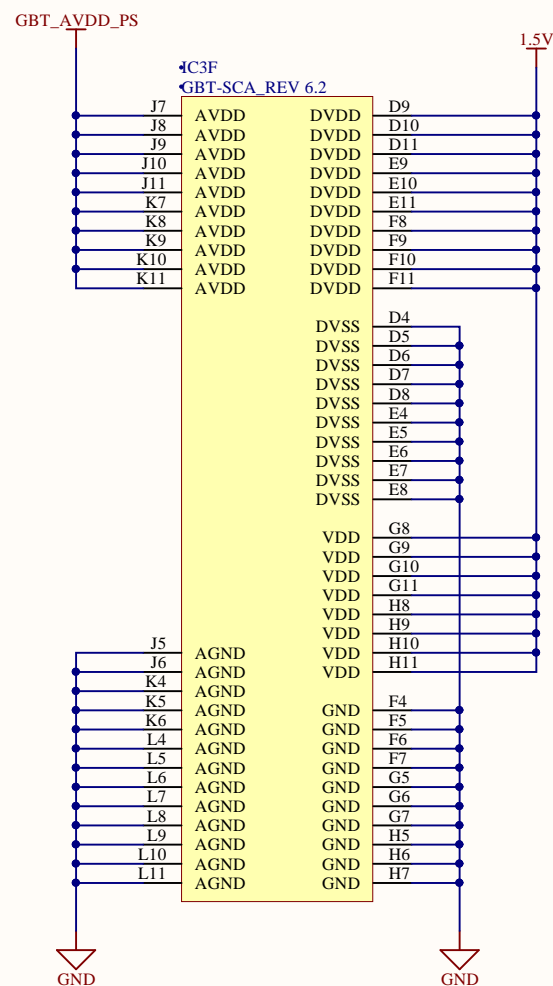
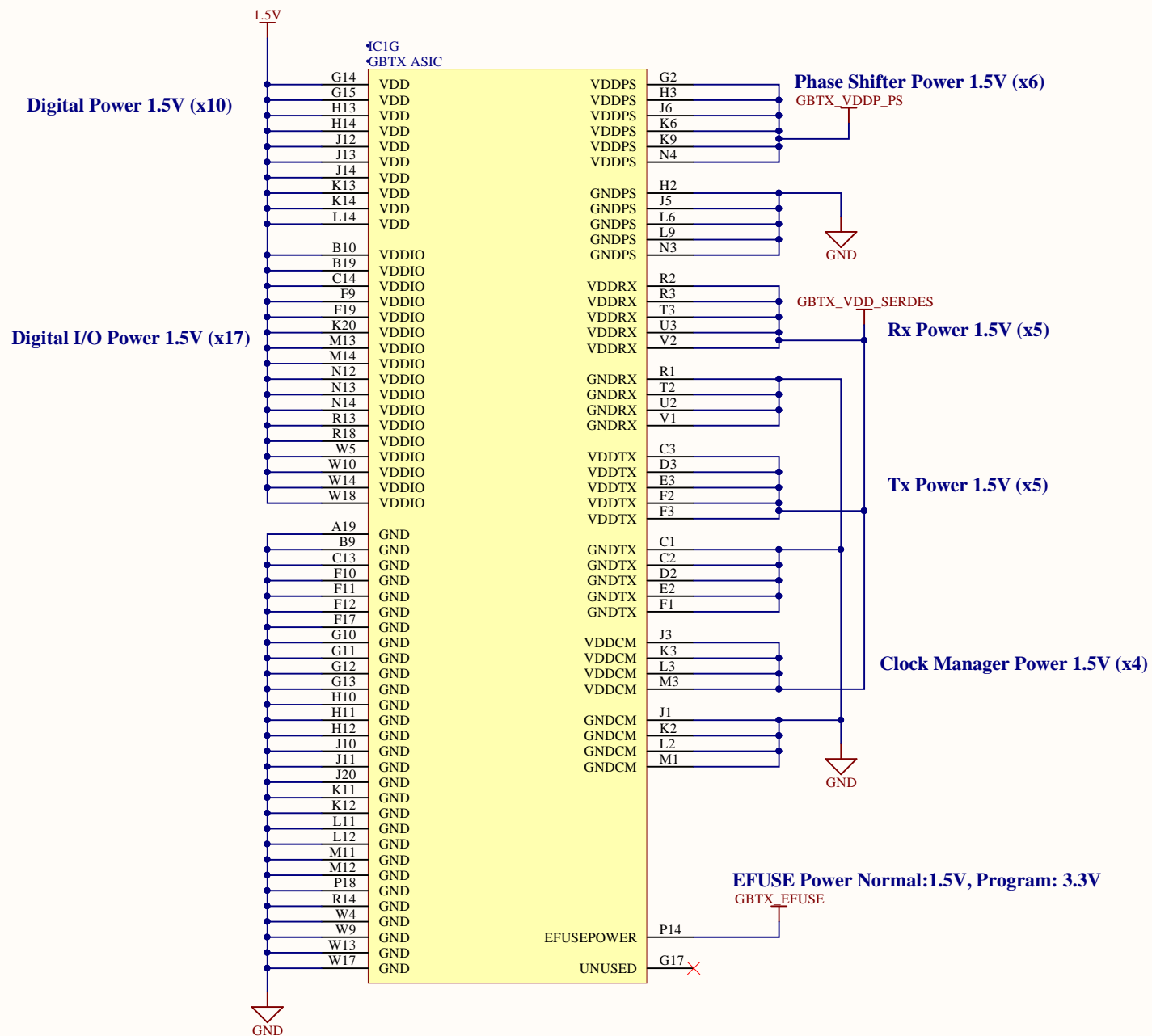
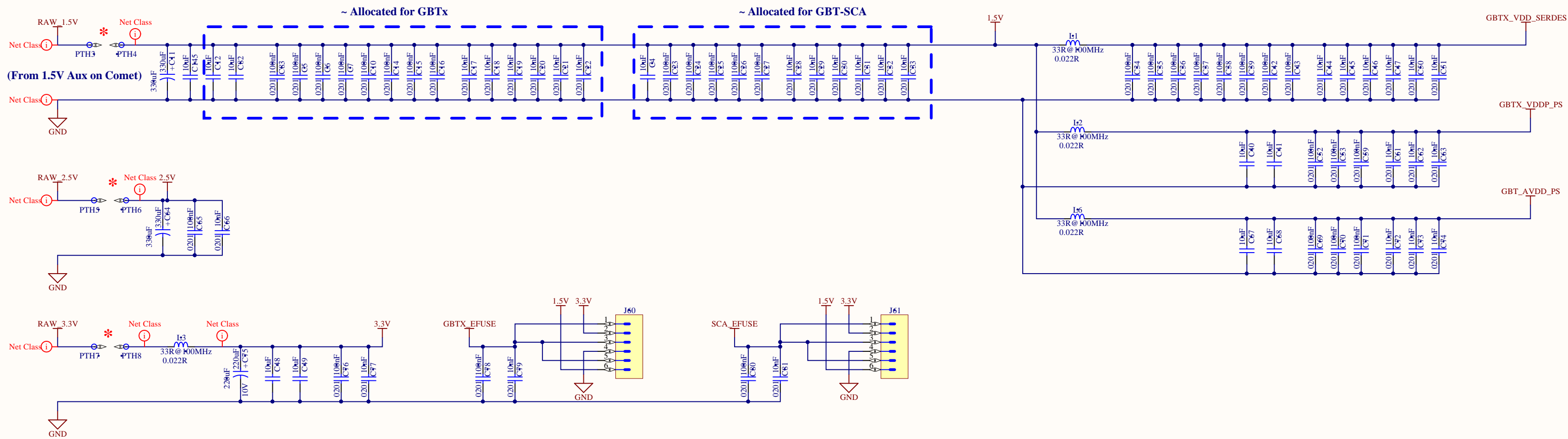
There are only 2 functional applications

- a) single Tx using either VTTx, VTRx, or SFP+
Unused Tx channel to be jumper configured with failsafe jumper resistors for DC coupled or 320 MHz clock if module contains internal AC coupling capacitors. This allows thermal evaluation.
- b) Standard Tx/Rx using either VTRx or SFP+
The i2C of Commercial SFP+ modules must be provided by the COMET FPGA using 3.3V pullups.
The i2C of CERN VTxx modules must be provided by the GBTx using 1.5V pullups.



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*** WIRE LOOP BETWEEN PLATED THRU HOLES TO ALLOW FOR Hall Effect Sensor CURRENT MEASUREMENTS**



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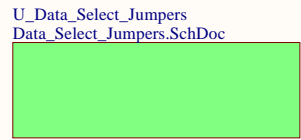
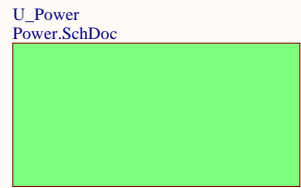
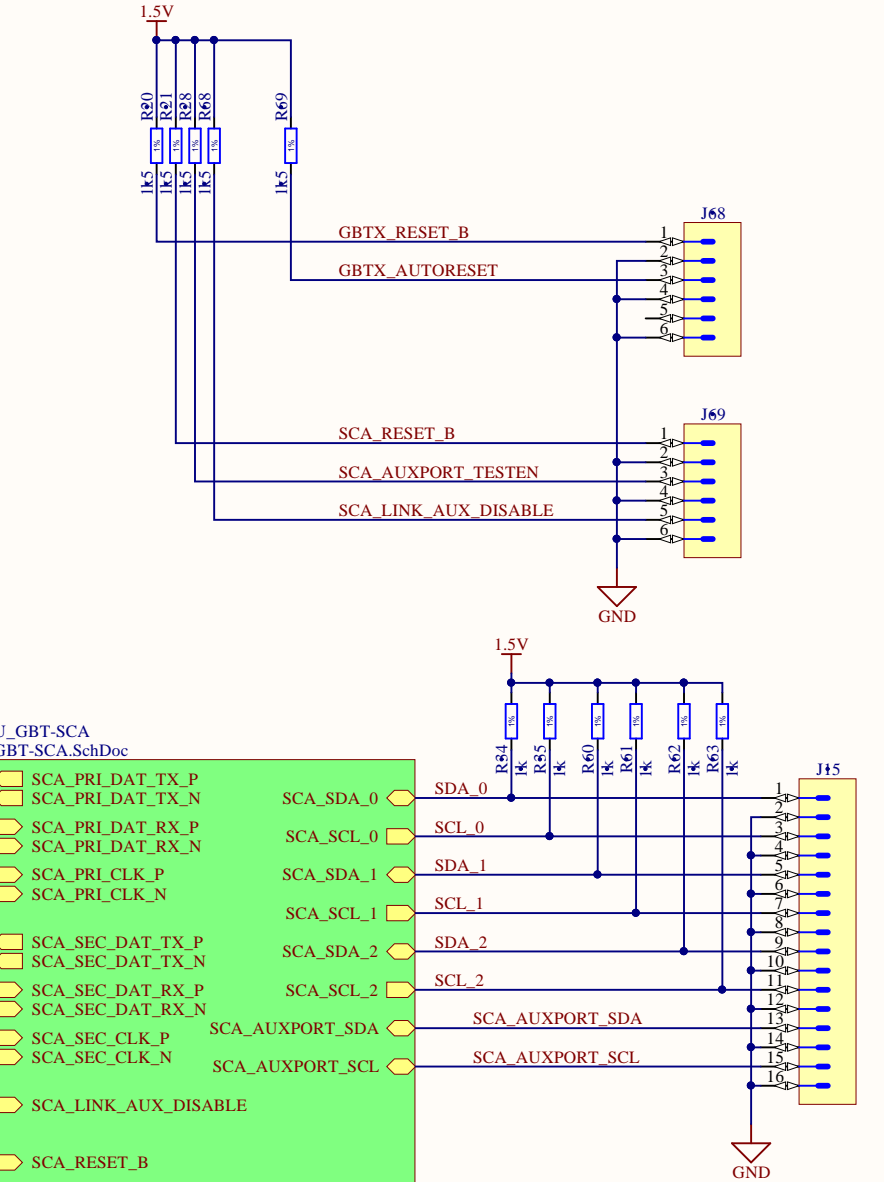
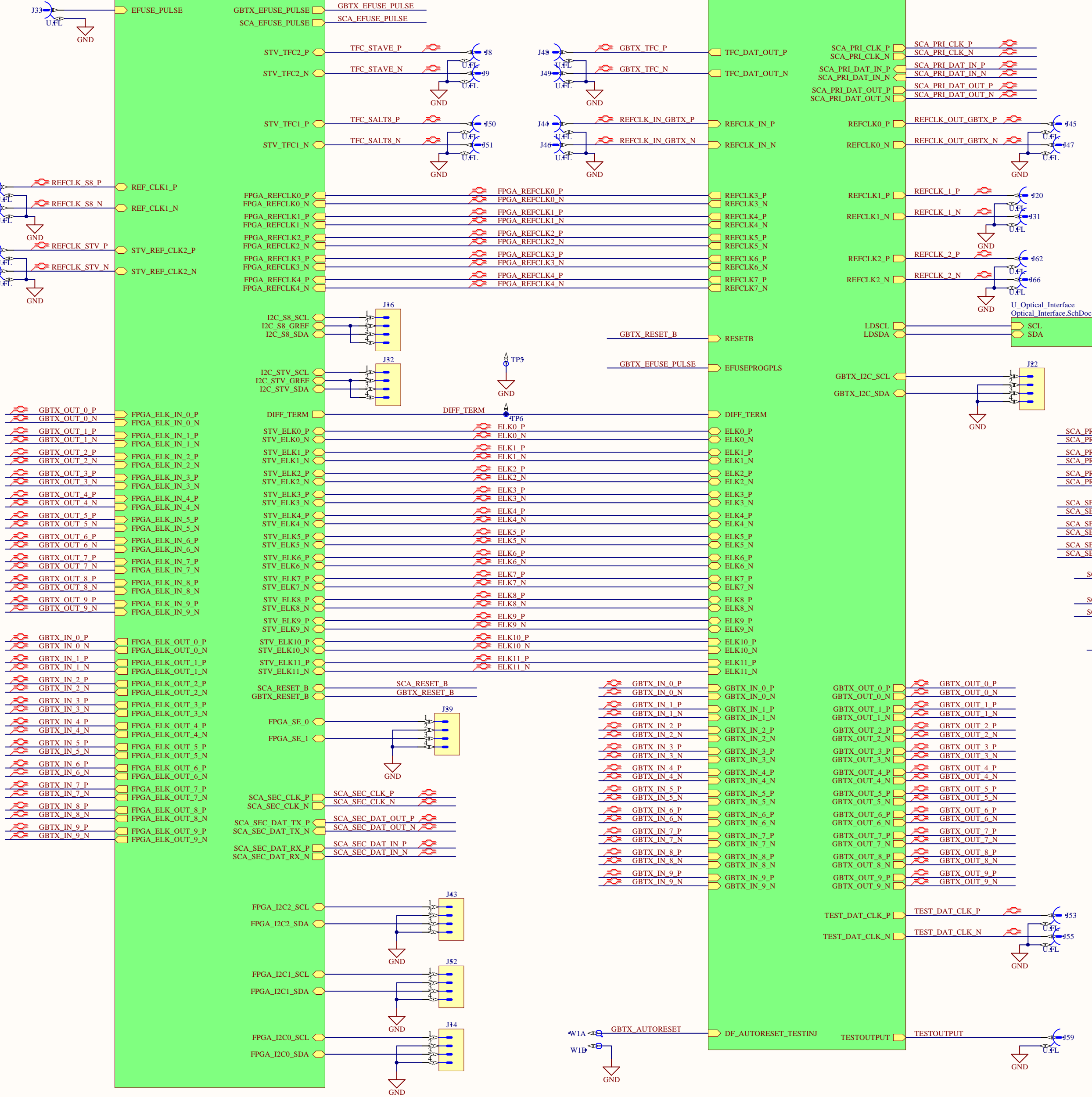
U.FL CONNECTORS CONNECTED TO THE STAVE VIA ERx8

LSHM_CONNS
LSHM_CONNS.SchDoc

U_GBTx_ALL_PORTS
GBTx_ALL_PORTS.SchDoc

Note 1: The SALT8 test board ERx8 connector signal-pins assignments restrict the location to the furthest out STAVE position.
The associated signals specific to SALT8 testing include:
i2C_S8 interface
TFC_SALT8
REF_CLK_SALT8

NOTE 2: The following signals are available at all of the STAVE positions
i2C_ST interface
TFC_STAVE
REF_CLK_STAVE
ELK[11:0]



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