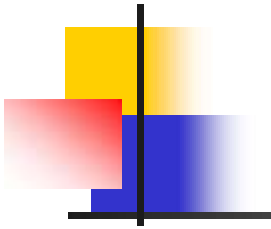
Registers

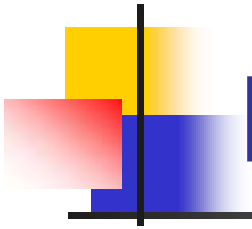


Registers and Counter

- The filp-flops are essential component in clocked sequential circuits.

  Circuits that include filp-flops are usually classifed by the function they perform. Two such circuits are registers and counters.

- An n-bit register consists of a group of n flip- flops capable of storing n bits of binary information.



Registers

- In its broadest definition, a register consists a group of flip-flops and gates that effect their transition.
  - The flip-flops hold the binary information.
  - The gates determine how the information is transferred into the register.
- Counters are a special type of register.
- A counter goes through a predetermined sequence of states.

Registers

- Fig shows a register constructed with four D-type filpflops.
- "Clock" triggers all flip-folps on the positive edge of each pulse.
- "Clear" is useful for clearing the register to all 0's prior to its clocked operation.

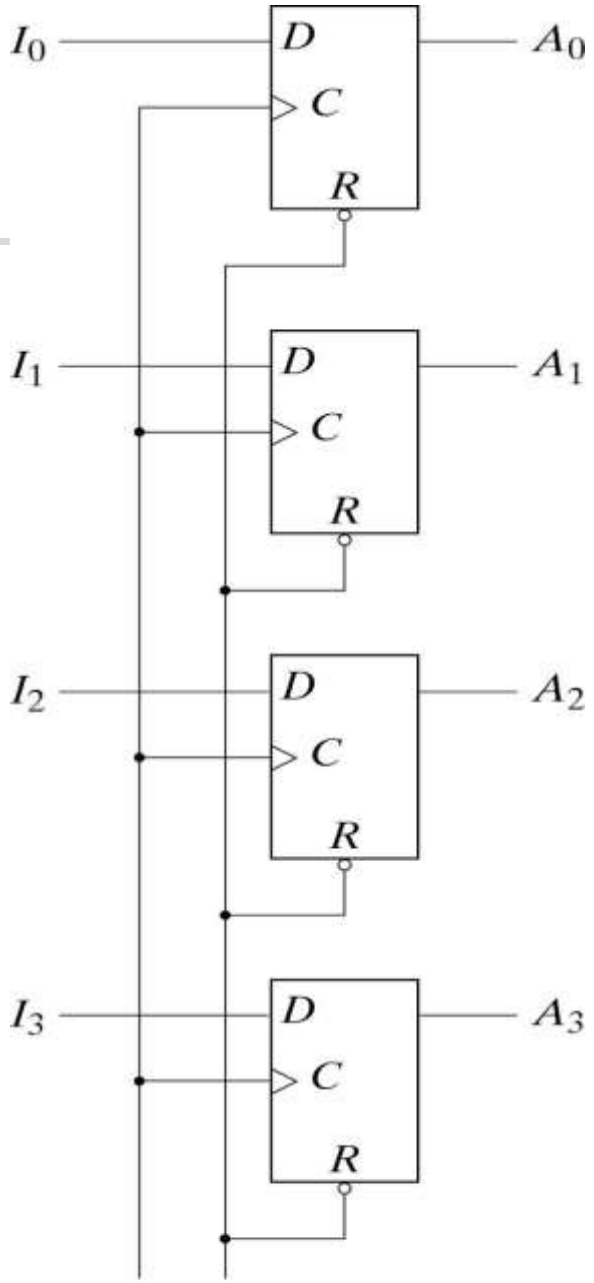
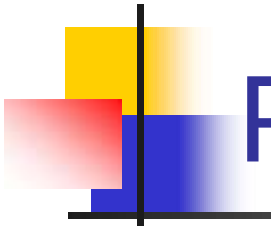


Fig. 6-1 4-Bit Register



Register with Parallel Load

- A clock edge applied to the C inputs of the register of Fig. 6-1 will load all four inputs in parallel.
- For synchronism, it is advisable to control the operation of the register with the D inputs rather than controlling the clock in the C inputs of the flip-flops.
- A 4-bit register with a load control input that is directed through gates and into the D inputs of the flip-flops si shown in Fig. 6-2.

Register with Parallel Load

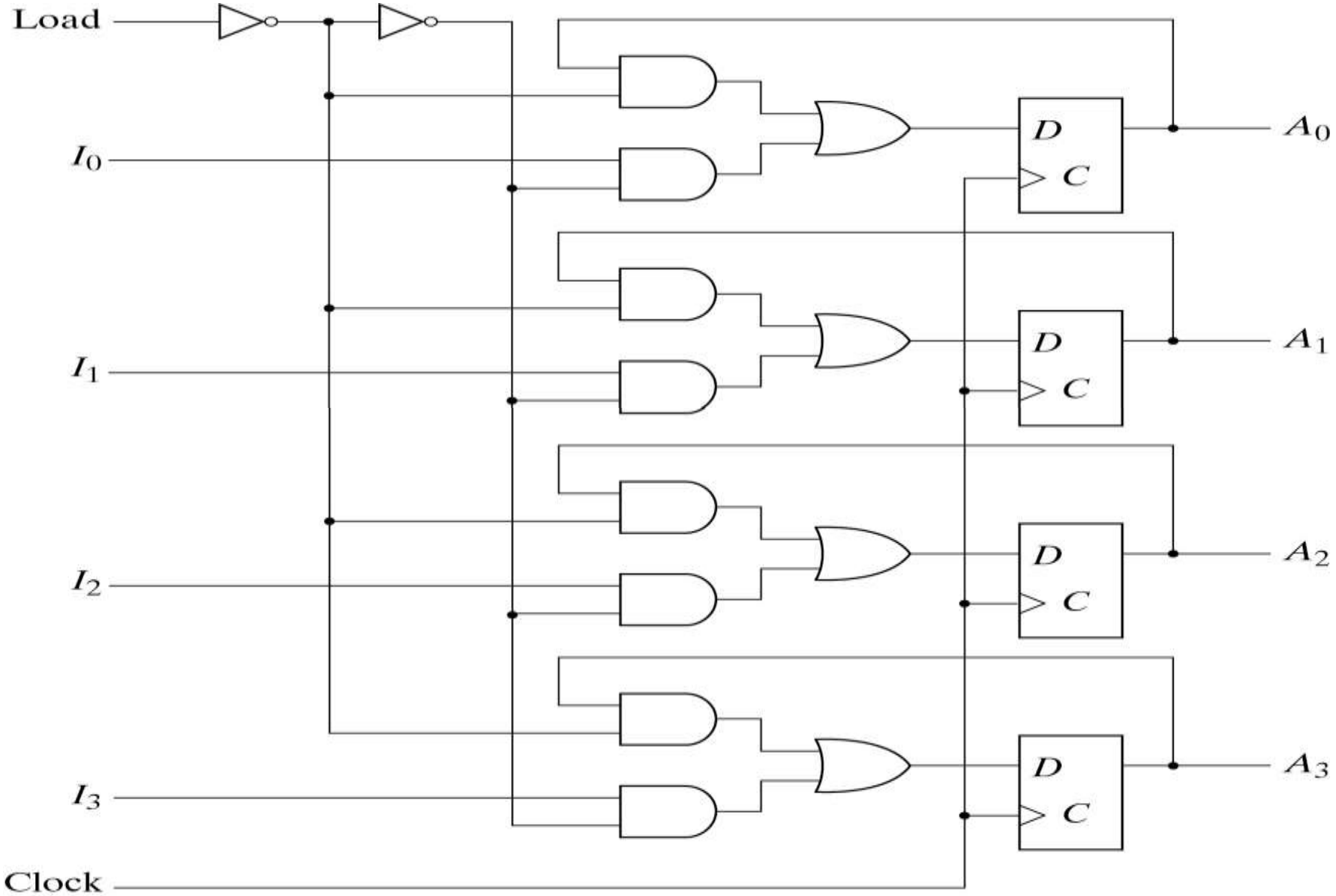
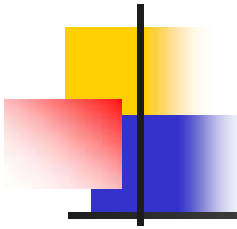


Fig. 6-2 4-Bit Register with Parallel Load



Register with Parallel Load

- When the load input is 1 , the data in the four inputs are transferred into the register with next positive edge of the clock.
- When the load input is 0 ,the outputs of the flip-flops are connected to their respective inputs.
- The feedback connection from output to input is necessary because the D flip-flops does not have a “no change” condition.

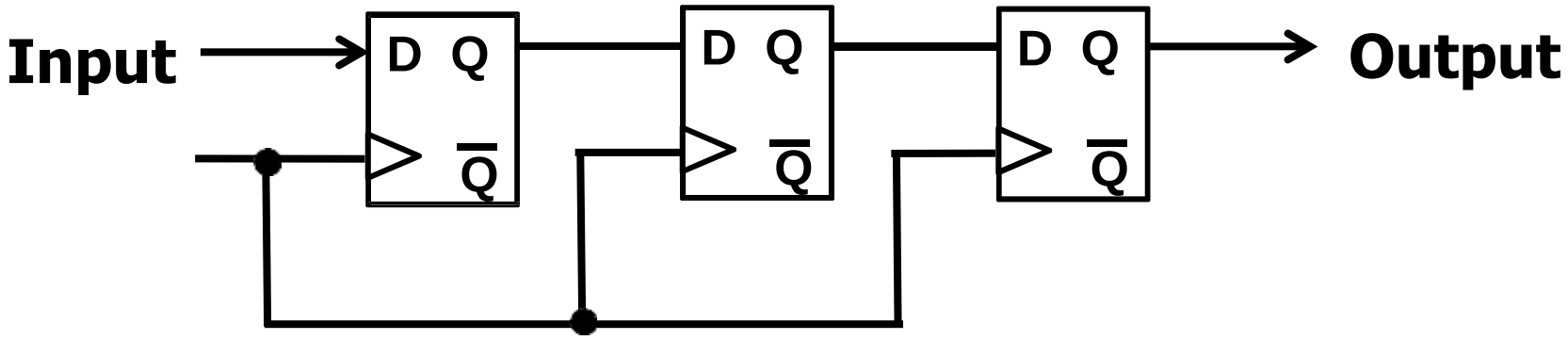
Shift Registers & its Types

Construction

- Shift registers are constructed from flip-flops due to their characteristics:
  - Edge-triggered devices
  - Output state retention
- Each Flip-Flop in a shift register can retain one binary digit.
  - For instance, if a 5-bit binary number needs to be stored and shifted, 5 flip-flops are required.
- Each binary digit transfer operation requires a clock edge.
- Asynchronous inputs are useful in resetting the whole configuration.

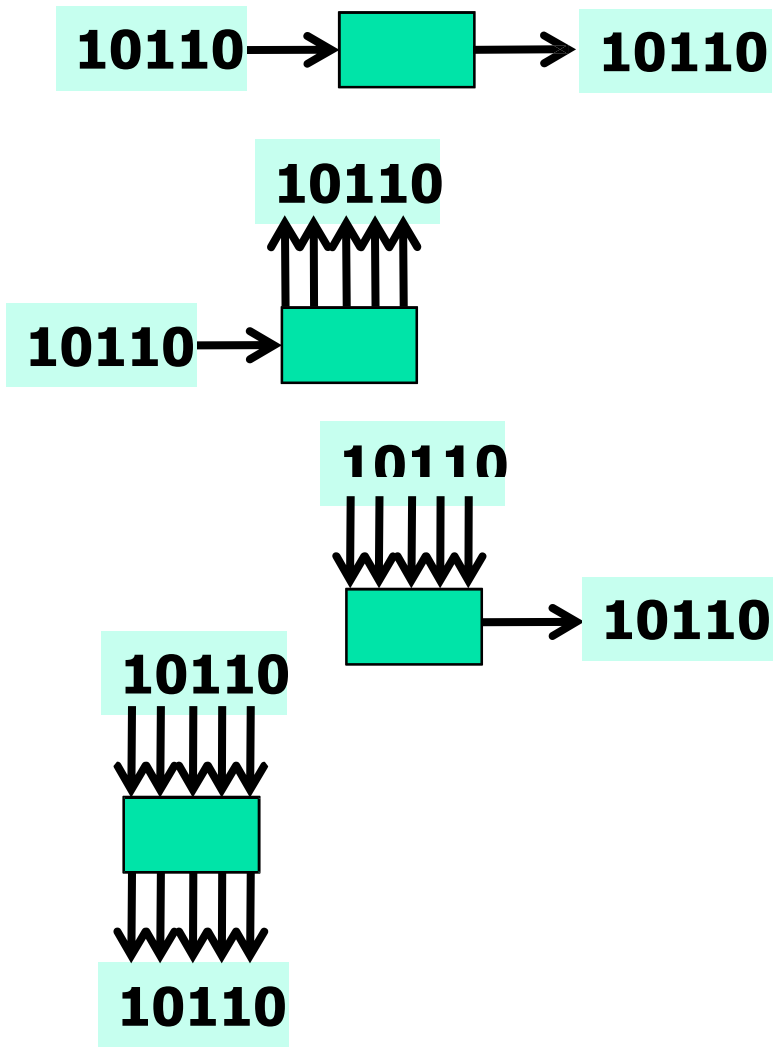
Shift Register Construction

- Shift registers are comprised of D Flip-Flops that share a common clock input.



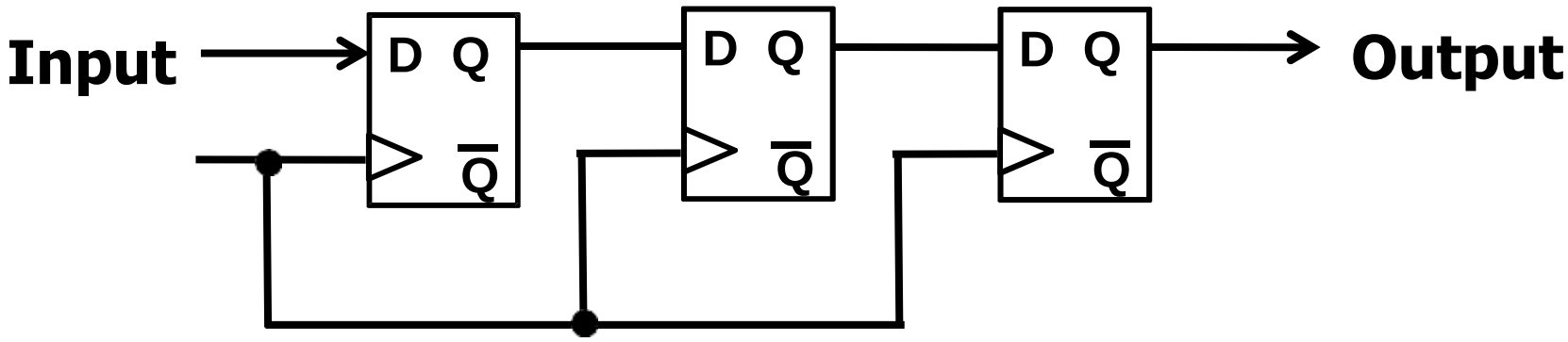
Shift Register Types

- SISO: Serial In, Serial Out
- SIPO: Serial In, Parallel Out
- PISO: Parallel In, Serial Out
- PIPO: Parallel In, Parallel Out



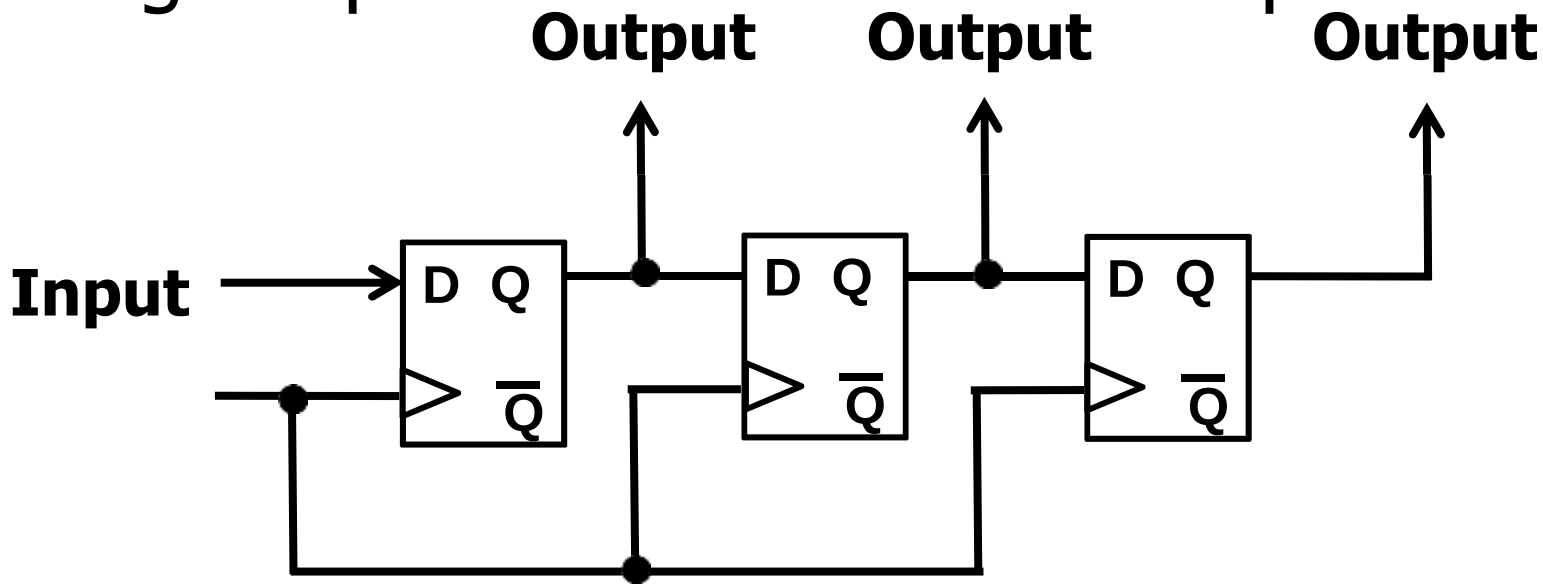
SISO Flip-Flop Shift Register

- a **Serial In Serial Out** shift register has a single input and a single output



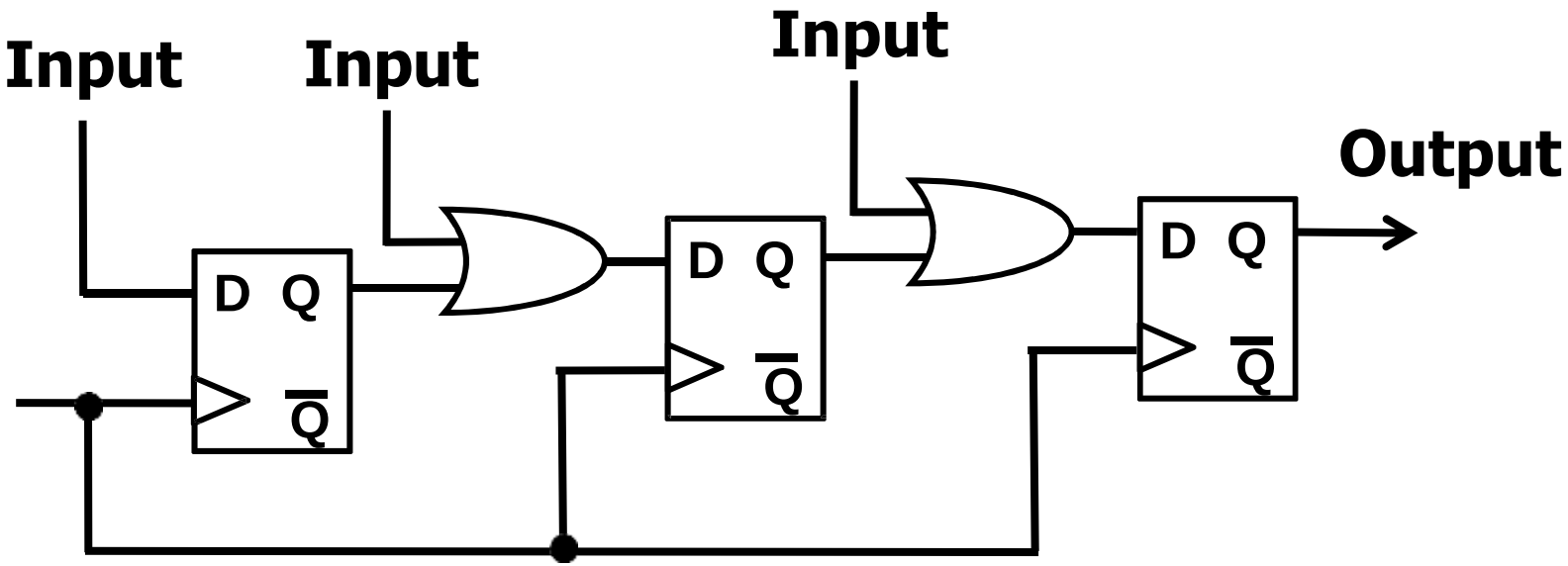
SIPO Flip-Flop Shift Register

- a **Serial In Parallel Out** shift register has a single input and access to all outputs



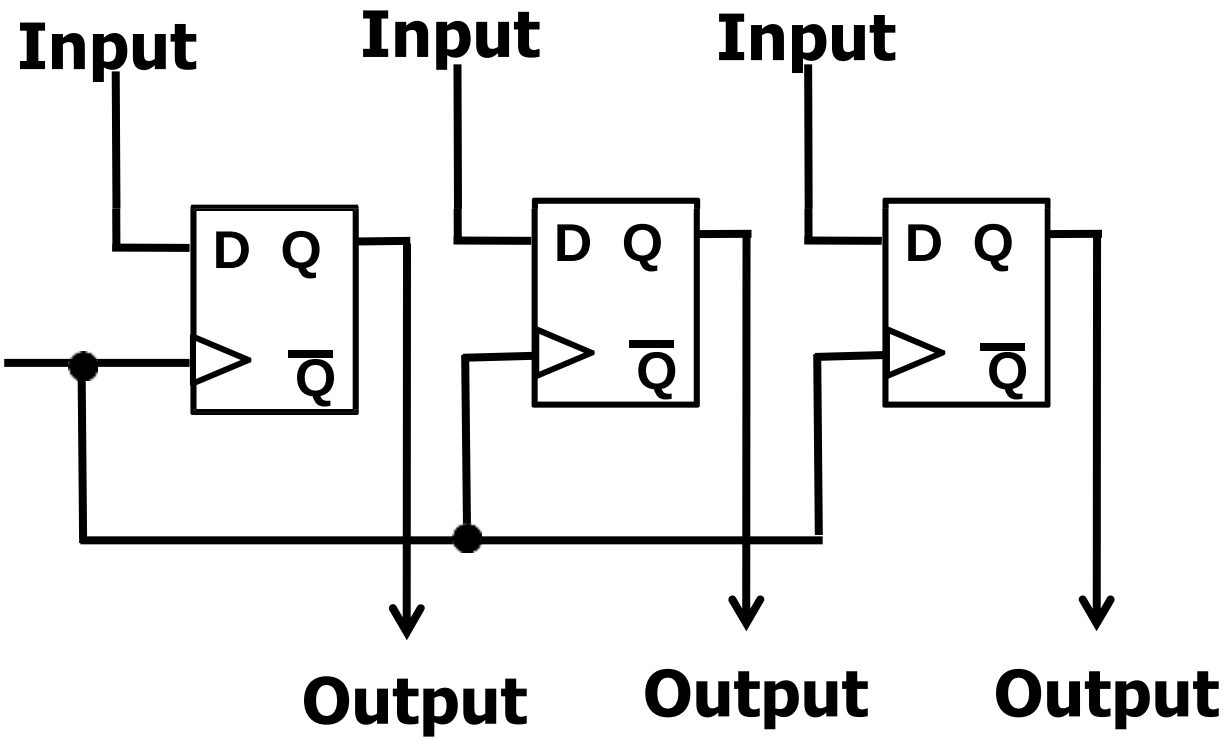
PISO Flip-Flop Shift Register

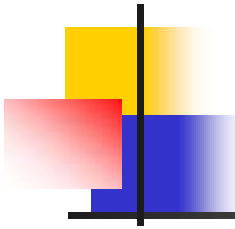
- a **Parallel In Serial Out** shift register requires additional gates. In this example the parallel input must revert to logic low; in other configurations steering gates are used to switch between loading and shifting operations.



PIPO Flip-Flop Shift Register

- a **Parallel In Parallel Out** register has the simplest configuration. It represents a memory device.

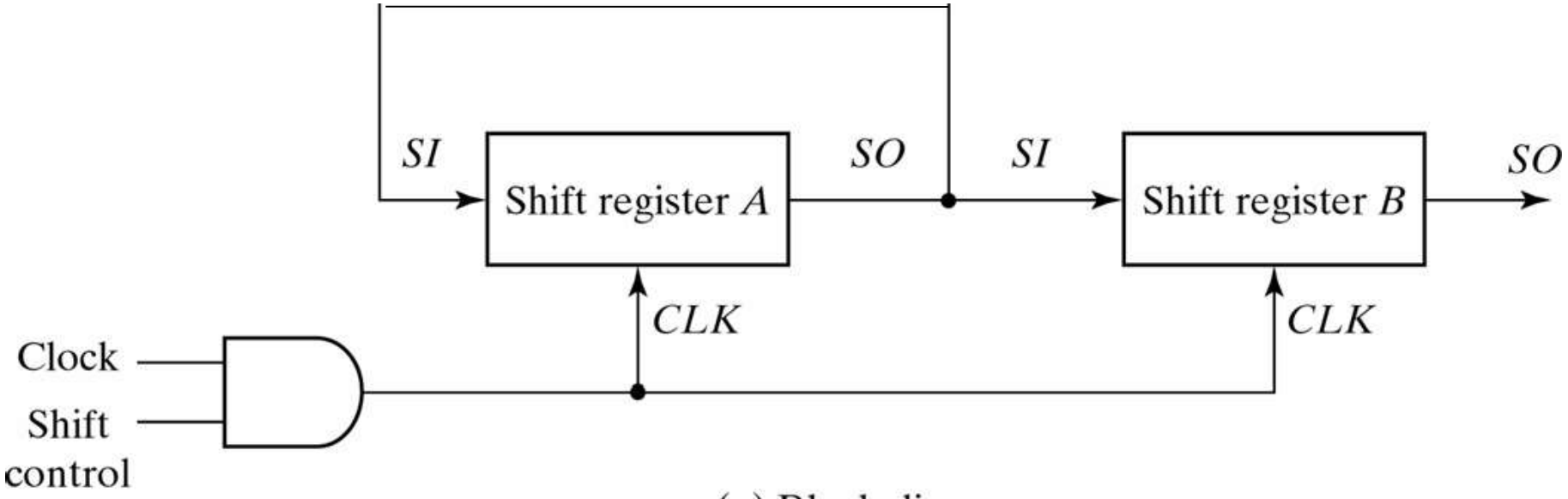




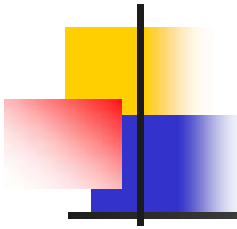
Serial Transfer

- A digital system is said tp operate in a serial mode when information is transferred and manipulated one bit at a time.
- This in contrast to parallel transfer where all the bits of the register are transferred at the same time.
- The serial transfer us done with shift registers, as shown in the block diagram of Fig. 6-4(a).

Serial Transfer



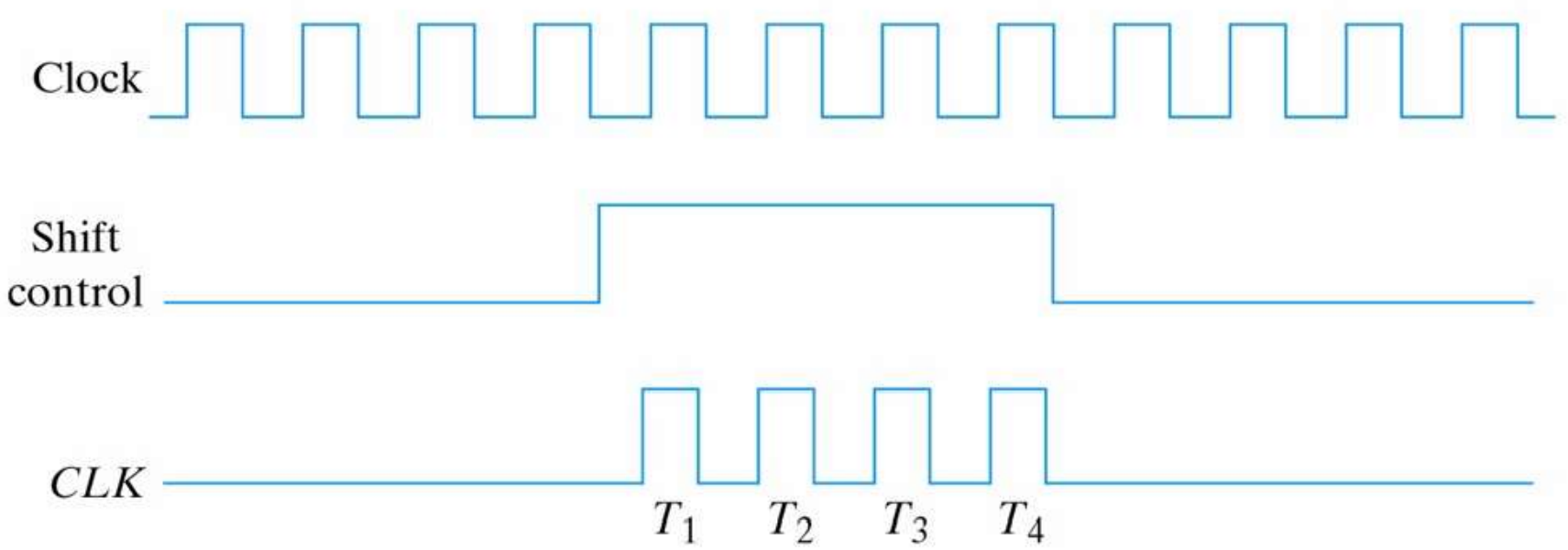
(a) Block diagram



Serial Transfer

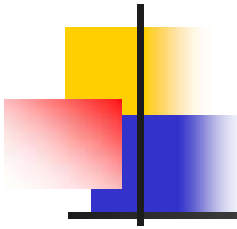
- To prevent the loss of information stored in the source register, the information in register A is made to circulate by connecting the serial output to its serial input.
- The shift control input determines when and how many times the registers are shifted. This is done with an AND gate that allows clock pulses to pass into the CLK terminals only when the shift control is active. [Fig. 6-4(a)].

Serial Transfer



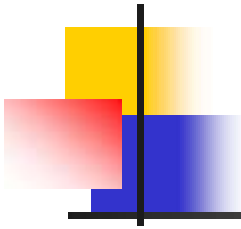
(b) Timing diagram

Fig. 6-4 Serial Transfer from Register *A* to register *B*



Serial Transfer

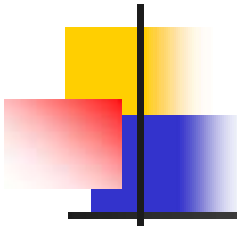
- The shift control signal is synchronized with the clock and changes value just after the negative edge of the clock.
- Each rising edge of the pulse causes a shift in both registers. The fourth pulse changes the shift control to 0 and the shift registers are disabled.



Serial Transfer

Table 6-1
Serial-Transfer Example

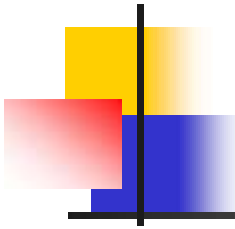
Timing Pulse	Shift Register A	Shift Register B
Initial value	1 0 1 1	0 0 1 0
After T1	1 1 0 1	1 0 0 1
After T2	1 1 1 0	1 1 0 0
After T3	0 1 1 1	0 1 1 0
After T4	1 0 1 1	1 0 1 1



Serial Transfer

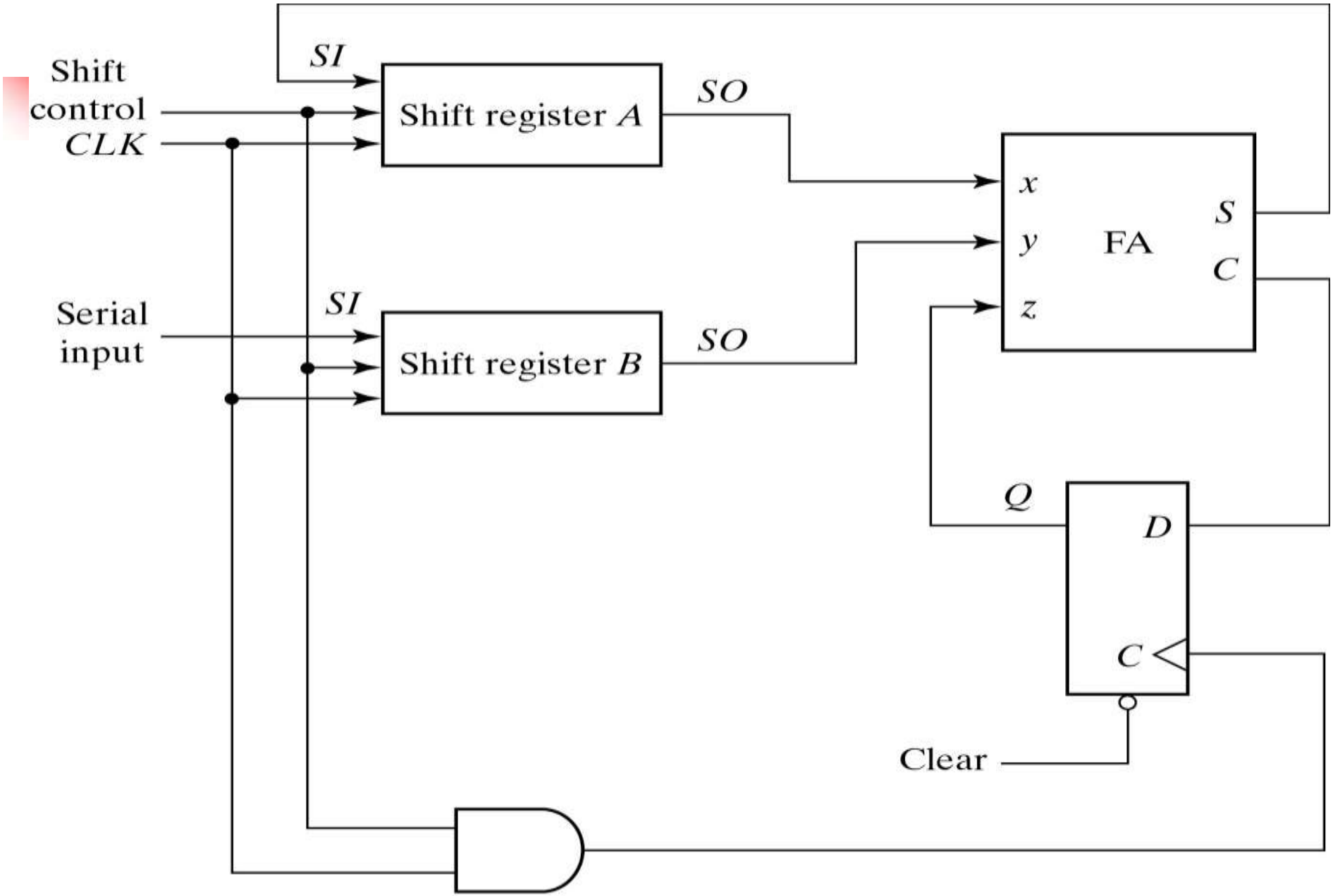
- In the parallel mode, information is available from all bits can be transferred simultaneously during one clock pulse.
- In the serial mode, the registers have a single serial input and a single serial output. The information us transferred one bit at a time while the registers are shifted in the same direction.

Serial Adder

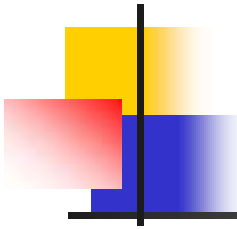


Serial Adder

- Operations in digital computers are usually done in parallel because this is a faster mode of operation.
- Serial operations are slower, but have the advantage of requiring less equipment.
- The two binary numbers to be added serially are stored in two shift registers.
- Bits are added one pair at a time through a single full adder.

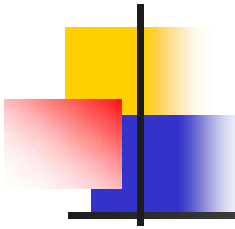


Block Diagram – Serial Adder



Serial Adder

- By shifting the sum into A while the bits of A are shifted out, it is possible to use one register for storing both the augend and sum bits.
- The carry out of the full adder is transferred to a D flip-flop.
- The output of the D flip-flop is then used as carry input for the next pair of significant bits.



Serial Adder

- To show that serial operations can be designed by means of sequential circuit procedure, we will redesign the serial adder using a state table.
- The serial outputs from registers are designated by x and y.
- The sequential circuit proper has two inputs, x and y, that provide a pair of significant bits, an output S that generates the sum bit, and flip-flop Q for storing the carry. [Table. 6-2]

Design a serial adder using JK flip flop

Table: State Table for serial Adder using JK

Present State	Inputs		Next State	Output	Flip-Flop Inputs	
Q	X	y	Q (Carry)	S (Sum)	J_Q	K_Q
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

Serial Adder using JK

- The two flip-flop input equations and the output equation can be simplified by means of map to obtain
  - $J_Q = xy$
  - $K_Q = x'y' = (x+y)'$
  - $S = x \oplus y \oplus Q$
- The circuit diagram is shown in following fig

Serial Adder using JK

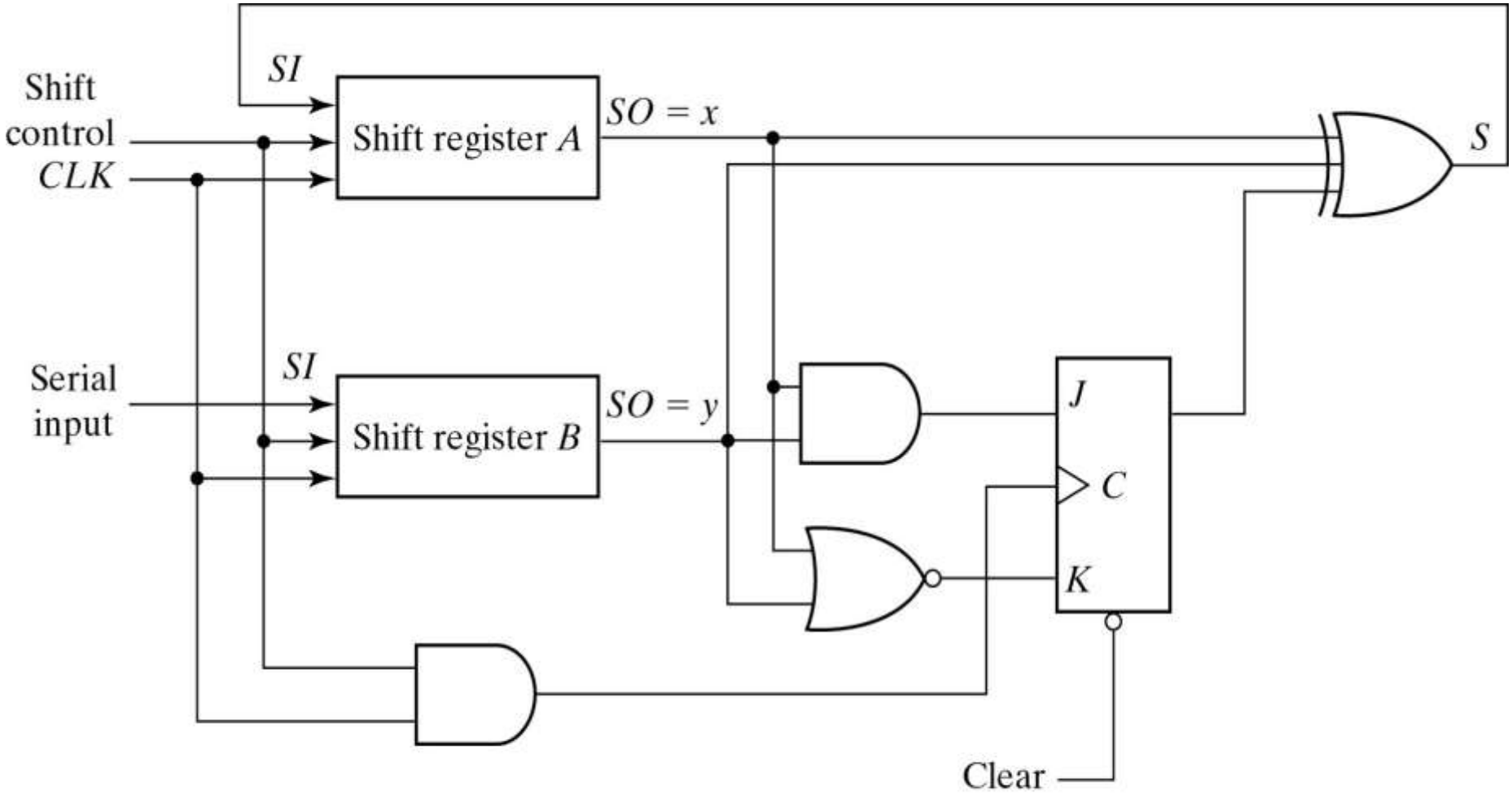
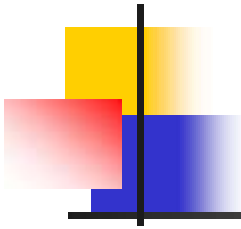


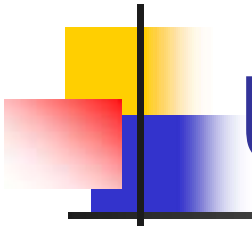
Fig. 6-6 Second form of Serial Adder

Universal Shift Register



Universal Shift Register

- A *clear* control to clear the register to 0.
- A *clock* input to synchronize the operations.
- A *shift-right* control to enable the shift operation and the *serial input* and *output* lines associated with the shift right.
- A *shift-left* control to enable the shift operation and the *serial input* and *output* lines associated with the shift left.



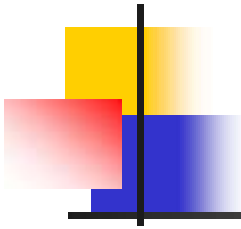
Universal Shift Register

- A *parallel-load* control to enable a parallel transfer and the n input lines associated with the parallel transfer.
- n parallel output lines.
- A control state that leaves the information in the register unchanged in the presence of the clock.
- If the register has both shifts and parallel load capabilities, it is referred to as a *universal shift register*.

Universal Shift Register

Table 6-3
Function Table for the Register of Fig. 6-7

Mode Control		
S_1	S_0	Register Operation
0	0	No Change
0	1	Shift right
1	0	Shift Left
1	1	Parallel load



Universal Shift Register

- Shift registers are often used to interface digital system situated remotely from each other.
- If the distance is far, it will be expensive to use n lines to transmit the n bits in parallel.
- Transmitter performs a parallel-to-serial conversion of data and the receiver does a serial-to-parallel conversion.

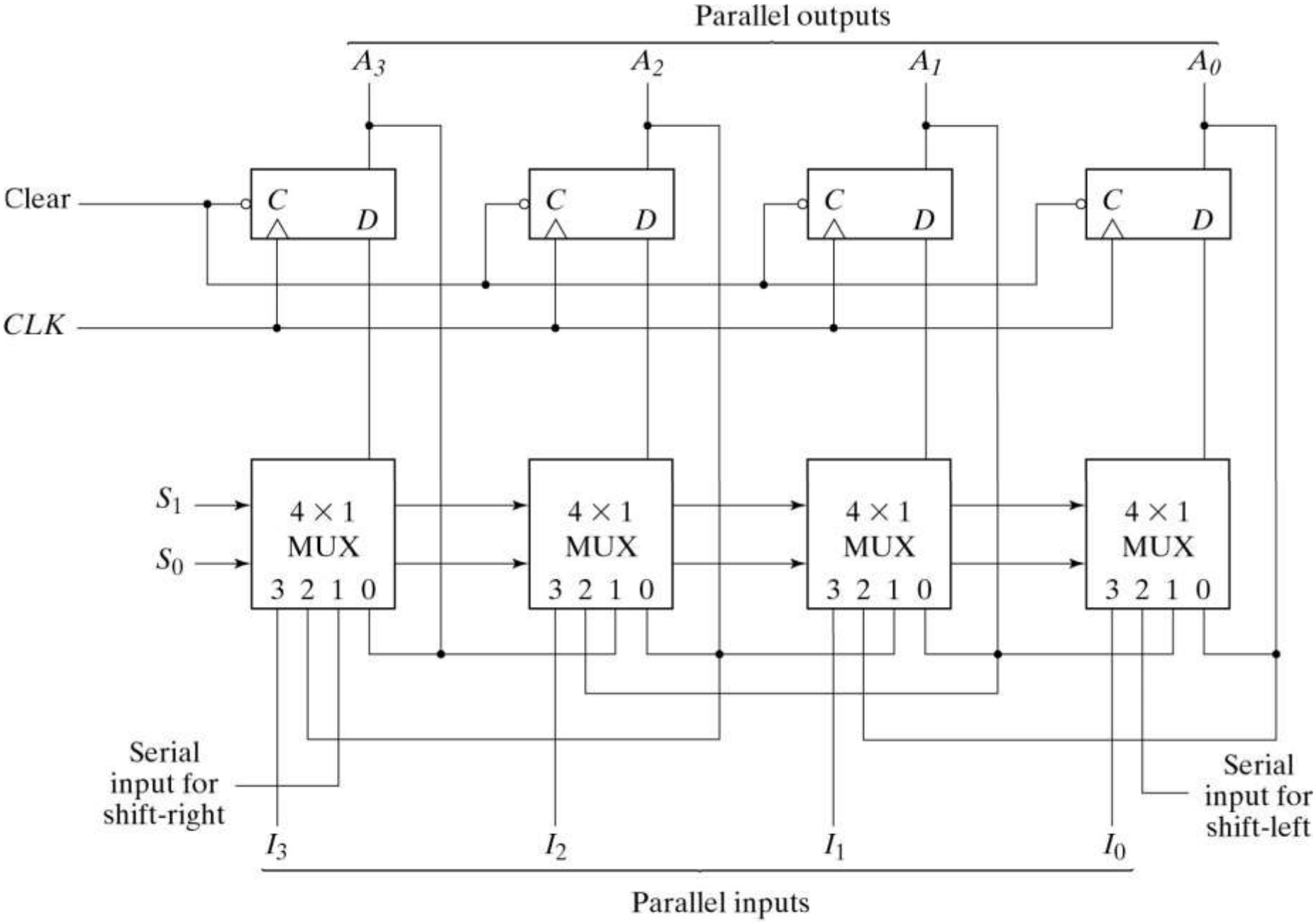


Fig. 6-7 4-Bit Universal Shift Register