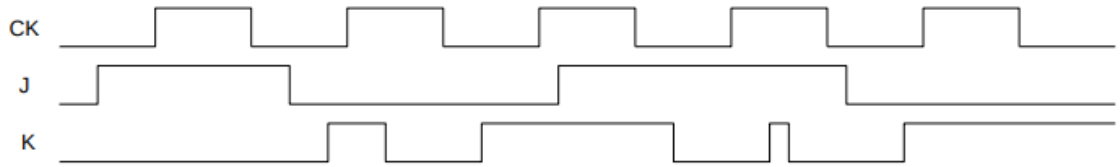
Exercise 1.

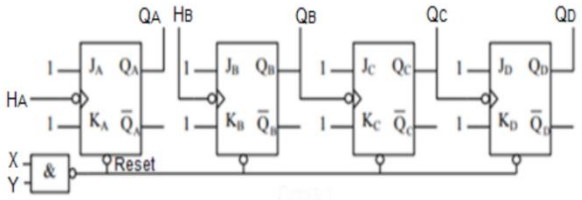
For the input sequence in the below figure, draw the output waveform of:

a) a negative edge-triggered JK flip-flop,
b) a positive edge-triggered JK flip-flop.



Exercise 2:

Consider the diagram in the figure below:



Given that:

- In addition to the JK inputs and the clock input H, the JK flip-flop has a Reset input that is active low and has priority over all other inputs.
- As soon as Reset=0, Q=0.

1. For what values of X and Y are the flip-flops reset to 0?
2. By drawing the timing diagram of the flip-flops QA, QB, QC, and QD, show that when QA=HB (where QA and HB are connected together), the circuit functions as a modulo-16 counter.
3. We need to design an asynchronous modulo-9 counter using JK flip-flops. Provide the corresponding circuit diagram.

Exercise 3:

Design a finite state machine that detects the sequence 1011 in a binary stream.

- Draw the state diagram.
- Provide the state transition table.

- Implement the machine using D flip-flops and logic gates.

Exercise 4:

- Design a 4-bit shift register that shifts data to the right with each clock pulse.
- Modify the shift register to include a parallel load feature.
- Describe its operation and draw the diagram.

Exercise 5:

Design a 4-bit universal shift register capable of the following operations:

- Shift left.
- Shift right.
- Parallel load.
- Hold.

1. Draw the circuit diagram.
2. Explain the control logic for selecting operations.

Exercise 6:

Design a 4-bit counter that can count both up and down depending on a control signal UP.

- Write the state table.
- Use JK flip-flops to implement the design.
- Simulate its behavior for UP=1and UP=0.

Exercise 7:

1. Design a 4-bit **ring counter** using D flip-flops.
2. Initialize the counter with 1000.
3. Explain its operation and draw the timing diagram for four clock cycles.
4. Repeat the three first questions for the **johnson counter**