الجمهـــوريــــــــة الجزائريــــــــة الديمــقـــراطيــــــــة الشعبيـــــــــة
People`s Democratic Republic of Algeria

Ministry of Higher Education and Scientific Research
National School of Cyber Security
Foundation Training Department

وزارة التعـليـــم العـــالـي والـبحــــث العــلـمـي
المدرســـة الوطنيـــة العليــا في الأمن السيبراني
قســـم التكويـــن القــــاعدي

Surname : ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ First Name : ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░

N° Student Card : ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ Date : ░ ░ / ░ ░ / ░ ░ ░ ░

Section : ░ ░ ░ ░ Group : ░ ░

Module : ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ Academic Year : ░░ ░ / ░ ░ ░ ░

CODE : Reserved for administration

MARK :

/ 20

CODE:

reserved for administration

Marker's Fullname :

…………………………

…………………………

…………………………

Invigilator :

…………………………

…………………………

…………………………

…………………………

…………………………

…………………………

Exercise 1: (04 points)

Select the correct answer (0.5 point for each correct answer)

1. **In a sequential circuit, the output at any time depends only on the input values at that time.**
   - a) Past output values
   - b) Intermediate values
   - **c) Both past output and present input**
   - d) Present input values

2. **In 1-to-4 Demultiplexer, how many select lines are required ?**
   - **a) 2**
   - b) 3
   - c) 1
   - d) 4

3. **All logic operations can be obtained by means of**
   - a) AND and NAND operations
   - b) OR and NOR operations
   - c) OR and NOT operations
   - **d) NAND and NOR operations.**

4. **Don't care conditions can be used for simplifying Boolean expressions in**
   - a) Registers
   - b) Terms
   - **c) K-maps**
   - d) Latches

5. **A 4-bit serial-parallel shift register has:**
   - a) Four serial inputs and four parallel outputs
   - b) One parallel input and four serial outputs
   - **c) One serial input and four parallel outputs**
   - c) four parallel input and four parallel outputs

6. **An asynchronous 4-bit counter:**
   - a) Is controlled by a single clock
   - b) Uses flip-flops that are synchronized with each other
   - c) Has a faster output frequency than the input clock
   - **d) Has flip-flops that are not all triggered simultaneously**

7. **What is the main function of a decoder?**
   - a) Multiply digital signals
   - b) Convert analog signals to digital signals
   - **c) Convert a binary input to a specific output**
   - d) Invert a binary signal

This area will be cut.

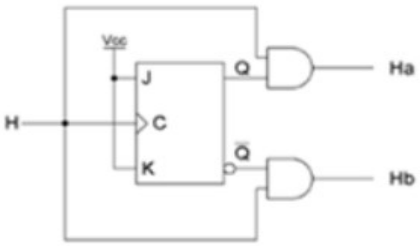
8. In a synchronous counter, the flip-flops are:

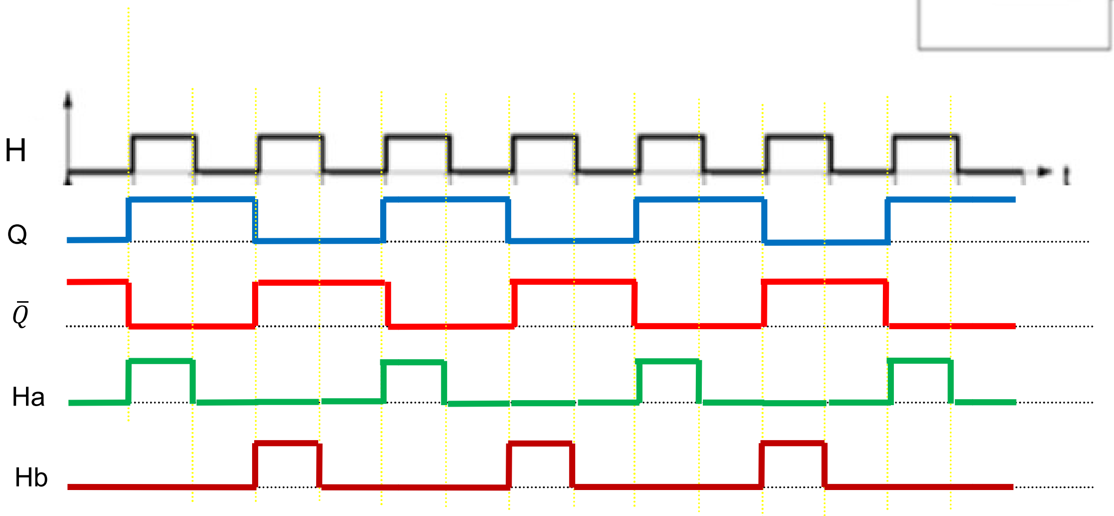
a) Triggered by independent input signals
b) **Triggered by the same clock signal**
c) Triggered asynchronously
d) Always of a different type (T, D, JK)

Exercise 2: (04 points)

From this figure, complete the below chronogram:

(1 point for each correct chronogram: Q, $\bar{Q}$, Ha and Hb)





Exercise 3: (06 points)

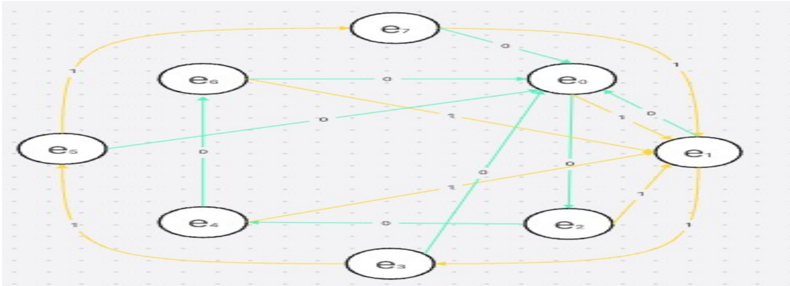
You are tasked with designing a synchronous counter that operate based on the control input S, as indicated in the table below:

Value of S	Counter Sequences
S=0	**0→2→4→6→0**
S=1	**1→3→5→7→1**

The counter uses a 3-bit binary representation for its states. The following rules must be followed:

a) The counter must correctly transition between states in the given sequence for each value of **S**.
b) If the initial state is invalid (does not belong to the sequence defined by **S**), the counter should automatically transition to the first valid state of the corresponding sequence.

1. Draw the Finite State Machine (FSM) for the counter, indicating the transitions between states for S=0 and S=1. (1point)



2. Calculate the minimum number of flip-flops required to represent these states.

The number of flip-flips is 3 (0.25 point)

3. Complete a state transition table indicating the current state, the next state for each value of S, and the outputs of the D flip-flops. (1point)
4. Derive the excitation equations for the D flip-flops.

Inputs				Next states			D flip-flops		
S	Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	D_2	D_1	D_0
0	0	0	0	0	1	0	0	1	0
0	0	0	1	0	0	0	0	0	0
0	0	1	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0
0	1	0	0	1	1	0	1	1	0
0	1	0	1	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0
1	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	1	0	1	1
1	0	1	0	0	0	1	0	0	1
1	0	1	1	1	0	1	1	0	1
1	1	0	0	0	0	1	0	0	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	0	0	1	0	0	1
1	1	1	1	0	0	1	0	0	1

$D_2 = \sum(2, 4, 11, 13)$ (0.25 point)

$= \bar{S}\bar{Q}_2Q_1\bar{Q}_0 + \bar{S}Q_2\bar{Q}_1\bar{Q}_0 + S\bar{Q}_2Q_1Q_0 + SQ_2\bar{Q}_1Q_0$

$D_1 = \sum(0, 4, 9, 13)$ (0.25 point)

$= \bar{S}\bar{Q}_2\bar{Q}_1\bar{Q}_0 + \bar{S}Q_2\bar{Q}_1\bar{Q}_0 + S\bar{Q}_2\bar{Q}_1Q_0 + SQ_2\bar{Q}_1Q_0$

$D_0 = \sum(8, 9, 10, 11, 12, 13, 14, 15)$ (0.25 point)

$= S\bar{Q}_2\bar{Q}_1\bar{Q}_0 + S\bar{Q}_2\bar{Q}_1Q_0 + S\bar{Q}_2Q_1\bar{Q}_0 + S\bar{Q}_2Q_1Q_0 + SQ_2\bar{Q}_1\bar{Q}_0 + SQ_2\bar{Q}_1Q_0 + SQ_2Q_1\bar{Q}_0 + SQ_2Q_1Q_0$

5. Simplify the excitation equations using Karnaugh maps.

SQ_2 \ Q_1Q_0	00	01	11	10
00				
01				
11	1	1	1	1
10	1	1	1	1

$D_0 = S$ (0.5 point)

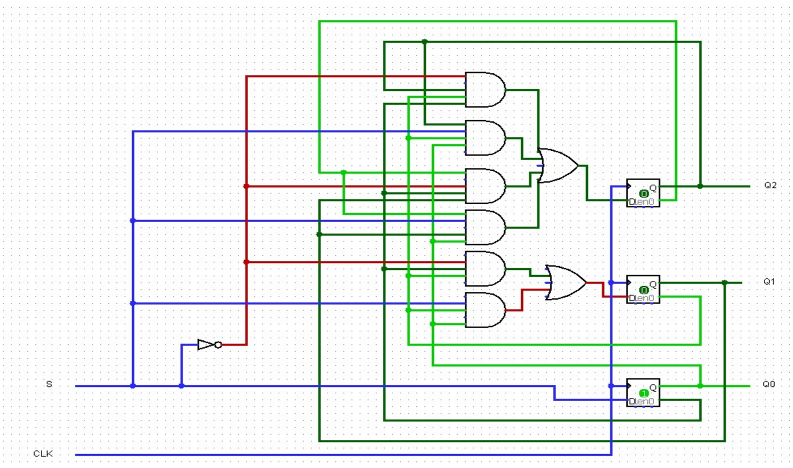
SQ_2 \ Q_1Q_0	00	01	11	10
00	1			
01	1			
11		1		
10		1		

$D_1 = S\bar{Q}_1Q_0 + \bar{S}\bar{Q}_1\bar{Q}_0$ (0.5 point)

SQ_2 \ Q_1Q_0	00	01	11	10
00				1
01	1			
11		1		
10			1	

$D_2 = \bar{S}Q_2\bar{Q}_1\bar{Q}_0 + SQ_2\bar{Q}_1Q_0 + \bar{S}\bar{Q}_2Q_1\bar{Q}_0 + S\bar{Q}_2Q_1Q_0$ (0.5 point)

6. Design a schematic for the counter using D flip-flops triggered on the falling edge of the clock and the necessary logic gates. (1.5 points)



Exercise 4 : (06 points)

A warehouse manager wants to implement a system to control 3 automatic doors (P1, P2, P3) based on the state of 4 sensors (C1, C2, C3, C4) located at strategic points in the warehouse.

- Each sensor Ci has two possible states (0: The sensor does not detect an object. 1: The sensor detects an object).
- Each door Pi has two possible states (0: The door remains closed. 1: The door opens).

The operating conditions for the doors are defined as follows:

a) Door P1 opens only if at least three sensors detect an object (i.e., their states are 1).
b) Door P2 opens only if sensors C1 and C4 detect an object (state 1), while sensors C2 and C3 do not detect anything (state 0).
c) Door P3 remains closed unless:

   - All sensors detect an object (all states 1), OR
   - C1 and C3 detect an object (state 1) while C2 and C4 do not detect anything (state 0).

1. Identify the input variables and the output variables, and complete the truth table for the system. (1.25 points)
2. Write the logical functions corresponding to each door (P1, P2, P3) **in Sum-of-Products (SoP) form.**

Inputs				Outputs		
C_4	C_3	C_2	C_1	P_3	P_2	P_1
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	1	0	0
0	1	1	0	0	0	0
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	0	1	0	1	0
1	0	1	0	0	0	0
1	0	1	1	0	0	1
1	1	0	0	0	0	0
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	1	0	1

$P_1 = \sum(7, 11, 13, 14, 15)$ (0.25 point)

$= \overline{C}_4C_3\,C_2C_1 + C_4\overline{C}_3\,C_2C_1 + C_4C_3\,\overline{C}_2C_1 + C_4C_3\,C_2\overline{C}_1 + C_4C_3\,C_2C_1$

$P_2 = \sum(9)$ (0.25 point)

$= C_4\overline{C}_3\,\overline{C}_2C_1$

$P_3 = \sum(5, 15)$ (0.25 point)

$= \overline{C}_4C_3\,\overline{C}_2C_1 + C_4C_3\,C_2C_1$

3. Simplify the obtained functions using Karnaugh maps.

C_4C_3 \ C_2C_1	00	01	11	10
00				
01			1	
11		1	1	1
10			1	

$P1 = C_4C_3\,C_1 + C_4C_3\,C_2 + C_3\,C_2C_1 + C_4C_2C_1$ (0.5 point)

C_4C_3 \ C_2C_1	00	01	11	10
00				
01				
11				
10		1		

$P2 = C_4\overline{C}_3\,\overline{C}_2C_1$ (0.25 point)

C_4C_3 \ C_2C_1	00	01	11	10
00				
01		1		
11			1	
10				

$P3 = \overline{C}_4C_3\,\overline{C}_2C_1 + C_4C_3\,C_2C_1$ (0.5 point)

Surname : ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ **First Name :** ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░

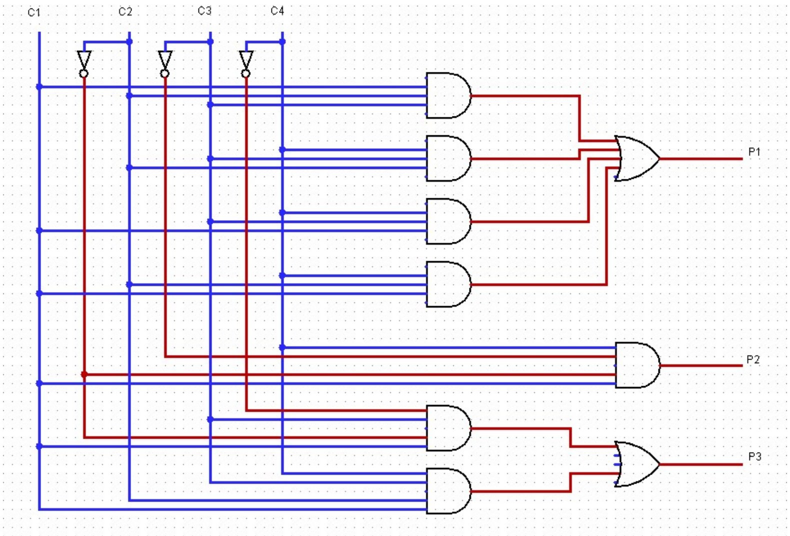
N° Student Card : ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ **Date :** ░ ░ / ░ ░ / ░ ░ ░ ░

Section : ░ ░ ░ ░ **Group :** ░ ░

Module : ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ ░ **Academic Year :** ░░░ ░ / ░ ░ ░ ░

CODE : Reserved for administration

4. Draw the logic circuit diagram representing the system using logical gates. (1.5 points)



5. Design the functionality of the circuit for each door P1, P2, P3 using a multiplexer. Specify the size of the multiplexer required for each output and explain how the inputs of the multiplexer should be configured based on the truth table. (1.25 points)