CS223 Laboratory Assignment 2

Multiplexers and Decoders

Lab dates and times:
Section 1: Monday 08:40-12:30
Section 2: Wednesday 08:40-12:30
Section 3 Tuesday 08:40-12:30
Section 4 Thursday 08:40-12:30

Location: EA Z04 (in the EA building, straight ahead past the elevators).
Groups: Each student will do the lab individually. Group size = 1

Preliminary Design Work (30 points)

Today's lab needs considerable advance preparation. You need to learn how to work with Xilinx's design tool set before attending the lab. Besides, schematics and SystemVerilog models should be prepared in advance, and assembled neatly into a Preliminary Report with a printed cover page and printed pages for the schematics and SystemVerilog codes. Each page should have a proper heading. The content of the report is as follows:

a) A cover page which includes the following: course name and code number, the number of the lab, your name and student ID, date, number of your trainer pack.
b) You need to draw the circuit of the following logic function using only a 2-to-4 Decoder (74HC139) and 2-input AND Gates (No inverter).

   $F(x,y) = \sum m(0,3)$

   Additionally, all IC pin numbers have to be specified clearly on gate pins (refer again to Circuit_schematic_versus_Logic_Diagram.doc). Try to use minimum number of ICs to make your circuit.
c) Design and draw the logic diagram for a 4-to-1 MUX, giving appropriate names to the data inputs, select inputs and output. You need to use only 2-to-4 line Decoder (74HC139) , 2-input OR Gates, 2-input AND Gates and Inverter Gates. Additionally, all IC pin numbers have to be specified clearly on gate pins (refer again to Circuit_schematic_versus_Logic_Diagram.doc). Try to use minimum number of ICs to make your circuit.
d) Now you need to realize the following function using the multiplexer you designed. Use only a single multiplexer, plus at most a single inverter:

   $F(x,y,z) = \sum m(1,3,4,5)$

e) Write the System Verilog module for part (b) in dataflow style code.

Additional pre-lab work:

You should study the following documents (available on Unilica) to be familiar with steps of design flow (simulation, synthesis, implementation, generation of programming file, downloading to FPGA board), using Xilinx Vivado tool. You can download, install and practice working with Xilinx Vivado on your own computer with free webpack license.

- Suggestions for Lab Success with SystemVerilog, Vivado, and BASYS3.
- Basys3 Vivado Decoder Tutorial.
- Vivado Tutorial.
- BASYS-3 FPGA Board Reference Manual (just take a look, and later use it as reference when needed).

You will need a copy of your designs and SystemVerilog programs with you in the lab to refer to or possibly correct and change it. The Preliminary Report will be turned in at the start of lab. Therefore, you must make a photocopy of it before you come to the lab, for your own use.

Part 1: Building a function using 2-to-4 Decoder (20 points)

Using the IC gate package 74HC139 available in the lab, build the function that you have designed in Preliminary Work (b). Connect inputs to switches, and the outputs to LEDs. Test and debug it, until the output gives the correct result. When you are convinced that your circuit works correctly, show it to your TA. Then you and your TA can check it quickly. Be prepared to answer questions that you may be asked.

Part 2: Building 4-to-1 MUX from IC gates (20 points)

Using the IC gate packages 74HC139 and gates available in the lab, build the 4-to-1 MUX that you have designed in Preliminary work part (c). Connect inputs to switches, and the output to a LED. Test and debug it, until the output gives the correct result. When you are convinced that your circuit works correctly, show it to your TA. Implement the F(x,y,z) in Preliminary work part (d) using your multiplexer and test it. Show it to your TA. Be prepared to answer questions that you may be asked.

Part 3: 2-to-4 Decoder on the FPGA (30 points)

In Vivado, show a System Verilog description of your 2-to-4 decoder to the TA or Tutor.
Create an .xdc file with Constraints, like in the tutorials found on **Unilica in Documents > Resources > BASYS3 board and Vivado**, in which you set the inputs and output of your decoder design to the locations on the BASYS3 board (actually, to the pins of the FPGA) that you want them connected to. The file basys3xdc.docx, found in the same Unilica folder, gives a comprehensive listing of all the pins on the FPGA. You will want to connect the 2 inputs to switches, and the 4 outputs to LEDs on the BASYS3 board. Your 2-to-4 decoder is now implemented on the FPGA. Test it with the switches, using the same test vectors as in part 1. When you have the same results, call the TA or Tutor to show your working 2-to-4 decoder.

Submit your code for MOSS similarity testing

Finally, when you are done and before leaving the lab, you need to upload the file *StudentID_SVerilog.txt* created in the Implementation with FPGA part. Be sure that the file contains exactly and only the codes which are specifically detailed above. Don't include the codes which are given to you. If you have multiple files, just copy and paste them in order, one after another inside text file. Check the specifications! Even if you didn't finish, or didn't get the SystemVerilog part working, you must submit your code to the Unilica Assignment for similarity checking. Your codes will be compared against all the other codes in all sections of the class, by the MOSS program, to determine how similar it is (as an indication of plagiarism). So be sure that the code you submit is code that you actually wrote yourself! All students must upload their code to the 'Unilica>Assignment' specific for your section. Check submission time and don't miss it before leaving the lab. After taking a backup of your work, don't forget to delete it from computer. Because students of other sections will work with your system too.

Clean Up!

1. Clean up your lab station, and return all the parts, wires, the Beti trainer board, etc. Leave your lab workstation.
2. CONGRATULATIONS! You are finished with Lab #2 and are one step closer to becoming a computer engineer.

NOTES

- Advance work on this lab, and all labs, is strongly suggested.
- Be sure to read and follow the Policies for CS223 labs, posted in Unilica.

LAB POLICIES

1. There are three computers in each row in the lab. Do not use middle computers, unless you are allowed by lab supervisor.
2. You borrow a Lab-board containing the development board, connectors, etc. in the beginning. The lab supervisor takes your signature. When you are done, return it to her, otherwise you will be responsible and lose points.
3. Each Lab-board has a number. You must always use the same trainer board pack throughout the semester.
4. You must be in the lab, working on the lab, from the time lab starts until you finish and leave. (Bathroom and snack breaks are the exception to this rule). Absence from the lab, at any time, is counted as absence from the whole lab that day.
5. No cell phone usage during lab. Tell friends not to call during the lab hours--you are busy learning how digital circuits work !.
6. Internet usage is permitted only to lab-related technical sites. No Facebook, Twitter, email, news, video games, etc--you are busy learning how digital circuits work !.
7. If you come to lab later than 20 minutes, you will loose that session completely.
8. When you are done, DO NOT return IC parts into the IC boxes, where you've taken them first. Just put them inside your lab pack box. Lab coordinator will check and return them later.