CS223 Laboratory Assignment 6

Delay in Combinational Circuits

Lab dates and times:
Section 1: Monday 08:40-12:30
Section 2: Wednesday 08:40-12:30
Section 3 Tuesday 08:40-12:30
Section 4 Thursday 08:40-12:30

Location: EA Z04 (in the EA building, straight ahead past the elevators)
Groups: Each student will do the lab individually. Group size = 1

Lab Assignment

You will design an experiment to investigate the concept of timing in combinational circuits through simulation. The Vivado simulation tool will be used to compare two different implementations of an ALU unit and compare their timing for different operations.

Preliminary Report (50 points)

All students should be prepared to submit their Preliminary Design Report at the start of their lab section time. You report should contain the following items, each starting at the top of a new page:

a) A cover page which includes the following: course name and code number, the number of the lab, your name and student ID, date, number of your trainer pack.
b) Prepare SystemVerilog code in structural style for the ALU in the textbook, Chapter 5, Table 5.1. Implement all eight operations by the exact circuit you see in Figure 15.5. Each gate or module,will be implemented by TTL 74LS00 family IC's. Find the proper IC code (you can find them here), and by referring to its datasheet from any manufacturer, find and assign a typical delay to that gate or module in your SystemVerilog code. Draw schematic and clearly write the IC code and its delay in nanosecond, on each module or gate.
c) Write SystemVerilog code in behavioral or data-flow style to describe the ALU IC with code 74LS181. You can ignore having all operations and implement only the eight operations you had in part (b). By refereeing to datasheet, assign a single typical propagation delay for whole ALU module.
d) Prepare SystemVerilog code for the circuit in Figure 1, which describes three registers connected to an ALU. Fill R2 and R3 with initial values. R1 should be able to capture the result of ALU operation at the first clock edge after enabling the registers. Prepare a testbench for each ALU to check all expected functionalities from that ALU.

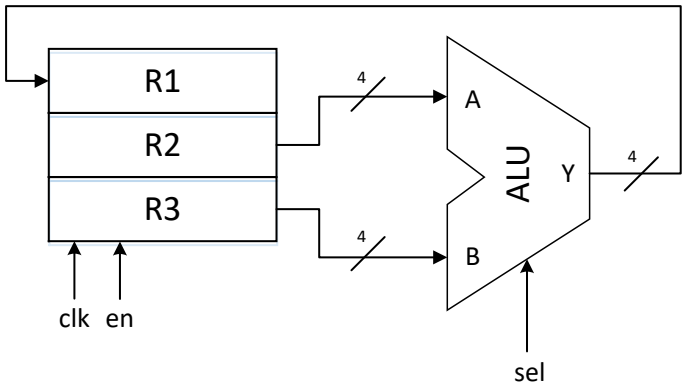

Figure 1

IMPORTANT NOTE: The SystemVerilog modules are code, and as with any program code, they should be well-structured, well-commented, use meaningful identifiers, use white space and indentation as appropriate to facilitate understanding, and in summary, should be self-documenting. If code is difficult to understand, it is not self-documenting! All pages in the report, with the possible exception of a hand-drawn logic diagram, should be printed. You should make a photocopy of the Preliminary Design Report, for you to use during the lab.

Lab Demo (50 points)

You should come to lab fully prepared. You are advised to arrive with the problem above fully implemented and tested and ready to work. In this lab you will not use BASYS-3 board and your work will be evaluated only based on simulation results. Your grade will be based on the followings:

a) In simulation, run the testbench you prepared in preliminary part (d) and confirm all functionalities of ALU in preliminary part (b). You should run simulation in a way that delays of all individual ICs can be distinguishable. For this purpose you can use suitable input values or explicitly assign name to intermediate wires and bring them into signal-lists in simulation window.
b) In simulation, run the testbench you prepared in preliminary part (d) and confirm all functionalities of ALU in preliminary part (c). The IC's delay should be visible in simulation window.
c) For each ALU, find the critical path's delay and maximum allowable clock frequency. After that, in simulation increase the clock rate up to a limit that the circuit stops working properly. Your simulation should show this clearly.
d) Finally, when you are convinced that all parts work correctly, call TA and show the results to the TA. He/she will ask questions to check your knowledge and understanding of the project and SystemVerilog, and you will receive a grade according to your answers.

Submit your code for MOSS similarity testing

Finally, when you are done and before leaving the lab, you need to upload the file *StudentID_SVerilog.txt* created in the Implementation with FPGA part. Be sure that the file contains exactly and only the codes which are specifically detailed above. Don't include the

codes which are given to you. If you have multiple files, just copy and paste them in order, one after another inside text file. Check the specifications! Even if you didn't finish, or didn't get the SystemVerilog part working, you must submit your code to the Unilica Assignment for similarity checking. Your codes will be compared against all the other codes in all sections of the class, by the MOSS program, to determine how similar it is (as an indication of plagiarism). So be sure that the code you submit is code that you actually wrote yourself! All students must upload their code to the 'Unilica>Assignment' specific for your section. Check submission time and don't miss it before leaving the lab. After taking a backup of your work, don't forget to delete it from computer. Because students of other sections will work with your system too.

Clean Up!

1) Clean up your lab station, and return all the parts, wires, the Beti trainer board, etc. Leave your lab workstation.

2) CONGRATULATIONS! You are finished with this lab and are one step closer to becoming a computer engineer.

NOTES

--Advance work on this lab, and all labs, is strongly suggested.

--Be sure to read and follow the Policies for CS223 labs, posted in Unilica.

LAB POLICIES

1. There are three computers in each row in the lab. Don't use middle computers, unless you are allowed by lab supervisor.
2. You borrow a Lab-board containing the development board, connectors, etc. in the beginning. The lab supervisor takes your signature. When you are done, return it to her, otherwise you will be responsible and lose points.
3. Each Lab-board has a number. You must always use the same trainer board pack throughout the semester.
4. You must be in the lab, working on the lab, from the time lab starts until you finish and leave. (Bathroom and snack breaks are the exception to this rule). Absence from the lab, at any time, is counted as absence from the whole lab that day.
5. No cell phone usage during lab. Tell friends not to call during the lab hours--you are busy learning how digital circuits work !.
6. Internet usage is permitted only to lab-related technical sites. No Facebook, Twitter, email, news, video games, etc--you are busy learning how digital circuits work !.
7. If you come to lab later than 20 minutes, you will lose that session completely.
8. When you are done, DO NOT return IC parts into the IC boxes, where you've taken them first. Just put them inside your lab pack box. Lab coordinator will check and return them later.