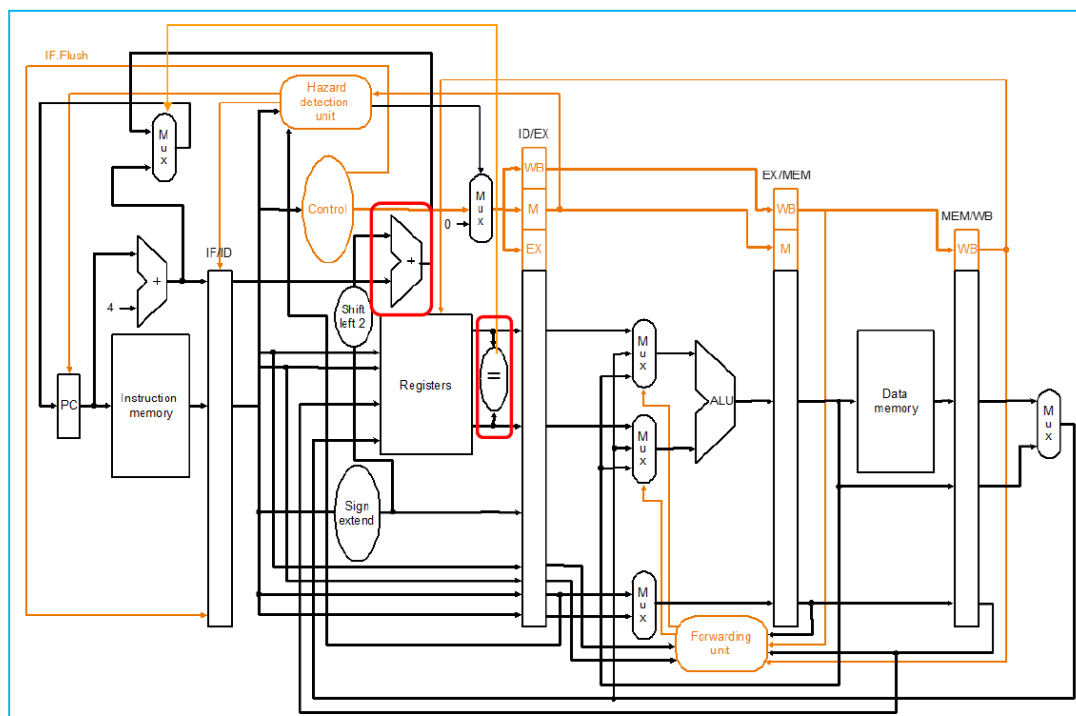
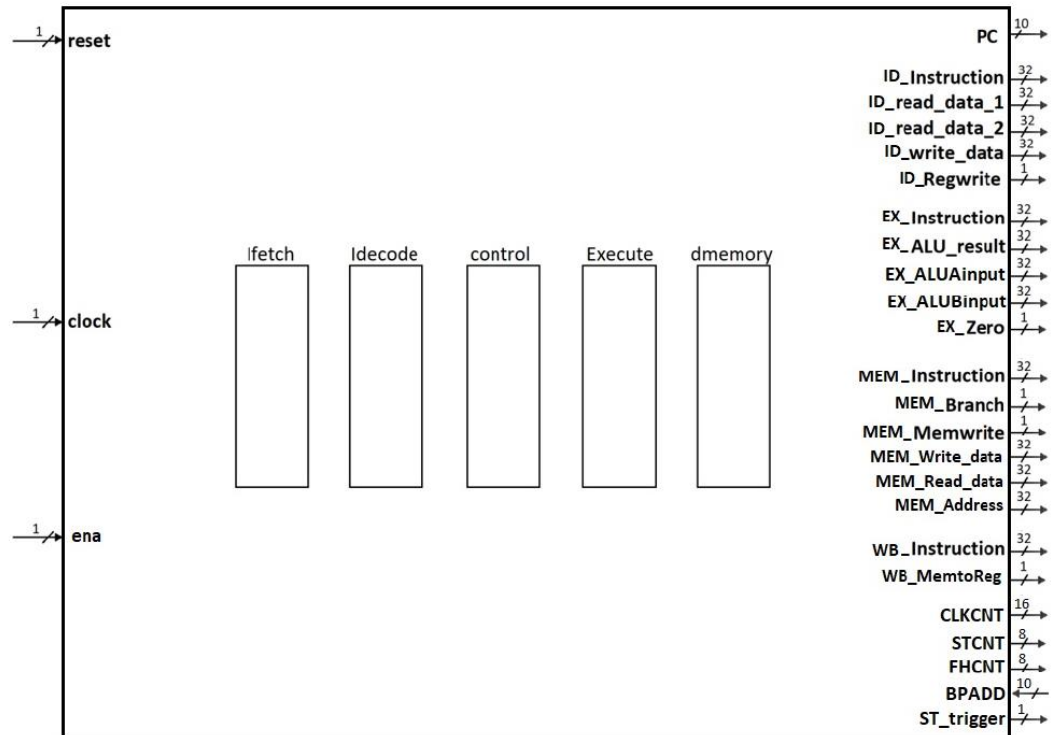
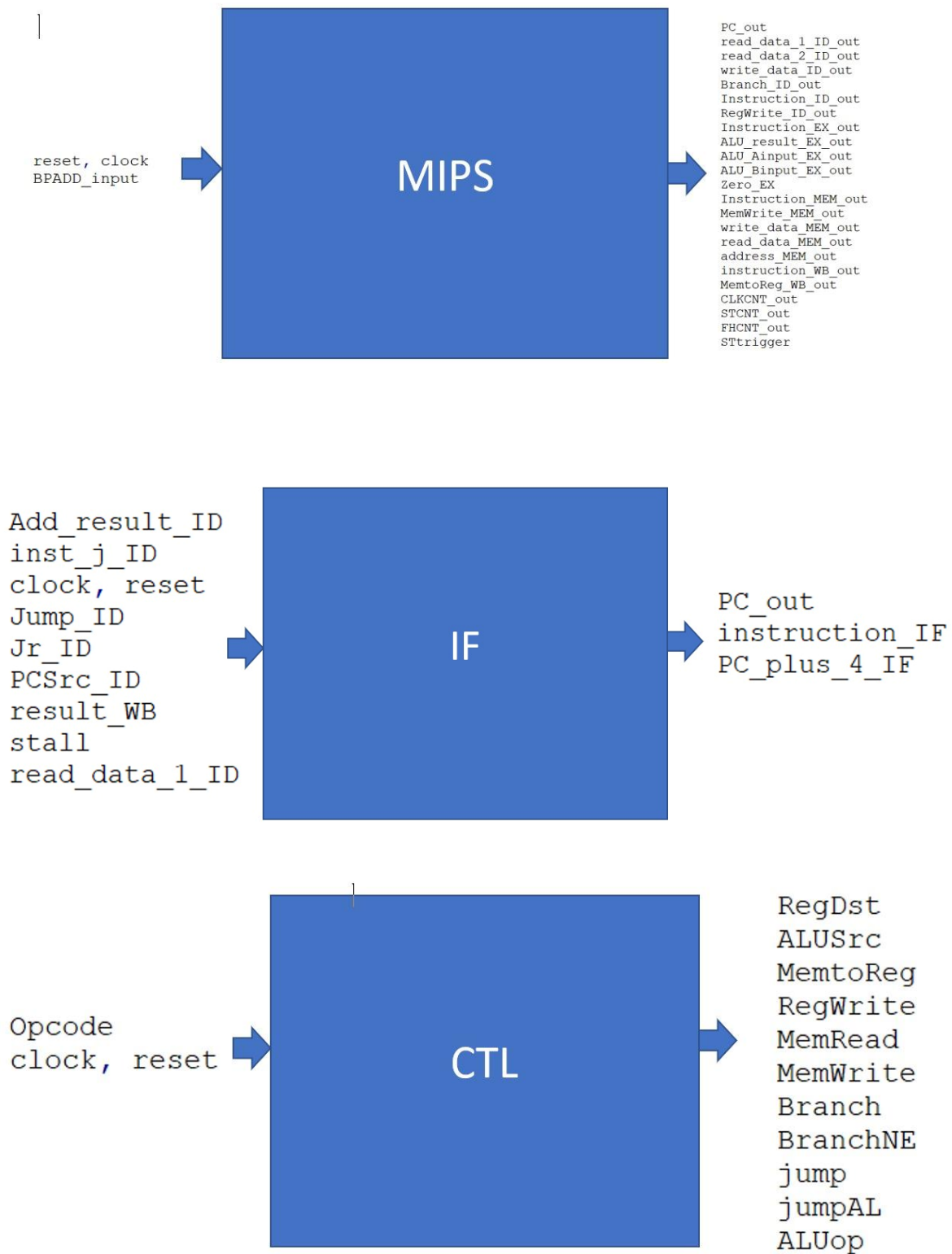


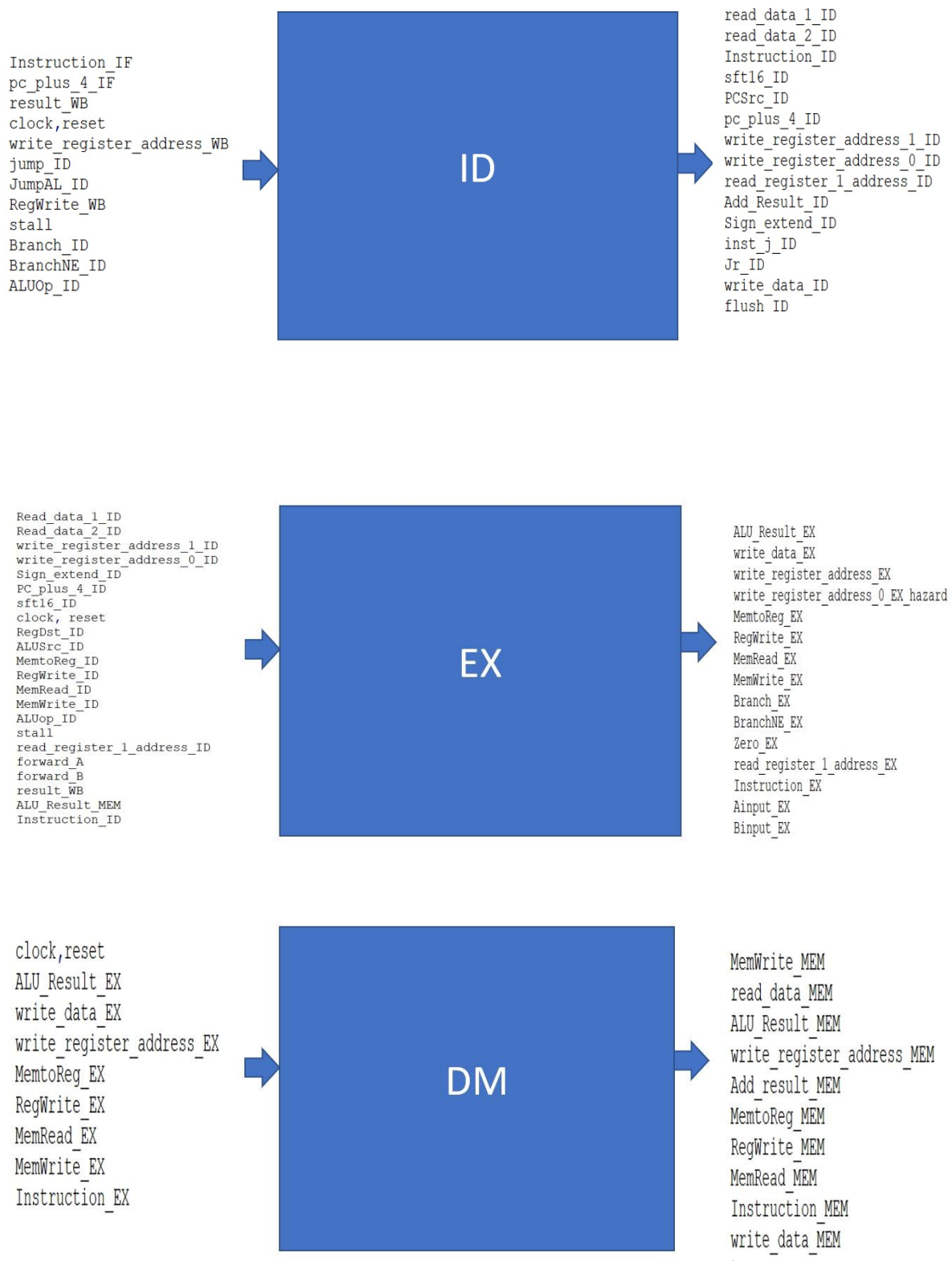
ניסוי 5:

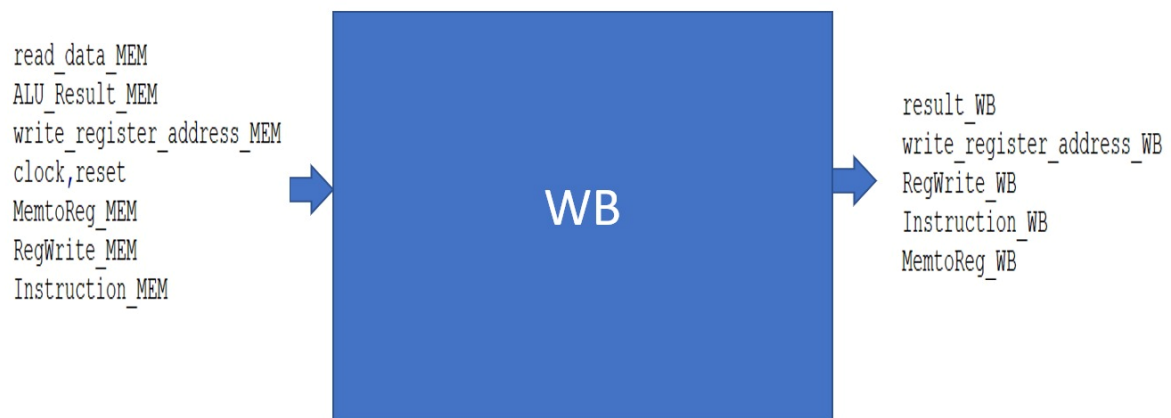
בניסוי זה מימשנו מעבד MIPS pipelined עם יחידת stall ו- forward, וכן יחידת hazard המבצעת flush.



לפנינו פירוט של כל בלוק:







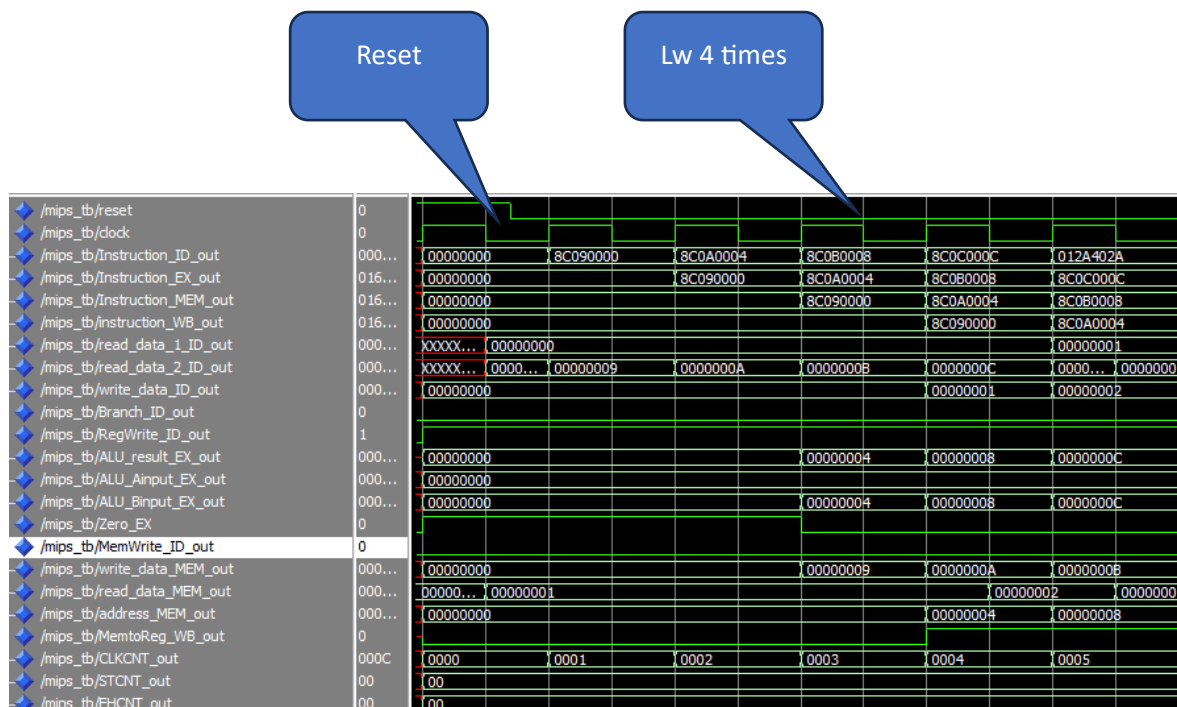
שלוש בן-יאיר 308374529
קרן מזעקי 318501335

לפנינו דוגמת קוד בדיקה שהרצנו, ואחריה תוצאות הtestbench בmodelsim:

```
.data
i: .word 1
j: .word 2
g: .word 3
h: .word 4
f: .word 5

.text
lw $t1, 0
lw $t2, 4
lw $t3, 8
lw $t4, 12
slt $t0, $t1, $t2
sub $t4, $t3, $t2
mul $t4, $t3, $t2
lui $t6, 100
and $t4, $t3, $t2
or $t4, $t3, $t2
xor $t4, $t3, $t2
sll $t4, $t3, 3
srl $t4, $t2, 2
sw $t4, 12
addi $t4, $t3, 5
andi $t4, $t3, 5
ori $t4, $t3, 5

xori $t4, $t3, 5
slti $t4, $t3, 1
TWO: add $t5, $t3, $t4
ONE: jal IF
      j THREE
      add $t5, $t3, $t4
IF:   move $t5, $t3
      jr $ra
THREE: bne $t0, $t1, END
ELSE:  sub $t5, $t3, $t4
END:   sw $t5, f
```



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R format

mul

[illegible]

Signal	Value	Hex Data
/mips_tb/reset	0	
/mips_tb/dclock	1	
/mips_tb/Instruction_ID_out	012...	000B60C0 000A6082 AC0C000C 216C0005 316C0005 356C0005
/mips_tb/Instruction_EX_out	8C0...	016A6026 000B60C0 000A6082 AC0C000C 216C0005 316C0005
/mips_tb/Instruction_MEM_out	8C0...	016A6026 016A6026 000B60C0 000A6082 AC0C000C 216C0005
/mips_tb/Instruction_WB_out	8C0...	016A6024 016A6026 016A6026 000B60C0 000A6082 AC0C000C
/mips_tb/read_data_1_ID_out	000...	00000000 00000000 00000000 00000000 00000000 00000000
/mips_tb/read_data_2_ID_out	000...	00000003 00000002 0000... 00000001 00000018 00000000
/mips_tb/write_data_ID_out	000...	00000002 00000003 00000001 00000018 00000000 0000000C
/mips_tb/Branch_ID_out	0	
/mips_tb/RegWrite_ID_out	1	
/mips_tb/ALU_result_EX_out	000...	00000001 00000018 00000000 0000000C 00000008 00000001
/mips_tb/ALU_Ainput_EX_out	000...	00000003 00000000 00000000 00000000 00000003 00000000
/mips_tb/ALU_Binput_EX_out	000...	00000002 00000003 00000002 0000000C 00000005 00000000
/mips_tb/Zero_EX	0	
/mips_tb/MemWrite_ID_out	0	
/mips_tb/write_data_MEM_out	000...	00000002 00000003 00000002 00000001 00000018 00000000
/mips_tb/read_data_MEM_out	000...	00000001 00000000 00000000 00000001 00000000 00000000
/mips_tb/address_MEM_out	000...	00000003 00000001 00000018 00000000 0000000C 00000008
/mips_tb/MemtoReg_WB_out	1	
/mips_tb/CLKCNT_out	0005	000C 000D 000E 000F 0010 0011
/mips_tb/STCNT_out	00	00
/mips_tb/FHCNT_out	00	00

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	/mips_tb/reset	0																										
	/mips_tb/dock	1																										
+		/mips_tb/Instruction_ID_out	012...	396C0005	296C0001	016C6820	0C000C17	00000000	000B6821																			
+		/mips_tb/Instruction_EX_out	8C0...	356C0005	396C0005	296C0001	016C6820	0C000C17	00000000																			
+		/mips_tb/Instruction_MEM_out	8C0...	316C0005	356C0005	396C0005	296C0001	016C6820	0C000C17																			
+		/mips_tb/Instruction_WB_out	8C0...	216C0005	316C0005	356C0005	396C0005	296C0001	016C6820																			
+		/mips_tb/read_data_1_ID_out	000...	00000003				00000000																				
+		/mips_tb/read_data_2_ID_out	000...	00000000	00000008	00000001	0000...	00000000	00000003																			
+		/mips_tb/write_data_ID_out	000...	00000008	00000001	00000007	00000015	00000000	00000003																			
	/mips_tb/Branch_ID_out	0																										
	/mips_tb/RegWrite_ID_out	1																										
+		/mips_tb/ALU_result_EX_out	000...	00000007	00000006	00000000	00000003	00000000																				
+		/mips_tb/ALU_Ainput_EX_out	000...	00000003				00000000																				
+		/mips_tb/ALU_Binput_EX_out	000...	00000005		00000001	00000000																					
	/mips_tb/Zero_EX	0																										
	/mips_tb/MemWrite_ID_out	0																										
+		/mips_tb/write_data_MEM_out	000...	00000000		00000008	00000001	00000007	00000000																			
+		/mips_tb/read_data_MEM_out	000...	00000003	00000001	00000002		00000001																				
+		/mips_tb/address_MEM_out	000...	00000001	00000007	00000006	00000000	00000003	00000000																			
	/mips_tb/MemtoReg_WB_out	1																										
+		/mips_tb/CLKCNT_out	0005	0012	0013	0014	0015	0016	0017																			
+		/mips_tb/STCNT_out	00	00																								
+		/mips_tb/FHCNT_out	00	00				01																				

וכן הלאה...

כעת צרבנו את הקוד לבקר באמצעות quartus.

לפנינו תמונה מהה-Signal-Tap קוד אסמבלי שהרצנו במidelsim:

[illegible]

שולם בן-יאיר 308374529
קרן מזעקי 318501335

Name	208 Value	0	1	2	3	4	5	6	7	8	9
reset	0										
PC_out[9..0]	378h	03Ch	040h	044h	048h	04Ch	050h	054h	05Ch	060h	064h
Instruction_ID_out[31..0]	00000000h	216C0005h	316C0005h	356C0005h	396C0005h	296C0001h	016C6820h	0C000C17h	00000000h	000B6821h	03E00008h
read_data_1_ID_out[31..0]	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h
read_data_2_ID_out[31..0]	00000000h	00000018h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h
write_data_ID_out[31..0]	00000000h	00000018h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h
RegWrite_ID_out	1										
Branch_ID_out	0										
Instruction_EX_out[31..0]	00000000h	AC0C000Ch	216C0005h	316C0005h	356C0005h	396C0005h	296C0001h	016C6820h	0C000C17h	00000000h	000B6821h
ALU_result_EX_out[31..0]	00000000h	0000000Ch	00000000h	00000001h	00000007h	00000006h	00000000h	00000003h	00000000h	00000003h	00000001h
ALU_Ainput_EX_out[31..0]	00000000h	00000000h	00000000h	00000000h	00000003h	00000000h	00000000h	00000003h	00000000h	00000000h	00000001h
ALU_Binput_EX_out[31..0]	00000000h	0000000Ch	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h
Zero_EX	1										
Instruction_MEM_out[31..0]	00000000h	000A6082h	AC0C000Ch	216C0005h	316C0005h	356C0005h	396C0005h	296C0001h	016C6820h	0C000C17h	00000000h
MemWrite_MEM_out	0										
write_data_MEM_out[31..0]	00000000h	00000002h	00000001h	00000018h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h
read_data_MEM_out[31..0]	00000001h	00000001h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h	00000000h
address_MEM_out[31..0]	00000000h	00000000h	0000000Ch	00000000h	00000001h	00000007h	00000000h	00000000h	00000003h	00000000h	00000000h
instruction_WB_out[31..0]	00000000h	000B60C0h	000A6082h	AC0C000Ch	216C0005h	316C0005h	356C0005h	396C0005h	296C0001h	016C6820h	0C000C17h
MemtoReg_WB_out	0										
CLKCNT_out[15..0]	0000h	0000h	0010h	0011h	0012h	0013h	0014h	0015h	0016h	0017h	0018h
STCNT_out[7..0]	00h										
FHCNT_out[7..0]	04h										
BPADD_input[7..0]	10h										
STtrigger	0										

המערך של Fmax:

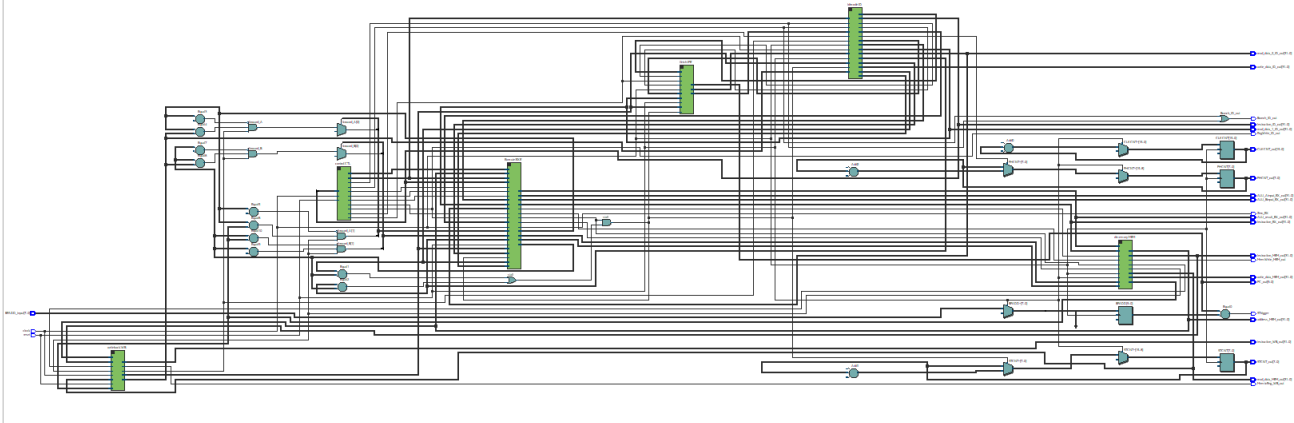
	Fmax	Restricted Fmax	Clock Name	Note
1	37.59 MHz	37.59 MHz	clock	
2	65.17 MHz	65.17 MHz	altera_reserved_tck	

logic usage report-וה:

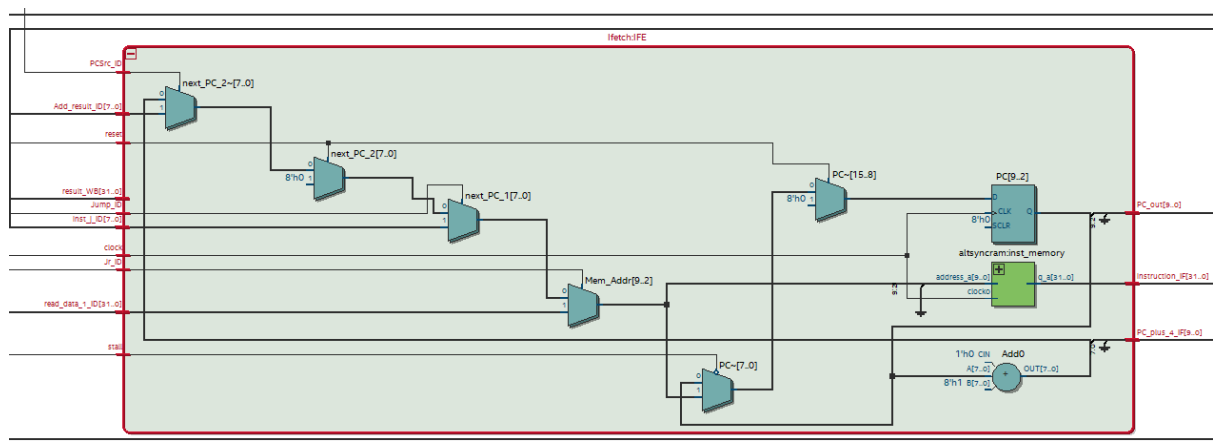
Analysis & Synthesis Resource Utilization by Entity						
<<Filter>>						
	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Pins	Memory Blocks	Virtual Pins
1	MIPS	2707 (58)	8005 (40)	10	...	2 464
1	Execute:EXE	566 (451)	105 (105)	0	0	2 0
2	Decode:ID	847 (847)	1032 (1032)	0	0	0 0
3	Fetch:IFE	51 (51)	8 (8)	0	...	0 0
4	Control:CTL	15 (15)	0 (0)	0	0	0 0
5	Memory:MEM	5 (5)	104 (104)	0	...	0 0
6	Hub:auto_hub	91 (1)	90 (0)	0	0	0 0
7	SignalTap:auto_signaltap_0	1042 (2)	6523 (946)	0	...	0 0
8	Writeback:WB	32 (32)	103 (103)	0	0	0 0

נוסחל על RTL viewer של כל רכיב:

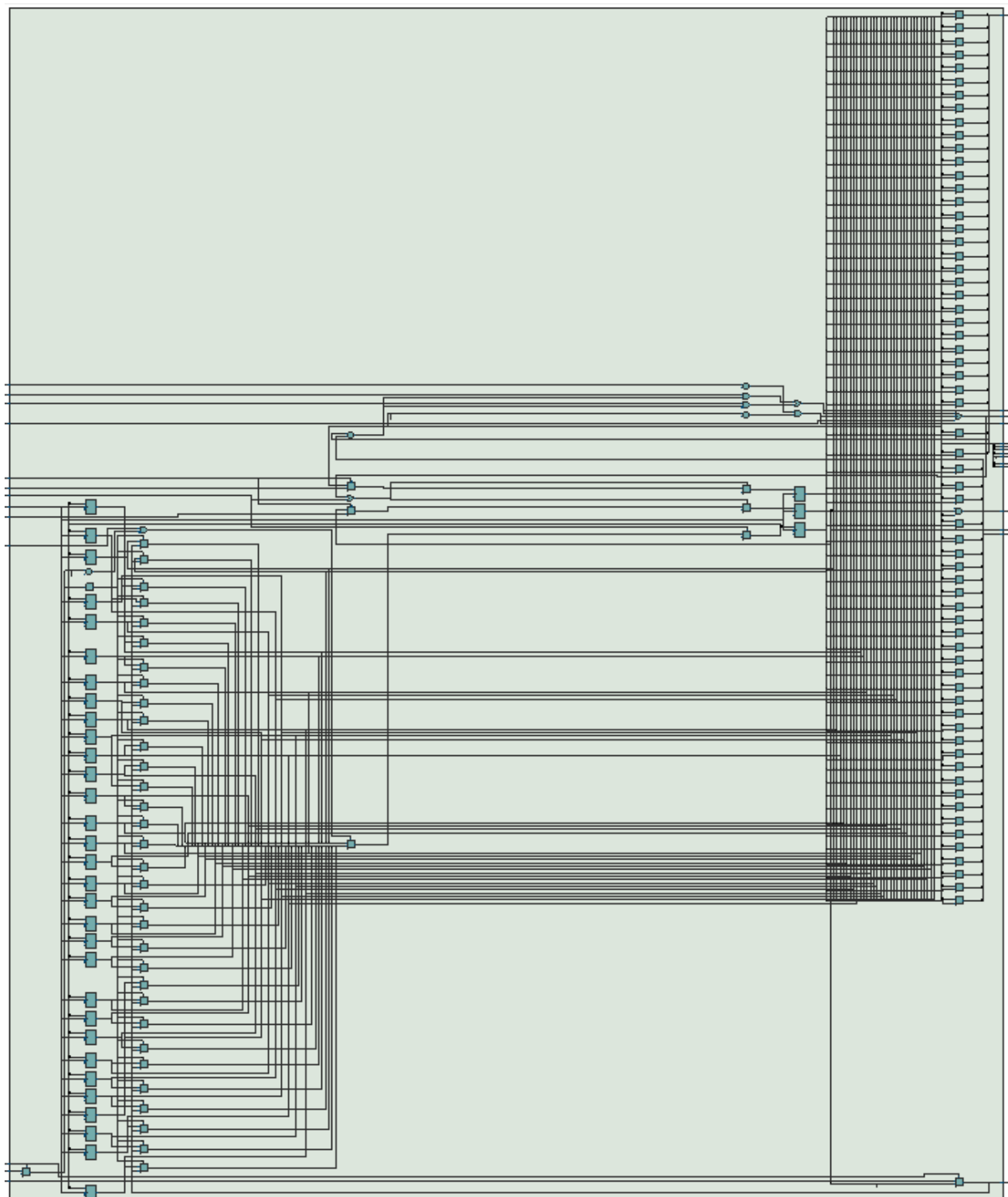
MIPS:



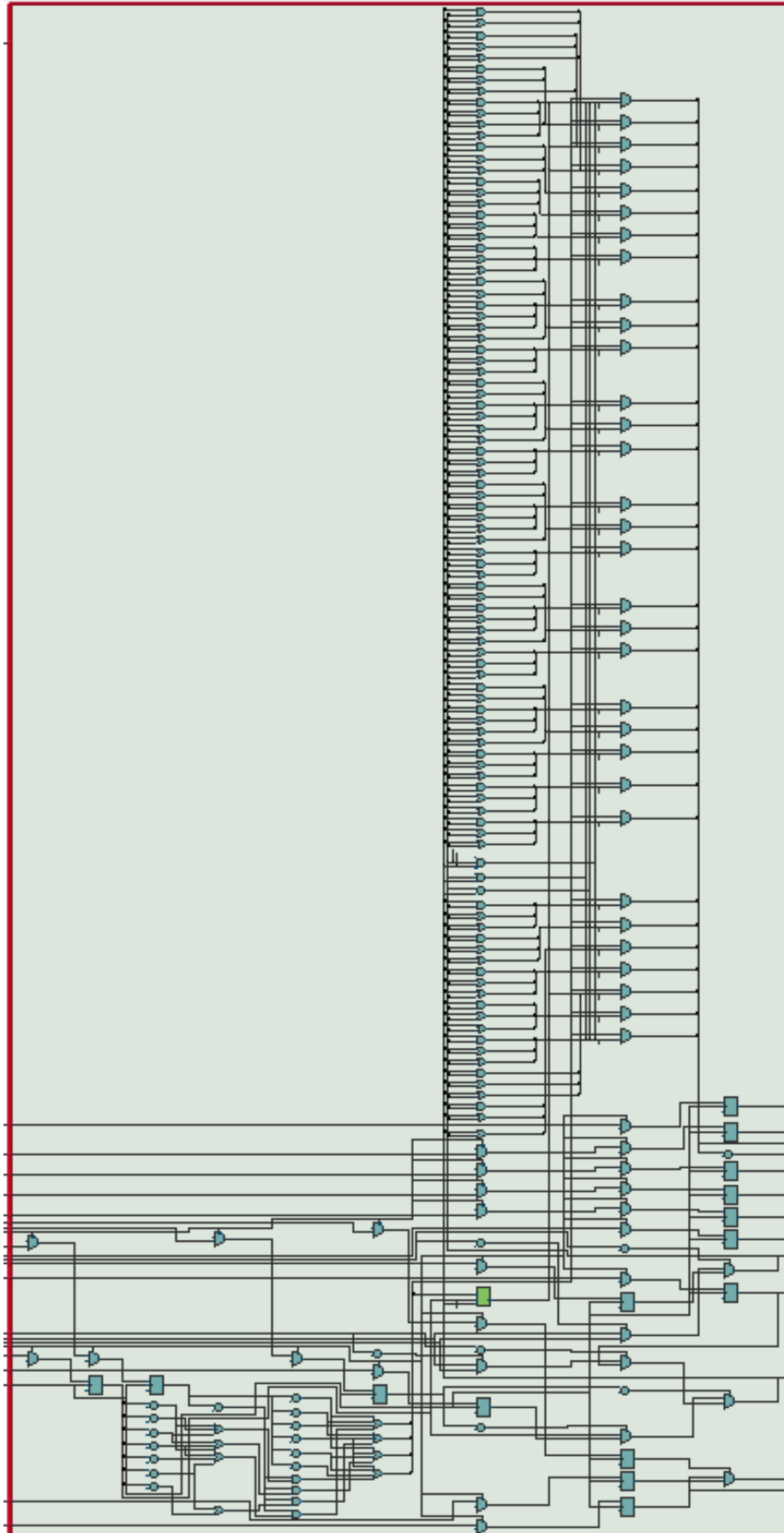
:IFETCH



:IDECODE

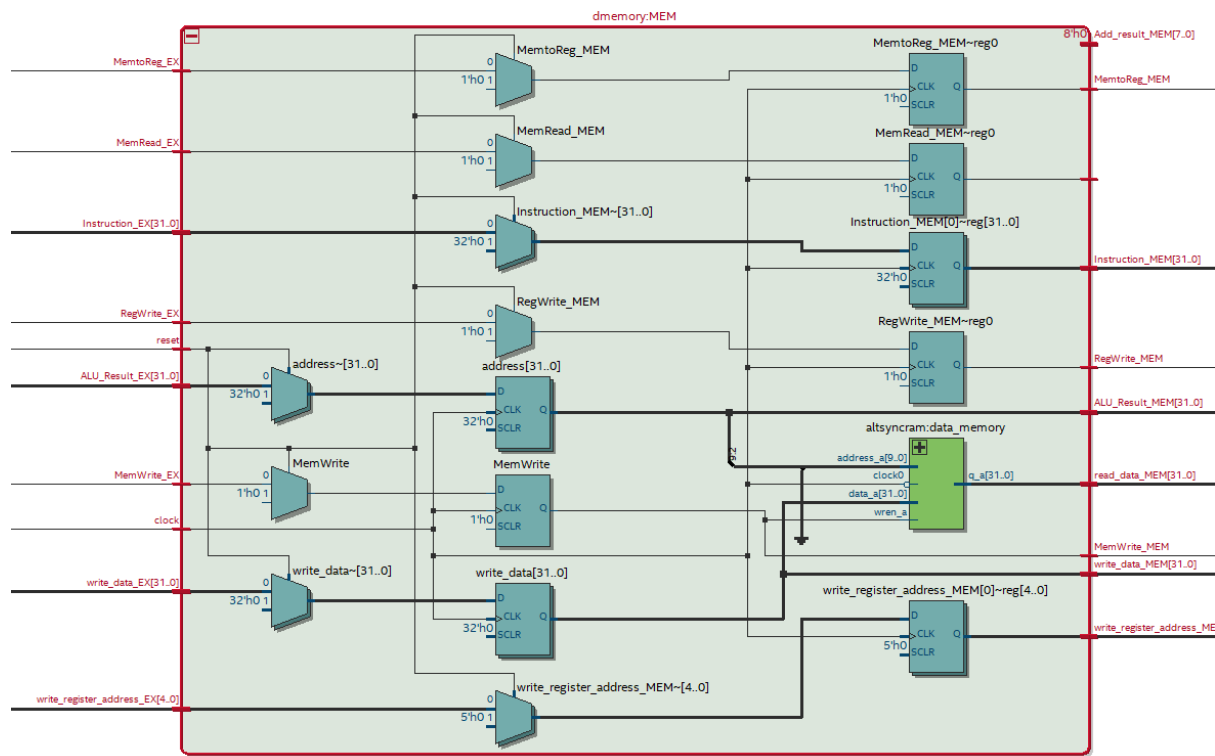


:EXECUTE

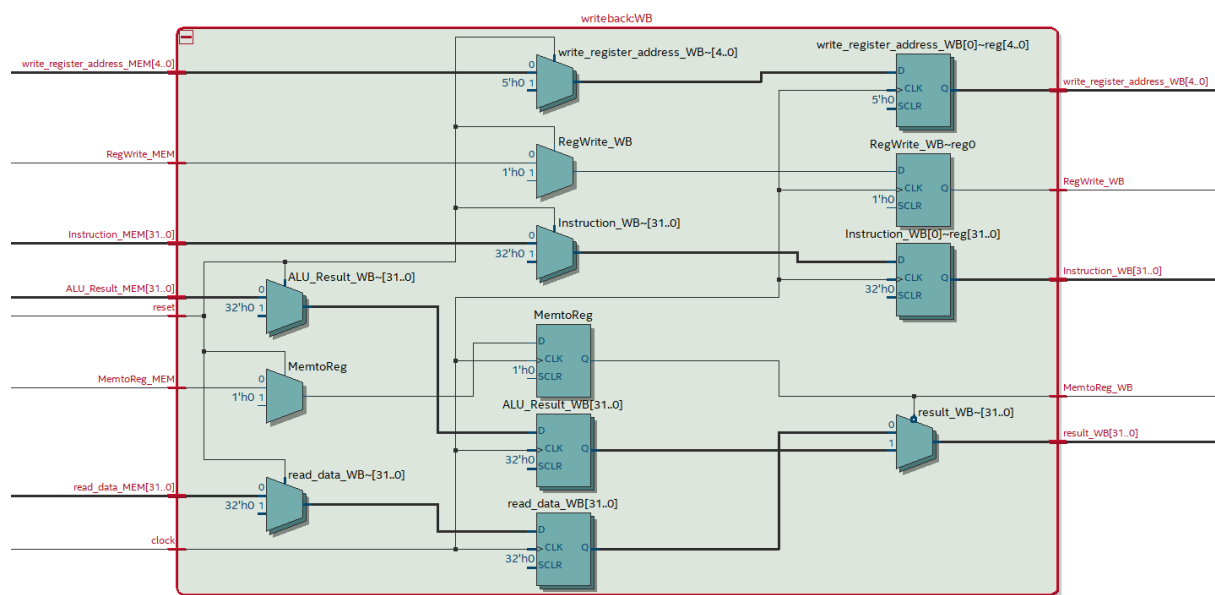


:DMEMORY

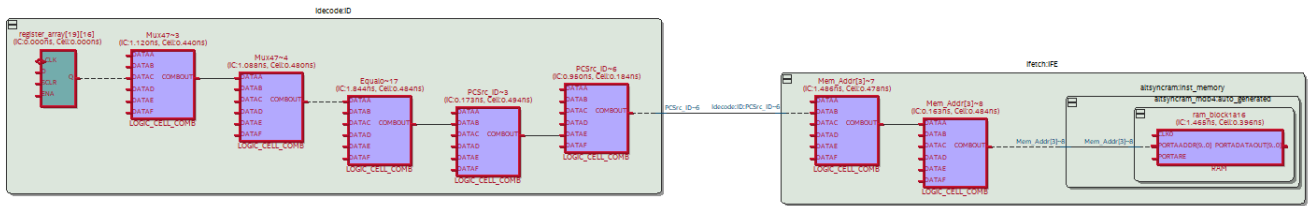
שולם בן-יאיר 308374529
קרן מזעקי 318501335



:WRITEBACK

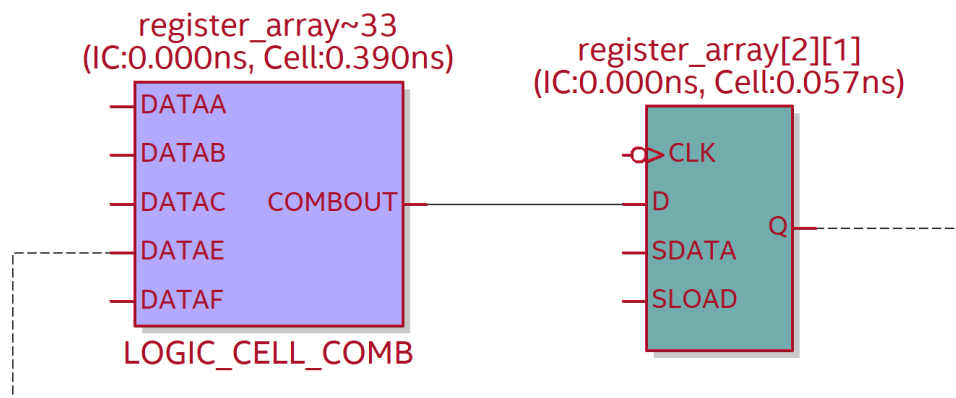


כעת נבחן את המסלול הקריטי:



כפי שניתן לראות, המסלול הקריטי הוא המסלול המבצע פעולה עם הזיכרון (lw או sw). הדבר הגיוני מכיוון שפעולה זו עוברת בכל שכבות המעבד ונכנסת לזיכרון RAM ולכן היא הארוכה ביותר.

המסלול הקצר ביותר:

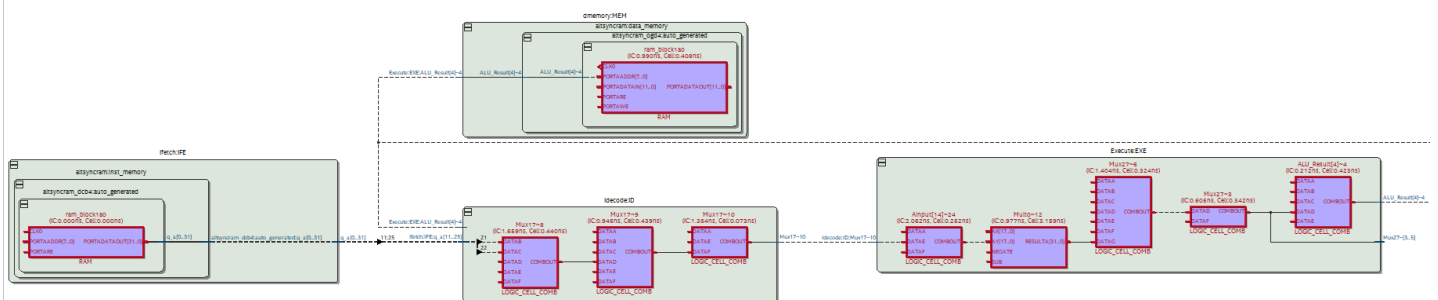


נבחן גם את המסלול הקריטי במעבד single cyclen:

ה-fmax הוא:

	Fmax	Restricted Fmax	Clock Name	Note
1	29.19 MHz	29.19 MHz	clock	
2	58.94 MHz	58.94 MHz	altera...ed_tck	

המסלול הקריטי הוא:



גם כאן זהו המסלול הנכנס לזיכרון, וככל הנראה קשור לפקודת sw או לפקודת sa.