INSTRUCTION	OPCODE (5 bits)					OPERANDS (13 bits)												
						12	11	10	9	8	7	6	5	4	3	2	1	0
ADD	0	0	0	0	0	DST				SRC1				SRC2				0
SUB	0	0	0	0	1	DST				SRC1				SRC2				0
NAND	0	0	0	1	0	DST				SRC1				SRC2				0
NOR	0	0	0	1	1	DST				SRC1				SRC2				0
SRL	0	0	1	0	0	DST				SRC1				SRC2				0
SRA	0	0	1	0	1	DST				SRC1				SRC2				0
ADDI	0	0	1	1	0	DST				SRC1				IMM5				
SUBI	0	0	1	1	1	DST				SRC1				IMM5				
NANDI	0	1	0	0	0	DST				SRC1				IMM5				
NORI	0	1	0	0	1	DST				SRC1				IMM5				
LD	0	1	0	1	0	DST				ADDR9								
ST	0	1	0	1	1	DST				ADDR9								
JUMP	0	1	1	0	0	PCoffset13												
JAL	0	1	1	0	1	PCoffset13												
LUI	0	1	1	1	0	DST				IMM9								
CMOV	0	1	1	1	1	REG1				REG2				REG3				0
PUSH	1	0	0	0	0	SRC1				0								
POP	1	0	0	0	1	SRC1				0								

Register	Address			
R1	0	0	0	0
R2	0	0	0	1
R3	0	0	1	0
R4	0	0	1	1
R5	0	1	0	0
R6	0	1	0	1
R7	0	1	1	0
R8	0	1	1	1
R9	1	0	0	0
R10	1	0	0	1
R11	1	0	1	0
R12	1	0	1	1
R13	1	1	0	0
R14	1	1	0	1
R15	1	1	1	0
R16	1	1	1	1