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Synthesis home assignment 2

Script:

```
set design top

set_app_var search_path
"/home/standard_cell_libraries/NangateOpenCellLibrary_PDKv1_3_v2010_12/lib/Front_End/Liberty/NLDM"


set_app_var link_library "NangateOpenCellLibrary_ff1p25v0c.db
NangateOpenCellLibrary_ss0p95v125c.db"


set_app_var target_library "NangateOpenCellLibrary_ff1p25v0c.db
NangateOpenCellLibrary_ss0p95v125c.db"


sh rm -rf work

sh mkdir -p work

define_design_lib work -path ./work
```

```
analyze -library work -format verilog ./$design.v

elaborate $design -lib work

current_design



source ./cons.tcl

link

check_design


compile -map_effort medium


report_area  -hierarchy >
/home/ahesham/Desktop/ITI_PHASE1/RISCV_kero/report/synth_area.rpt

report_cell > /home/ahesham/Desktop/ITI_PHASE1/RISCV_kero/report/synth_cells.rpt

report_qor  > /home/ahesham/Desktop/ITI_PHASE1/RISCV_kero/report/synth_qor.rpt

report_resources >
/home/ahesham/Desktop/ITI_PHASE1/RISCV_kero/report/synth_resources.rpt

report_timing -max_paths 10 >
/home/ahesham/Desktop/ITI_PHASE1/RISCV_kero/report/synth_timing_setup.rpt

report_timing -delay_type min -max_paths 10 >
/home/ahesham/Desktop/ITI_PHASE1/RISCV_kero/report/synth_timing_hold.rpt


write_sdc  output/${design}.sdc


define_name_rules  no_case -case_insensitive

change_names -rule no_case -hierarchy

change_names -rule verilog -hierarchy

set verilogout_no_tri      true

set verilogout_equation  false
```

```
write -hierarchy -format verilog -output output/${design}.v

write_sdf -version 2.1 output/${design}.sdf

write -f ddc -hierarchy -output output/${design}.ddc


exit
```

Constraints:

```
create_clock -name clk -period 6 [get_ports clk]

set_clock_uncertainty -setup 0.35 [get_clocks clk]

set_driving_cell -lib_cell BUF_X4 [remove_from_collection][all_inputs][get_ports clk]

set_input_delay -max 3 -clock [get_clocks clk] [remove_from_collection] [all_inputs] [get_ports clk]

set_output_delay -max 3 -clock [get_clocks clk] [all_outputs]

set_load -max 120 [all_outputs]

set_max_fanout 4 {rst}

set_max_fanout 4 {instr}

set_dont_use {NangateOpenCellLibrary_ff1p25v0c/DFFR_X1*}

set_max_area 10000
```

Timing report:

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 10
Design : top
Version: G-2012.06-SP2
Date   : Mon Oct  8 05:51:59 2018
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: fast   Library: NangateOpenCellLibrary_ff1p25v0c
Wire Load Model Mode: top

  Startpoint: D_Path/reg_file_inst/register_reg_25__0_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: aluresult[31]
            (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  top                5K_hvratio_1_1        NangateOpenCellLibrary_ff1p25v0c

  Point                                    Incr       Path
```

---

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

D_Path/reg_file_inst/register_reg_25__0_/CK (DFFR_X2)

0.00 # 0.00 r

D_Path/reg_file_inst/register_reg_25__0_/Q (DFFR_X2)

0.06 0.06 f

D_Path/reg_file_inst/U2838/ZN (AOI22_X1) 0.03 0.09 r

D_Path/reg_file_inst/U54/ZN (NAND3_X1) 0.03 0.12 f

D_Path/reg_file_inst/U520/ZN (NOR4_X1) 0.05 0.17 r

D_Path/reg_file_inst/U519/ZN (NAND2_X1) 0.02 0.20 f

D_Path/reg_file_inst/RD2[0] (regfile_32_bits) 0.00 0.20 f

D_Path/mux2_1_inst/in1[0] (mux2_1) 0.00 0.20 f

D_Path/mux2_1_inst/U2/Z (MUX2_X1) 0.04 0.24 f

D_Path/mux2_1_inst/out[0] (mux2_1) 0.00 0.24 f

D_Path/ALU_inst/data2[0] (ALU) 0.00 0.24 f

D_Path/ALU_inst/add_8/B[0] (ALU_DW01_add_0) 0.00 0.24 f

D_Path/ALU_inst/add_8/U13/ZN (AND2_X1) 0.03 0.27 f

D_Path/ALU_inst/add_8/U1_1/CO (FA_X1) 0.06 0.33 f

D_Path/ALU_inst/add_8/U1_2/CO (FA_X1) 0.06 0.38 f

D_Path/ALU_inst/add_8/U1_3/CO (FA_X1) 0.06 0.44 f

D_Path/ALU_inst/add_8/U1_4/CO (FA_X1) 0.06 0.50 f

D_Path/ALU_inst/add_8/U1_5/CO (FA_X1) 0.06 0.56 f

D_Path/ALU_inst/add_8/U1_6/CO (FA_X1) 0.06 0.61 f

D_Path/ALU_inst/add_8/U1_7/CO (FA_X1) 0.06 0.67 f

D_Path/ALU_inst/add_8/U1_8/CO (FA_X1) 0.06 0.73 f

D_Path/ALU_inst/add_8/U1_9/CO (FA_X1) 0.06 0.79 f

D_Path/ALU_inst/add_8/U1_10/CO (FA_X1) 0.06 0.85 f

D_Path/ALU_inst/add_8/U1_11/CO (FA_X1) 0.06 0.90 f

D_Path/ALU_inst/add_8/U1_12/CO (FA_X1) 0.06 0.96 f

D_Path/ALU_inst/add_8/U1_13/CO (FA_X1) 0.06 1.02 f

D_Path/ALU_inst/add_8/U1_14/CO (FA_X1) 0.06 1.08 f

D_Path/ALU_inst/add_8/U1_15/CO (FA_X1) 0.06 1.14 f

D_Path/ALU_inst/add_8/U1_16/CO (FA_X1) 0.06 1.19 f

D_Path/ALU_inst/add_8/U1_17/CO (FA_X1) 0.06 1.25 f

D_Path/ALU_inst/add_8/U1_18/CO (FA_X1) 0.06 1.31 f

D_Path/ALU_inst/add_8/U1_19/CO (FA_X1) 0.06 1.37 f

D_Path/ALU_inst/add_8/U1_20/CO (FA_X1) 0.06 1.42 f

D_Path/ALU_inst/add_8/U1_21/CO (FA_X1) 0.06 1.48 f

D_Path/ALU_inst/add_8/U1_22/CO (FA_X1) 0.06 1.54 f

D_Path/ALU_inst/add_8/U1_23/CO (FA_X1) 0.06 1.60 f

D_Path/ALU_inst/add_8/U1_24/CO (FA_X1) 0.06 1.66 f

D_Path/ALU_inst/add_8/U1_25/CO (FA_X1) 0.06 1.71 f

D_Path/ALU_inst/add_8/U1_26/CO (FA_X1) 0.06 1.77 f

D_Path/ALU_inst/add_8/U1_27/CO (FA_X1) 0.06 1.83 f

D_Path/ALU_inst/add_8/U1_28/CO (FA_X1) 0.06 1.89 f

D_Path/ALU_inst/add_8/U4/ZN (INV_X1) 0.02 1.91 r

D_Path/ALU_inst/add_8/U1/ZN (OAI22_X1) 0.03 1.94 f

D_Path/ALU_inst/add_8/U1_30/CO (FA_X1) 0.06 2.00 f

D_Path/ALU_inst/add_8/U15/ZN (XNOR2_X1) 0.04 2.04 f

D_Path/ALU_inst/add_8/U14/ZN (XNOR2_X1) 0.04 2.08 f

D_Path/ALU_inst/add_8/SUM[31] (ALU_DW01_add_0) 0.00 2.08 f

D_Path/ALU_inst/U17/ZN (AOI22_X1) 0.03 2.11 r

D_Path/ALU_inst/U40/ZN (NAND3_X1) 0.03 2.15 f

D_Path/ALU_inst/aluresult[31] (ALU) 0.00 2.15 f

D_Path/aluresult[31] (data_path) 0.00 2.15 f

U27/Z (BUF_X4) 0.08 2.22 f

aluresult[31] (out) 0.75 2.97 f

data arrival time		2.97
clock clk (rise edge)	6.00	6.00
clock network delay (ideal)	0.00	6.00
clock uncertainty	-0.35	5.65
output external delay	-3.00	2.65
data required time		2.65
---	---	---
data required time		2.65
data arrival time		-2.97
---	---	---
slack (VIOLATED)		-0.32

Constraints change (set_load command):

create_clock -name clk -period 6 [get_ports clk]

set_clock_uncertainty -setup 0.35 [get_clocks clk]

set_driving_cell -lib_cell BUF_X4 [remove_from_collection][all_inputs][get_ports clk]

set_input_delay -max 3 -clock [get_clocks clk] [remove_from_collection] [all_inputs] [get_ports clk]

set_output_delay -max 3 -clock [get_clocks clk] [all_outputs]

set_load -max 80 [all_outputs]

set_max_fanout 4 {rst}

set_max_fanout 4 {instr}

set_dont_use {NangateOpenCellLibrary_ff1p25v0c/DFFR_X1*}

set_max_area 10000

Timing report:

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 10
Design : top
Version: G-2012.06-SP2
Date   : Mon Oct  8 05:56:21 2018
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: fast   Library: NangateOpenCellLibrary_ff1p25v0c
Wire Load Model Mode: top

  Startpoint: D_Path/reg_file_inst/register_reg_30__0_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: aluresult[31]
            (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  top                5K_hvratio_1_1        NangateOpenCellLibrary_ff1p25v0c

  Point                                    Incr       Path
```

---

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

D_Path/reg_file_inst/register_reg_30__0_/CK (DFFR_X2)

0.00 # 0.00 r

D_Path/reg_file_inst/register_reg_30__0_/Q (DFFR_X2)

0.06 0.06 f

D_Path/reg_file_inst/U2839/ZN (AOI22_X1) 0.03 0.09 r

D_Path/reg_file_inst/U39/ZN (NAND3_X1) 0.03 0.12 f

D_Path/reg_file_inst/U343/ZN (NOR4_X1) 0.05 0.17 r

D_Path/reg_file_inst/U499/ZN (NAND2_X1) 0.02 0.20 f

D_Path/reg_file_inst/RD2[0] (regfile_32_bits) 0.00 0.20 f

D_Path/mux2_1_inst/in1[0] (mux2_1) 0.00 0.20 f

D_Path/mux2_1_inst/U2/Z (MUX2_X1) 0.04 0.24 f

D_Path/mux2_1_inst/out[0] (mux2_1) 0.00 0.24 f

D_Path/ALU_inst/data2[0] (ALU) 0.00 0.24 f

D_Path/ALU_inst/add_8/B[0] (ALU_DW01_add_0) 0.00 0.24 f

D_Path/ALU_inst/add_8/U15/ZN (AND2_X1) 0.03 0.27 f

D_Path/ALU_inst/add_8/U1_1/CO (FA_X1) 0.06 0.33 f

D_Path/ALU_inst/add_8/U1_2/CO (FA_X1) 0.06 0.38 f

D_Path/ALU_inst/add_8/U1_3/CO (FA_X1) 0.06 0.44 f

D_Path/ALU_inst/add_8/U1_4/CO (FA_X1) 0.06 0.50 f

D_Path/ALU_inst/add_8/U1_5/CO (FA_X1) 0.06 0.56 f

D_Path/ALU_inst/add_8/U1_6/CO (FA_X1) 0.06 0.61 f

D_Path/ALU_inst/add_8/U1_7/CO (FA_X1) 0.06 0.67 f

D_Path/ALU_inst/add_8/U1_8/CO (FA_X1) 0.06 0.73 f

D_Path/ALU_inst/add_8/U1_9/CO (FA_X1) 0.06 0.79 f

D_Path/ALU_inst/add_8/U1_10/CO (FA_X1) 0.06 0.85 f

D_Path/ALU_inst/add_8/U1_11/CO (FA_X1) 0.06 0.90 f

D_Path/ALU_inst/add_8/U1_12/CO (FA_X1) 0.06 0.96 f

D_Path/ALU_inst/add_8/U1_13/CO (FA_X1) 0.06 1.02 f

D_Path/ALU_inst/add_8/U1_14/CO (FA_X1) 0.06 1.08 f

D_Path/ALU_inst/add_8/U1_15/CO (FA_X1) 0.06 1.14 f

D_Path/ALU_inst/add_8/U1_16/CO (FA_X1) 0.06 1.19 f

D_Path/ALU_inst/add_8/U1_17/CO (FA_X1) 0.06 1.25 f

D_Path/ALU_inst/add_8/U1_18/CO (FA_X1) 0.06 1.31 f

D_Path/ALU_inst/add_8/U1_19/CO (FA_X1) 0.06 1.37 f

D_Path/ALU_inst/add_8/U1_20/CO (FA_X1) 0.06 1.42 f

D_Path/ALU_inst/add_8/U1_21/CO (FA_X1) 0.06 1.48 f

D_Path/ALU_inst/add_8/U1_22/CO (FA_X1) 0.06 1.54 f

D_Path/ALU_inst/add_8/U1_23/CO (FA_X1) 0.06 1.60 f

D_Path/ALU_inst/add_8/U1_24/CO (FA_X1) 0.06 1.66 f

D_Path/ALU_inst/add_8/U1_25/CO (FA_X1) 0.06 1.71 f

D_Path/ALU_inst/add_8/U1_26/CO (FA_X1) 0.06 1.77 f

D_Path/ALU_inst/add_8/U1_27/CO (FA_X1) 0.06 1.83 f

D_Path/ALU_inst/add_8/U1_28/CO (FA_X1) 0.06 1.89 f

D_Path/ALU_inst/add_8/U4/ZN (INV_X1) 0.02 1.91 r

D_Path/ALU_inst/add_8/U1/ZN (OAI22_X1) 0.03 1.94 f

D_Path/ALU_inst/add_8/U1_30/CO (FA_X1) 0.06 2.00 f

D_Path/ALU_inst/add_8/U14/ZN (XNOR2_X1) 0.04 2.04 f

D_Path/ALU_inst/add_8/U13/ZN (XNOR2_X1) 0.04 2.08 f

D_Path/ALU_inst/add_8/SUM[31] (ALU_DW01_add_0) 0.00 2.08 f

D_Path/ALU_inst/U203/ZN (AOI22_X1) 0.04 2.11 r

D_Path/ALU_inst/U104/ZN (NAND3_X1) 0.03 2.15 f

D_Path/ALU_inst/aluresult[31] (ALU) 0.00 2.15 f

D_Path/aluresult[31] (data_path) 0.00 2.15 f

U26/Z (BUF_X4) 0.06 2.21 f

aluresult[31] (out) 0.50 2.71 f

data arrival time		2.71
clock clk (rise edge)	6.00	6.00
clock network delay (ideal)	0.00	6.00
clock uncertainty	-0.35	5.65
output external delay	-3.00	2.65
data required time		2.65
---		
data required time		2.65
data arrival time		-2.71
---		
slack (VIOLATED)		-0.06

Constraints change (set_input and set_output_delay command):

create_clock -name clk -period 6 [get_ports clk]

set_clock_uncertainty -setup 0.35 [get_clocks clk]

set_driving_cell -lib_cell BUF_X4 [remove_from_collection][all_inputs][get_ports clk]

set_input_delay -max 2.4 -clock [get_clocks clk] [remove_from_collection] [all_inputs] [get_ports clk]

set_output_delay -max 2.4 -clock [get_clocks clk] [all_outputs]

set_load -max 80 [all_outputs]

set_max_fanout 4 {rst}

set_max_fanout 4 {instr}

set_dont_use {NangateOpenCellLibrary_ff1p25v0c/DFFR_X1*}

set_max_area 10000

Timing report:

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 10
Design : top
Version: G-2012.06-SP2
Date   : Mon Oct  8 06:05:01 2018
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: fast   Library: NangateOpenCellLibrary_ff1p25v0c
Wire Load Model Mode: top

  Startpoint: D_Path/reg_file_inst/register_reg[31][0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: aluresult[31]
            (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  top                5K_hvratio_1_1        NangateOpenCellLibrary_ff1p25v0c

  Point                                    Incr       Path
```

```
---------------------------------------------------------------------------
clock clk (rise edge)                          0.00       0.00
clock network delay (ideal)                    0.00       0.00
D_Path/reg_file_inst/register_reg[31][0]/CK (DFFR_X2)
                                               0.00 #     0.00 r
D_Path/reg_file_inst/register_reg[31][0]/Q (DFFR_X2)
                                               0.06       0.06 f
D_Path/reg_file_inst/U3327/Z (MUX2_X1)         0.04       0.10 f
D_Path/reg_file_inst/U3329/Z (MUX2_X1)         0.04       0.14 f
D_Path/reg_file_inst/U3333/Z (MUX2_X1)         0.04       0.18 f
D_Path/reg_file_inst/U3341/Z (MUX2_X1)         0.04       0.22 f
D_Path/reg_file_inst/U33/Z (MUX2_X2)           0.09       0.30 f
D_Path/reg_file_inst/RD2[0] (regfile_32_bits)  0.00       0.30 f
D_Path/mux2_1_inst/in1[0] (mux2_1)             0.00       0.30 f
D_Path/mux2_1_inst/U47/ZN (AOI22_X1)           0.04       0.35 r
D_Path/mux2_1_inst/U46/ZN (INV_X1)             0.03       0.38 f
D_Path/mux2_1_inst/out[0] (mux2_1)             0.00       0.38 f
D_Path/ALU_inst/data2[0] (ALU)                 0.00       0.38 f
D_Path/ALU_inst/add_8/B[0] (ALU_DW01_add_0)    0.00       0.38 f
D_Path/ALU_inst/add_8/U2/ZN (AND2_X1)          0.03       0.41 f
D_Path/ALU_inst/add_8/U1_1/CO (FA_X1)          0.06       0.47 f
D_Path/ALU_inst/add_8/U1_2/CO (FA_X1)          0.06       0.53 f
D_Path/ALU_inst/add_8/U1_3/CO (FA_X1)          0.06       0.59 f
D_Path/ALU_inst/add_8/U1_4/CO (FA_X1)          0.06       0.64 f
D_Path/ALU_inst/add_8/U1_5/CO (FA_X1)          0.06       0.70 f
D_Path/ALU_inst/add_8/U1_6/CO (FA_X1)          0.06       0.76 f
D_Path/ALU_inst/add_8/U1_7/CO (FA_X1)          0.06       0.82 f
D_Path/ALU_inst/add_8/U1_8/CO (FA_X1)          0.06       0.87 f
D_Path/ALU_inst/add_8/U1_9/CO (FA_X1)          0.06       0.93 f
```

D_Path/ALU_inst/add_8/U1_10/CO (FA_X1) 0.06 0.99 f

D_Path/ALU_inst/add_8/U1_11/CO (FA_X1) 0.06 1.05 f

D_Path/ALU_inst/add_8/U1_12/CO (FA_X1) 0.06 1.11 f

D_Path/ALU_inst/add_8/U1_13/CO (FA_X1) 0.06 1.16 f

D_Path/ALU_inst/add_8/U1_14/CO (FA_X1) 0.06 1.22 f

D_Path/ALU_inst/add_8/U1_15/CO (FA_X1) 0.06 1.28 f

D_Path/ALU_inst/add_8/U1_16/CO (FA_X1) 0.06 1.34 f

D_Path/ALU_inst/add_8/U1_17/CO (FA_X1) 0.06 1.40 f

D_Path/ALU_inst/add_8/U1_18/CO (FA_X1) 0.06 1.45 f

D_Path/ALU_inst/add_8/U1_19/CO (FA_X1) 0.06 1.51 f

D_Path/ALU_inst/add_8/U1_20/CO (FA_X1) 0.06 1.57 f

D_Path/ALU_inst/add_8/U1_21/CO (FA_X1) 0.06 1.63 f

D_Path/ALU_inst/add_8/U1_22/CO (FA_X1) 0.06 1.68 f

D_Path/ALU_inst/add_8/U1_23/CO (FA_X1) 0.06 1.74 f

D_Path/ALU_inst/add_8/U1_24/CO (FA_X1) 0.06 1.80 f

D_Path/ALU_inst/add_8/U1_25/CO (FA_X1) 0.06 1.86 f

D_Path/ALU_inst/add_8/U1_26/CO (FA_X1) 0.06 1.92 f

D_Path/ALU_inst/add_8/U1_27/CO (FA_X1) 0.06 1.97 f

D_Path/ALU_inst/add_8/U1_28/CO (FA_X1) 0.06 2.03 f

D_Path/ALU_inst/add_8/U1_29/CO (FA_X1) 0.06 2.09 f

D_Path/ALU_inst/add_8/U1_30/CO (FA_X1) 0.06 2.15 f

D_Path/ALU_inst/add_8/U1_31/S (FA_X1) 0.08 2.23 r

D_Path/ALU_inst/add_8/SUM[31] (ALU_DW01_add_0) 0.00 2.23 r

D_Path/ALU_inst/U54/ZN (AOI22_X1) 0.03 2.26 f

D_Path/ALU_inst/U15/ZN (OAI211_X1) 0.03 2.29 r

D_Path/ALU_inst/U13/ZN (INV_X1) 0.02 2.31 f

D_Path/ALU_inst/U14/ZN (INV_X2) 0.09 2.39 r

D_Path/ALU_inst/aluresult[31] (ALU) 0.00 2.39 r

D_Path/aluresult[31] (data_path) 0.00 2.39 r

aluresult[31] (out)	0.62	3.01 r
data arrival time		3.01
clock clk (rise edge)	6.00	6.00
clock network delay (ideal)	0.00	6.00
clock uncertainty	-0.35	5.65
output external delay	-2.40	3.25
data required time		3.25

---

data required time	3.25
data arrival time	-3.01

---

slack (MET)	0.24

Constraints change (set_clock_uncertainty command):

```
create_clock -name clk -period 6 [get_ports clk]

set_clock_uncertainty -setup 0.2 [get_clocks clk]

set_driving_cell -lib_cell BUF_X4 [remove_from_collection][all_inputs][get_ports clk]

set_input_delay -max 3 -clock [get_clocks clk] [remove_from_collection] [all_inputs] [get_ports clk]

set_output_delay -max 3 -clock [get_clocks clk] [all_outputs]

set_load -max 80 [all_outputs]

set_max_fanout 4 {rst}

set_max_fanout 4 {instr}

set_dont_use {NangateOpenCellLibrary_ff1p25v0c/DFFR_X1*}

set_max_area 10000
```

Timing report:

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 10
Design : top
Version: G-2012.06-SP2
Date   : Mon Oct  8 06:18:34 2018
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 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: fast   Library: NangateOpenCellLibrary_ff1p25v0c
Wire Load Model Mode: top

  Startpoint: D_Path/reg_file_inst/register_reg_9__2_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: aluresult[31]
            (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  top                5K_hvratio_1_1        NangateOpenCellLibrary_ff1p25v0c

  Point                                    Incr       Path
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---------------------------------------------------------------------------
clock clk (rise edge)                          0.00       0.00
clock network delay (ideal)                    0.00       0.00
D_Path/reg_file_inst/register_reg_9__2_/CK (DFFR_X2)
                                               0.00 #     0.00 r
D_Path/reg_file_inst/register_reg_9__2_/Q (DFFR_X2)     0.06       0.06 f
D_Path/reg_file_inst/U2508/ZN (AOI22_X1)                0.04       0.10 r
D_Path/reg_file_inst/U2507/ZN (OAI221_X1)               0.03       0.14 f
D_Path/reg_file_inst/U32/ZN (OR4_X1)                    0.07       0.20 f
D_Path/reg_file_inst/U30/ZN (OR2_X2)                    0.08       0.28 f
D_Path/reg_file_inst/RD2[2] (regfile_32_bits)           0.00       0.28 f
D_Path/mux2_1_inst/in1[2] (mux2_1)                      0.00       0.28 f
D_Path/mux2_1_inst/U47/ZN (AOI22_X1)                    0.04       0.33 r
D_Path/mux2_1_inst/U33/ZN (INV_X1)                      0.03       0.36 f
D_Path/mux2_1_inst/out[2] (mux2_1)                      0.00       0.36 f
D_Path/ALU_inst/data2[2] (ALU)                          0.00       0.36 f
D_Path/ALU_inst/add_8/B[2] (ALU_DW01_add_0)             0.00       0.36 f
D_Path/ALU_inst/add_8/U1_2/CO (FA_X1)                   0.08       0.44 f
D_Path/ALU_inst/add_8/U1_3/CO (FA_X1)                   0.06       0.50 f
D_Path/ALU_inst/add_8/U1_4/CO (FA_X1)                   0.06       0.55 f
D_Path/ALU_inst/add_8/U1_5/CO (FA_X1)                   0.06       0.61 f
D_Path/ALU_inst/add_8/U1_6/CO (FA_X1)                   0.06       0.67 f
D_Path/ALU_inst/add_8/U1_7/CO (FA_X1)                   0.06       0.73 f
D_Path/ALU_inst/add_8/U1_8/CO (FA_X1)                   0.06       0.78 f
D_Path/ALU_inst/add_8/U1_9/CO (FA_X1)                   0.06       0.84 f
D_Path/ALU_inst/add_8/U1_10/CO (FA_X1)                  0.06       0.90 f
D_Path/ALU_inst/add_8/U1_11/CO (FA_X1)                  0.06       0.96 f
D_Path/ALU_inst/add_8/U1_12/CO (FA_X1)                  0.06       1.02 f
D_Path/ALU_inst/add_8/U1_13/CO (FA_X1)                  0.06       1.07 f
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D_Path/ALU_inst/add_8/U1_14/CO (FA_X1) 0.06 1.13 f

D_Path/ALU_inst/add_8/U1_15/CO (FA_X1) 0.06 1.19 f

D_Path/ALU_inst/add_8/U1_16/CO (FA_X1) 0.06 1.25 f

D_Path/ALU_inst/add_8/U1_17/CO (FA_X1) 0.06 1.31 f

D_Path/ALU_inst/add_8/U1_18/CO (FA_X1) 0.06 1.36 f

D_Path/ALU_inst/add_8/U1_19/CO (FA_X1) 0.06 1.42 f

D_Path/ALU_inst/add_8/U1_20/CO (FA_X1) 0.06 1.48 f

D_Path/ALU_inst/add_8/U1_21/CO (FA_X1) 0.06 1.54 f

D_Path/ALU_inst/add_8/U1_22/CO (FA_X1) 0.06 1.59 f

D_Path/ALU_inst/add_8/U1_23/CO (FA_X1) 0.06 1.65 f

D_Path/ALU_inst/add_8/U1_24/CO (FA_X1) 0.06 1.71 f

D_Path/ALU_inst/add_8/U1_25/CO (FA_X1) 0.06 1.77 f

D_Path/ALU_inst/add_8/U1_26/CO (FA_X1) 0.06 1.83 f

D_Path/ALU_inst/add_8/U1_27/CO (FA_X1) 0.06 1.88 f

D_Path/ALU_inst/add_8/U1_28/CO (FA_X1) 0.06 1.94 f

D_Path/ALU_inst/add_8/U1_29/CO (FA_X1) 0.06 2.00 f

D_Path/ALU_inst/add_8/U1_30/CO (FA_X1) 0.06 2.06 f

D_Path/ALU_inst/add_8/U1_31/S (FA_X1) 0.08 2.14 r

D_Path/ALU_inst/add_8/SUM[31] (ALU_DW01_add_0) 0.00 2.14 r

D_Path/ALU_inst/U207/ZN (AOI22_X1) 0.03 2.17 f

D_Path/ALU_inst/U121/ZN (OAI221_X1) 0.03 2.20 r

D_Path/ALU_inst/aluresult[31] (ALU) 0.00 2.20 r

D_Path/aluresult[31] (data_path) 0.00 2.20 r

U1/Z (BUF_X2) 0.09 2.29 r

aluresult[31] (out) 0.50 2.79 r

data arrival time 2.79

clock clk (rise edge) 6.00 6.00

clock network delay (ideal) 0.00 6.00

clock uncertainty	-0.20	5.80
output external delay	-3.00	2.80
data required time		2.80

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data required time	2.80
data arrival time	-2.79

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slack (MET)	0.01