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LAB 1: Synthesis

part 1: using typical libraries.

First -> synthesis script is as following:

```
set design mips_16
set_app_var search_path "/home/standard_cell_libraries/NangateOpenCellLibrary_PDKv1_3_v2010_12/lib/Front_End/Liberty/NLDM"

set_app_var link_library "NangateOpenCellLibrary_tt1p1v25c.db "

set_app_var target_library "NangateOpenCellLibrary_tt1p1v25c.db "

sh rm -rf work
sh mkdir -p work
define_design_lib work -path ./work


analyze -library work -format verilog ./$design.v
elaborate $design -lib work
current_design


source ./cons.tcl
link
check_design

compile -map_effort medium

report_area  -hierarchy > /home/ahesham/Desktop/ITI_PHASE1/Mips/report/synth_area.rpt
report_cell > /home/ahesham/Desktop/ITI_PHASE1/Mips/report/synth_cells.rpt
report_qor  >  /home/ahesham/Desktop/ITI_PHASE1/Mips/report/synth_qor.rpt
report_resources > /home/ahesham/Desktop/ITI_PHASE1/Mips/report/synth_resources.rpt
report_timing -max_paths 10 > /home/ahesham/Desktop/ITI_PHASE1/Mips/report/synth_timing_setup.rpt
report_timing -delay_type min -max_paths 10 > /home/ahesham/Desktop/ITI_PHASE1/Mips/report/synth_timing_hold.rpt

write_sdc  output/${design}.sdc

define_name_rules  no_case -case_insensitive
change_names -rule no_case -hierarchy
change_names -rule verilog -hierarchy
set verilogout_no_tri    true
set verilogout_equation  false

write -hierarchy -format verilog -output output/${design}.v
write_sdf -version 2.1 output/${design}.sdf
write -f ddc -hierarchy -output output/${design}.ddc
```

and constraint file is as following:

```
create_clock -name clk -period 6 [get_ports clk]
set_clock_uncertainty -setup 0.2 [get_clocks clk]
set_input_delay -max 3 -clock [get_clocks clk] [remove_from_collection] [all_inputs] [get_ports clk]
set_output_delay -max 3 -clock [get_clocks clk] [all_outputs]
```

results of timing reports:

```
 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: typical   Library: NangateOpenCellLibrary_tt1p1v25c
Wire Load Model Mode: top

  Startpoint: pc_current_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: pc_out[1] (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mips_16            5K_hvratio_1_1        NangateOpenCellLibrary_tt1p1v25c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  pc_current_reg[1]/CK (DFFR_X1)           0.00 #     0.00 r
  pc_current_reg[1]/Q (DFFR_X1)            0.11       0.11 r
  pc_out[1] (out)                          0.00       0.11 r
  data arrival time                                   0.11

  clock clk (rise edge)                    6.00       6.00
  clock network delay (ideal)              0.00       6.00
  clock uncertainty                       -0.20       5.80
  output external delay                   -3.00       2.80
  data required time                                  2.80
  -----------------------------------------------------------
  data required time                                  2.80
  data arrival time                                  -0.11
  -----------------------------------------------------------
  slack (MET)                                        2.69
```

Then optimizing by providing the tool one constraint more as following:

```
create_clock -name clk -period 6 [get_ports clk]
set_clock_uncertainty -setup 0.2 [get_clocks clk]
set_input_delay -max 3 -clock [get_clocks clk] [remove_from_collection] [all_inputs] [get_ports clk]
set_output_delay -max 3 -clock [get_clocks clk] [all_outputs]
set_driving_cell -lib_cell BUF_X4 [remove_from_collection][all_inputs][get_ports clk]
set_load -max 80 [all_outputs]
```

results of timing reports:

```
Operating Conditions: typical   Library: NangateOpenCellLibrary_tt1p1v25c
Wire Load Model Mode: top

  Startpoint: pc_current_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: pc_out[1] (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mips_16            5K_hvratio_1_1        NangateOpenCellLibrary_tt1p1v25c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  pc_current_reg[1]/CK (DFFR_X2)           0.00 #     0.00 r
  pc_current_reg[1]/Q (DFFR_X2)            0.22       0.22 r
  pc_out[1] (out)                          0.66       0.88 r
  data arrival time                                   0.88

  clock clk (rise edge)                    6.00       6.00
  clock network delay (ideal)              0.00       6.00
  clock uncertainty                       -0.20       5.80
  output external delay                   -3.00       2.80
  data required time                                  2.80
  -----------------------------------------------------------
  data required time                                  2.80
  data arrival time                                  -0.88
  -----------------------------------------------------------
  slack (MET)                                        1.92
```

Optimizing again:

```
create_clock -name clk -period 6 [get_ports clk]
set_clock_uncertainty -setup 0.2 [get_clocks clk]
set_input_delay -max 3 -clock [get_clocks clk] [remove_from_collection] [all_inputs] [get_ports clk]
set_output_delay -max 3 -clock [get_clocks clk] [all_outputs]
set_driving_cell -lib_cell BUF_X4 [remove_from_collection][all_inputs][get_ports clk]
set_load -max 120 [all_outputs]
```

results of timing reports:

```
Operating Conditions: typical   Library: NangateOpenCellLibrary_tt1p1v25c
Wire Load Model Mode: top

  Startpoint: pc_current_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: pc_out[1] (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mips_16            5K_hvratio_1_1        NangateOpenCellLibrary_tt1p1v25c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  pc_current_reg[1]/CK (DFFR_X1)           0.00 #     0.00 r
  pc_current_reg[1]/QN (DFFR_X1)           0.08       0.08 f
  U185/ZN (INV_X4)                         0.14       0.23 r
  pc_out[1] (out)                          0.99       1.22 r
  data arrival time                                   1.22

  clock clk (rise edge)                    6.00       6.00
  clock network delay (ideal)              0.00       6.00
  clock uncertainty                       -0.20       5.80
  output external delay                   -3.00       2.80
  data required time                                  2.80
  -----------------------------------------------------------
  data required time                                  2.80
  data arrival time                                  -1.22
  -----------------------------------------------------------
  slack (MET)                                        1.58
```

After a lot of iterations and constraints, final constraints are:

```
create_clock -name clk -period 4 [get_ports clk]
set_clock_uncertainty -setup 0.8 [get_clocks clk]
set_input_delay -max 3 -clock [get_clocks clk] [remove_from_collection] [all_inputs] [get_ports clk]
set_output_delay -max 3 -clock [get_clocks clk] [all_outputs]
```

Final minimum positive setup slack is 0.9 as following:

```
Operating Conditions: typical   Library: NangateOpenCellLibrary_tt1p1v25c
Wire Load Model Mode: top

  Startpoint: pc_current_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: pc_out[1] (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mips_16            5K_hvratio_1_1        NangateOpenCellLibrary_tt1p1v25c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  pc_current_reg[1]/CK (DFFR_X1)           0.00 #     0.00 r
  pc_current_reg[1]/Q (DFFR_X1)            0.11       0.11 r
  pc_out[1] (out)                          0.00       0.11 r
  data arrival time                                   0.11

  clock clk (rise edge)                    4.00       4.00
  clock network delay (ideal)              0.00       4.00
  clock uncertainty                       -0.80       3.20
  output external delay                   -3.00       0.20
  data required time                                  0.20
  -----------------------------------------------------------
  data required time                                  0.20
  data arrival time                                  -0.11
  -----------------------------------------------------------
  slack (MET)                                         0.09
```

part 1: using worst libraries.

First -> synthesis script is as following:

```
set design mips_16
set_app_var search_path "/home/standard_cell_libraries/NangateOpenCellLibrary_PDKv1_3_v2010_12/lib/Front_End/Liberty/NLDM"

set_app_var link_library "NangateOpenCellLibrary_ss0p95vn40c.db "

set_app_var target_library "NangateOpenCellLibrary_ss0p95vn40c.db "

sh rm -rf work
sh mkdir -p work
define_design_lib work -path ./work


analyze -library work -format verilog ./$design.v
elaborate $design -lib work
current_design


source ./cons.tcl
link
check_design

compile -map_effort medium

report_area  -hierarchy > /home/ahesham/Desktop/ITI_PHASE1/Mips/report/synth_area.rpt
report_cell > /home/ahesham/Desktop/ITI_PHASE1/Mips/report/synth_cells.rpt
report_qor  > /home/ahesham/Desktop/ITI_PHASE1/Mips/report/synth_qor.rpt
report_resources > /home/ahesham/Desktop/ITI_PHASE1/Mips/report/synth_resources.rpt
report_timing -max_paths 10 > /home/ahesham/Desktop/ITI_PHASE1/Mips/report/synth_timing_setup.rpt
report_timing -delay_type min -max_paths 10 > /home/ahesham/Desktop/ITI_PHASE1/Mips/report/synth_timing_hold.rpt

write_sdc  output/${design}.sdc

define_name_rules  no_case -case_insensitive
change_names -rule no_case -hierarchy
change_names -rule verilog -hierarchy
set verilogout_no_tri    true
set verilogout_equation  false

write -hierarchy -format verilog -output output/${design}.v
write_sdf -version 2.1 output/${design}.sdf
write -f ddc -hierarchy -output output/${design}.ddc
```

and constraint file is as following:

```
create_clock -name clk -period 6 [get_ports clk]
set_clock_uncertainty -setup 0.2 [get_clocks clk]
set_input_delay -max 3 -clock [get_clocks clk] [remove_from_collection] [all_inputs] [get_ports clk]
set_output_delay -max 3 -clock [get_clocks clk] [all_outputs]
```

Results of timing reports:

```
Operating Conditions: worst_low   Library: NangateOpenCellLibrary_ss0p95vn40c
Wire Load Model Mode: top

  Startpoint: pc_current_reg[15]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: pc_out[15] (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mips_16            5K_hvratio_1_1        NangateOpenCellLibrary_ss0p95vn40c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  pc_current_reg[15]/CK (DFFRS_X1)         0.00 #     0.00 r
  pc_current_reg[15]/Q (DFFRS_X1)          0.08       0.08 f
  pc_out[15] (out)                         0.00       0.08 f
  data arrival time                                   0.08

  clock clk (rise edge)                    6.00       6.00
  clock network delay (ideal)              0.00       6.00
  clock uncertainty                       -0.20       5.80
  output external delay                   -3.00       2.80
  data required time                                  2.80
  -----------------------------------------------------------
  data required time                                  2.80
  data arrival time                                  -0.08
  -----------------------------------------------------------
  slack (MET)                                         2.72
```

After some iterations, the final constraints are as following:

```
create_clock -name clk -period 4 [get_ports clk]
set_clock_uncertainty -setup 0.3 [get_clocks clk]
set_input_delay -max 3 -clock [get_clocks clk] [remove_from_collection] [all_inputs] [get_ports clk]
set_output_delay -max 3 -clock [get_clocks clk] [all_outputs]
set_load -max 80 [all_outputs]
set_dont_use {NangateOpenCellLibrary_ss0p95vn40c/DFFRS_X1*}
```

Final minimum setup slack is zero as shown:

```
Operating Conditions: worst_low   Library: NangateOpenCellLibrary_ss0p95vn40c
Wire Load Model Mode: top

  Startpoint: pc_current_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: pc_out[0] (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mips_16            5K_hvratio_1_1        NangateOpenCellLibrary_ss0p95vn40c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  pc_current_reg[0]/CK (SDFFR_X1)          0.00 #     0.00 r
  pc_current_reg[0]/QN (SDFFR_X1)          0.09       0.09 f
  U283/ZN (INV_X2)                         0.10       0.20 r
  pc_out[0] (out)                          0.50       0.70 r
  data arrival time                                   0.70

  clock clk (rise edge)                    4.00       4.00
  clock network delay (ideal)              0.00       4.00
  clock uncertainty                       -0.30       3.70
  output external delay                   -3.00       0.70
  data required time                                  0.70
  -----------------------------------------------------------
  data required time                                  0.70
  data arrival time                                  -0.70
  -----------------------------------------------------------
  slack (MET)                                         0.00
```

Comment:

As shown from final constraints, the clock frequency is the same for both but notice that clock uncertainty model for worst library is more optimism than typical library so:

maximum clock frequency for worst library = 1/(4ns – 0.3 ns) = 0.27 GHZ

maximum clock frequency for typical library = 1/(4ns – 0.8ns) = 0.3125 GHZ