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LAB 1: Linting

Q1.

The major violations that linting tool can detect are:

* Non-Synthesizable constructs
* Unintentional latches
* Unused declarations
* Multiple drivers and undriven signals
* Race conditions
* Incorrect usage of blocking and non-blocking assignments
* Incomplete assignments in subroutines
* Case statement style issues
* Set and reset conflicts
* Out-of-range indexing

Q2.



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Error: combinational loop

Solution: break the loop by a flip-flop as follows:

**module** Q2\_a**(output** **reg** a**,** **input** b**,**clk**,**rst**);**

**always@(posedge** clk**,negedge** rst**)**

**begin**

**if(~**rst**)**

a **<=** 0**;**

**else**

a **<=** a **&** b**;**

**end**

**endmodule**



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Error: flip-flop should have an asynchronous set or reset

Solution: put asynchronous reset for flip-flop

**module** Q2\_b**(output** **reg** c**,** **input** a**,**b**,**clk**,**rst**);**

**always@(posedge** clk**,negedge** rst**)**

**begin**

**if(~**rst**)**

c **<=** 0**;**

**else** **if(**a **>** b**)**

c **<=** a**;**

**end**

**endmodule**



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Error: - Do not assign over the same signal in an always construct for sequential circuits

* No begin-end for if statement before else.
* Flip-flop should have an asynchronous set or reset.

Solution: - declare another variable with c variable to assign it to b.

* add begin-end in if statement.
* put asynchronous reset for flip flop

**module** Q2\_c**(input** a**,**b**,**clk**,**rst**,** **output** **reg** c**,**d**);**

**always@(posedge** clk**,negedge** rst**)**

**begin**

**if(~**rst**)**

**begin**

c **<=** 0**;**

d **<=** 0**;**

**end**

**else** **if** **(**a **>** b**)**

**begin**

c **<=** a**;**

d **<=** b**;**

**end**

**else**

c **<=** c**;**

**end**

**endmodule**



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Error: - LHS width is less than RHS width of assignment

* Block should not contain feedthroughs.

Solution: - make size of LHS equal to size of RHS and solve feedthroughs using buffer.

**module** Q2\_d**(**

**input** **[**7**:**0**]** b**,**

**output** **[**7**:**0**]** a

**);**

**buf** b1**(**a**,**b**);**

**endmodule**



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Error: An input has been declared but not read

Solution: remove input B.

**module** Q2\_e**(**

**input** a**,**

**output** c**);**

**assign** c **=** a**;**

**endmodule**





Error: - RHS of the assignment contains X.

* Based number 32'bx has no meaning in synthesis.

Solution: - assign another value for A

**module** Q2\_f**(**

**output** **[**31**:**0**]** A

**);**

**assign** A **=** 32'b1**;**

**endmodule**



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Error: - case statement(or selected signal assignment) does not have a default or OTHERS clause.

* Latch inferred for signal 'x' in module 'Q2\_g'.

Solution: - add default statement

**module** Q2\_g**(**

**input** **[**1**:**0**]** v**,**

**output** **reg** x

**);**

**always** **@(\*)** **begin**

**case(**v**)**

2'b00**:** x **=** 1'b1**;**

2'b10**:** x **=** 1'b0**;**

**default:** x **=** 1'b1**;**

**endcase**

**end**

**endmodule**



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Error: - Combinational loop exists at 'Q2\_h.a- Q2\_h.z- Q2\_h.out'.

* Reserved name 'out'.

Solution: - change in assign statements to eliminate combinational loops

**module** Q2\_h**(**

**input** **wire** en**,**inp**,**c**,**y**,**

**output** **wire** out**,**a**,**z

**);**

**assign** out **=** en**?** inp**:**c**;**

**assign** a **=** en**?** y**:**c**;**

**assign** z **=** en**?** inp**:**y**;**

**endmodule**



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Error: - Flip-flop 'out2' has neither asynchronous set nor asynchronous reset.

- Asynchronous reset signal 'lint.rst' (flop: 'Q2\_i.out1') used as non reset/synchronous-reset at instance 'Q2\_i.out2\_reg.D'

Solution: - put asynchronous reset for flip flop of out2

**module** Q2\_i **(**

**input** **wire** clk**,**rst**,**in**,**

**output** **reg** out1**,**out2

**);**

**always** **@(posedge** clk **or** **posedge** rst**)** **begin**

**if(**rst**)** **begin**

out1 **<=** 1'b0**;**

**end**

**else** **begin**

out1 **<=** in**;**

**end**

**end**

**always** **@(posedge** clk **or** **posedge** rst**)** **begin**

**if(**rst**)** **begin**

out2 **<=** 1'b0**;**

**end**

**else** **begin**

out2 **<=** in**;**

**end**

**end**

**endmodule**