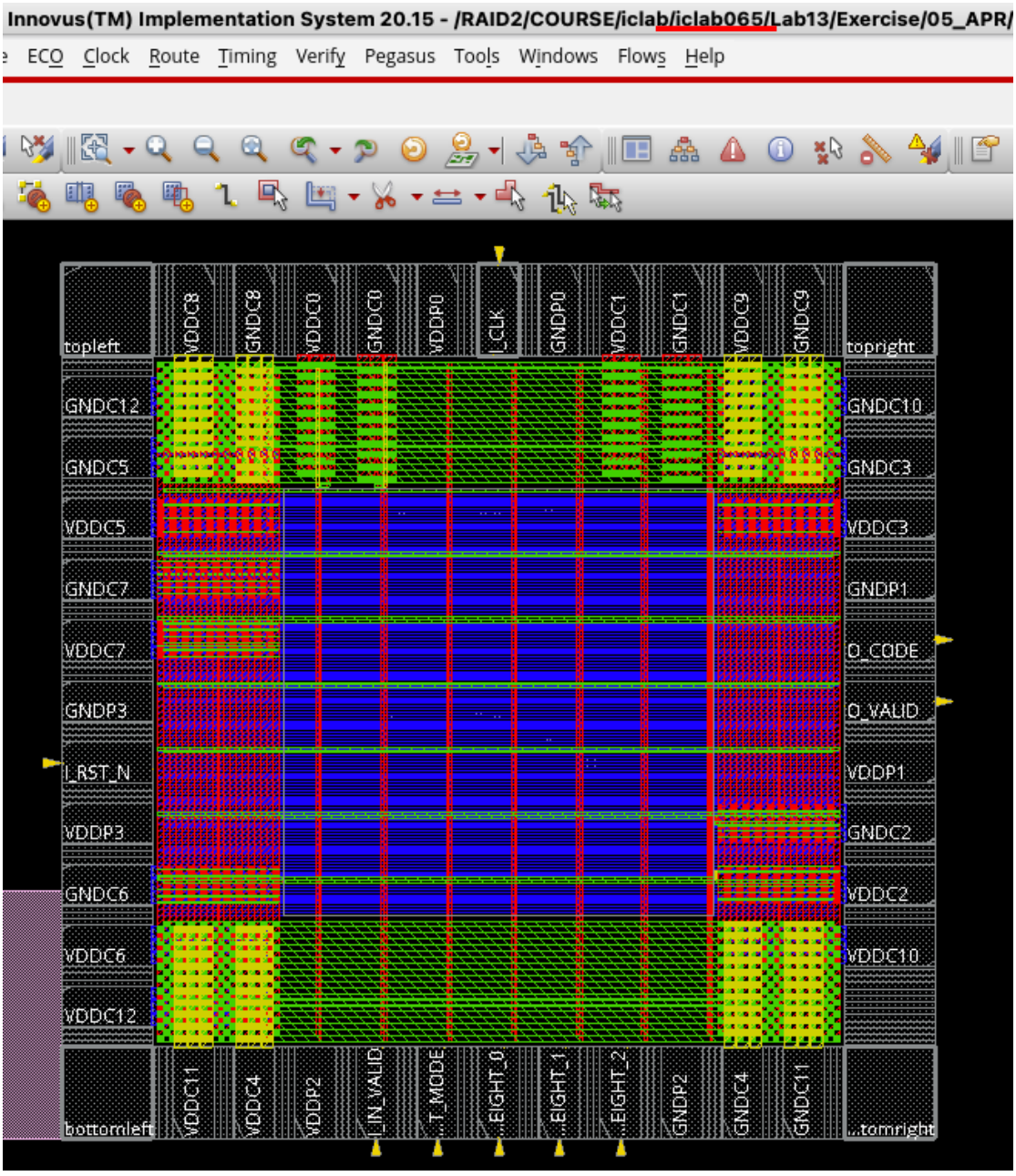
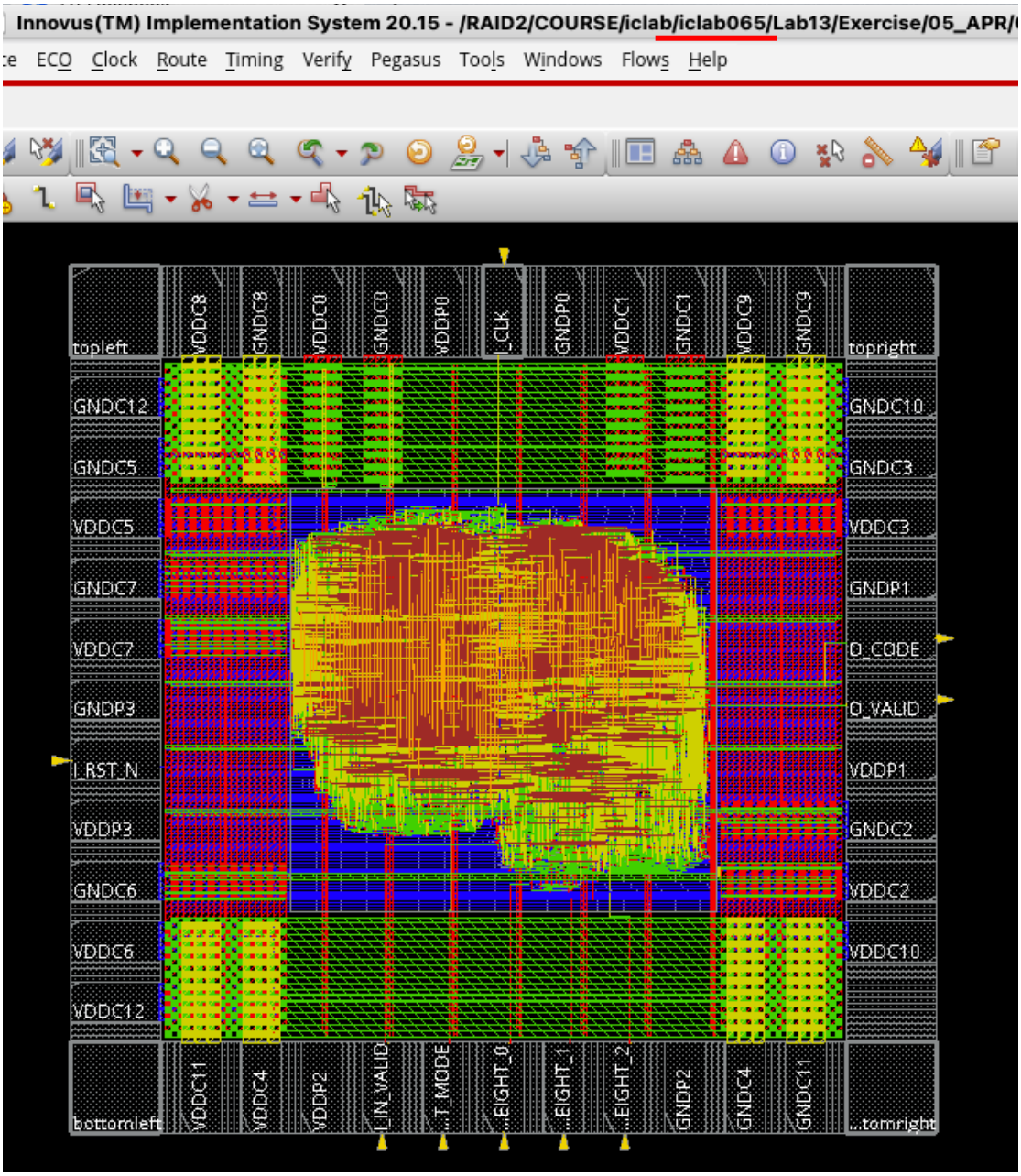
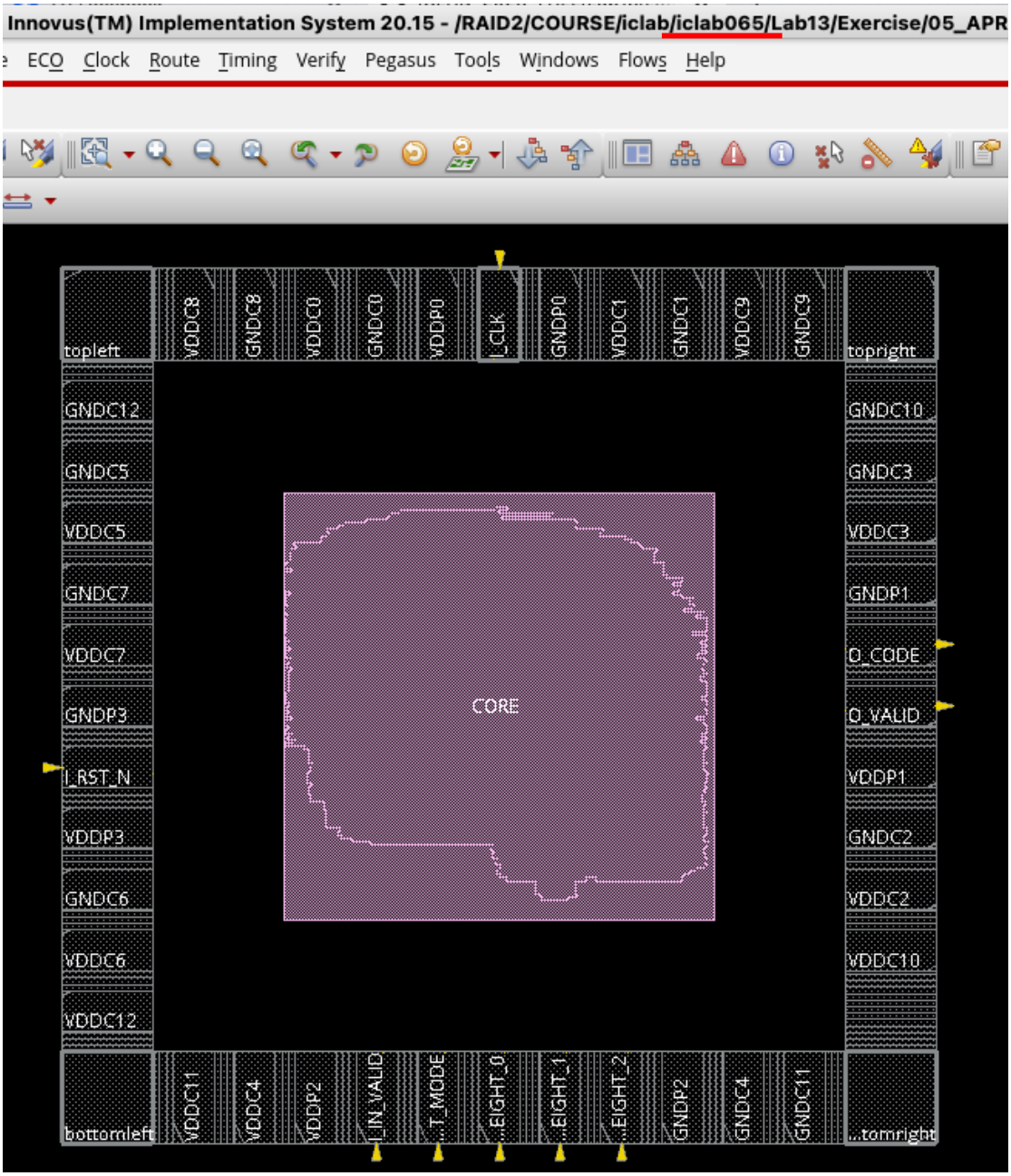
Report

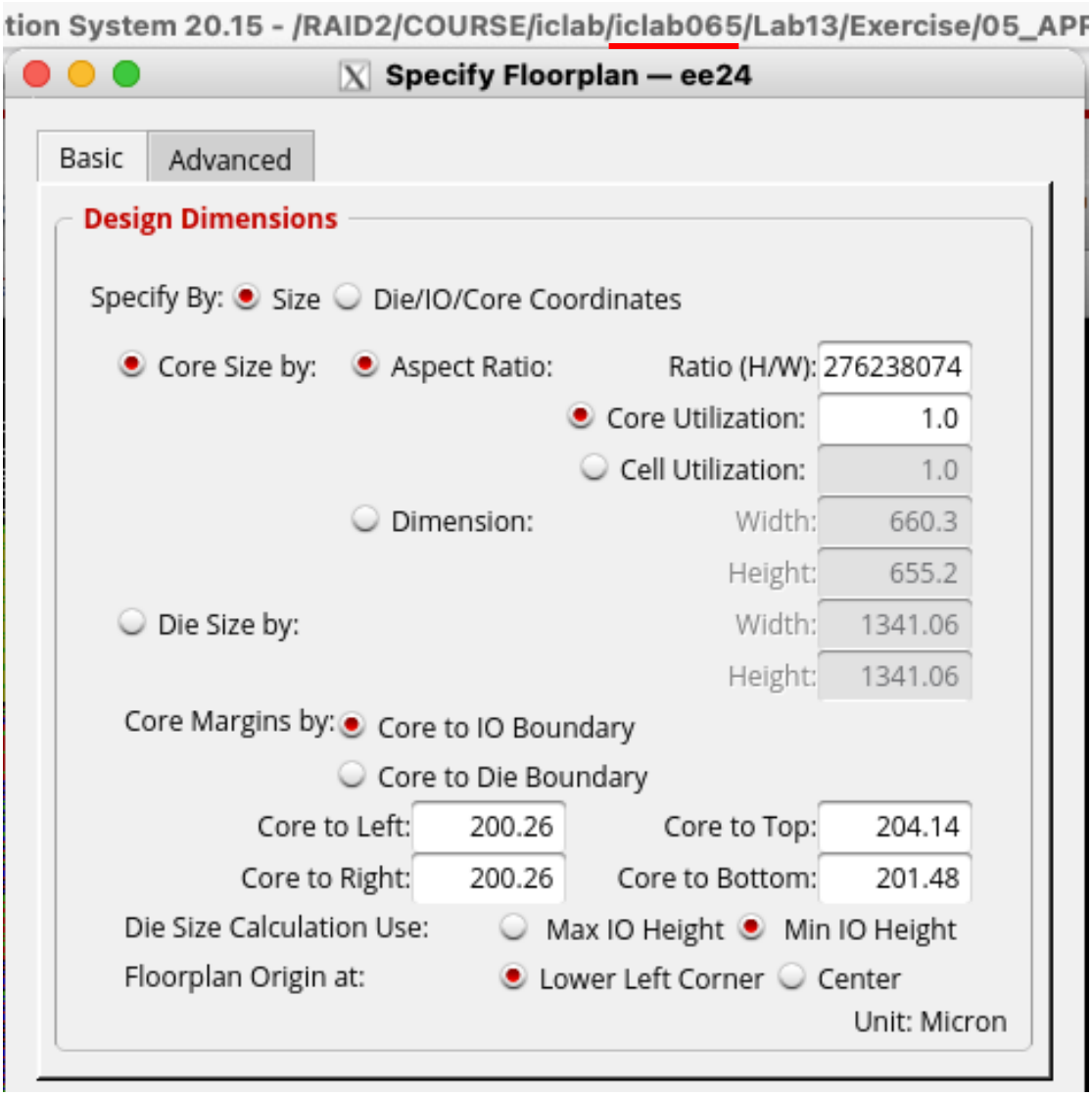
1. Chip Layout View :




Innovus(TM) Implementation System 20.15 - /RAID2/COURSE/iclab/iclab065/Lab13/Exercise/05_APR/
ECO Clock Route Timing Verify Pegasus Tools Windows Flows Help
topleft
topright
bottomleft
bottomright
VDDC8
GNDC8
VDDC0
GNDC0
VDDP0
I_CLK
GNDP0
VDDC1
GNDC1
VDDC9
GNDC9
GNDC12
GNDC10
GNDC5
GNDC3
VDDC5
VDDC3
GNDC7
GNDP1
VDDC7
O_CODE
GNDP3
O_VALID
I_RST_N
VDDP1
VDDP3
GNDC2
GNDC6
VDDC2
VDDC6
VDDC10
VDDC12
VDDC11
VDDC4
VDDP2
I_IN_VALID
...T_MODE
...EIGHT_0
...EIGHT_1
...EIGHT_2
GNDP2
GNDC4
GNDC11

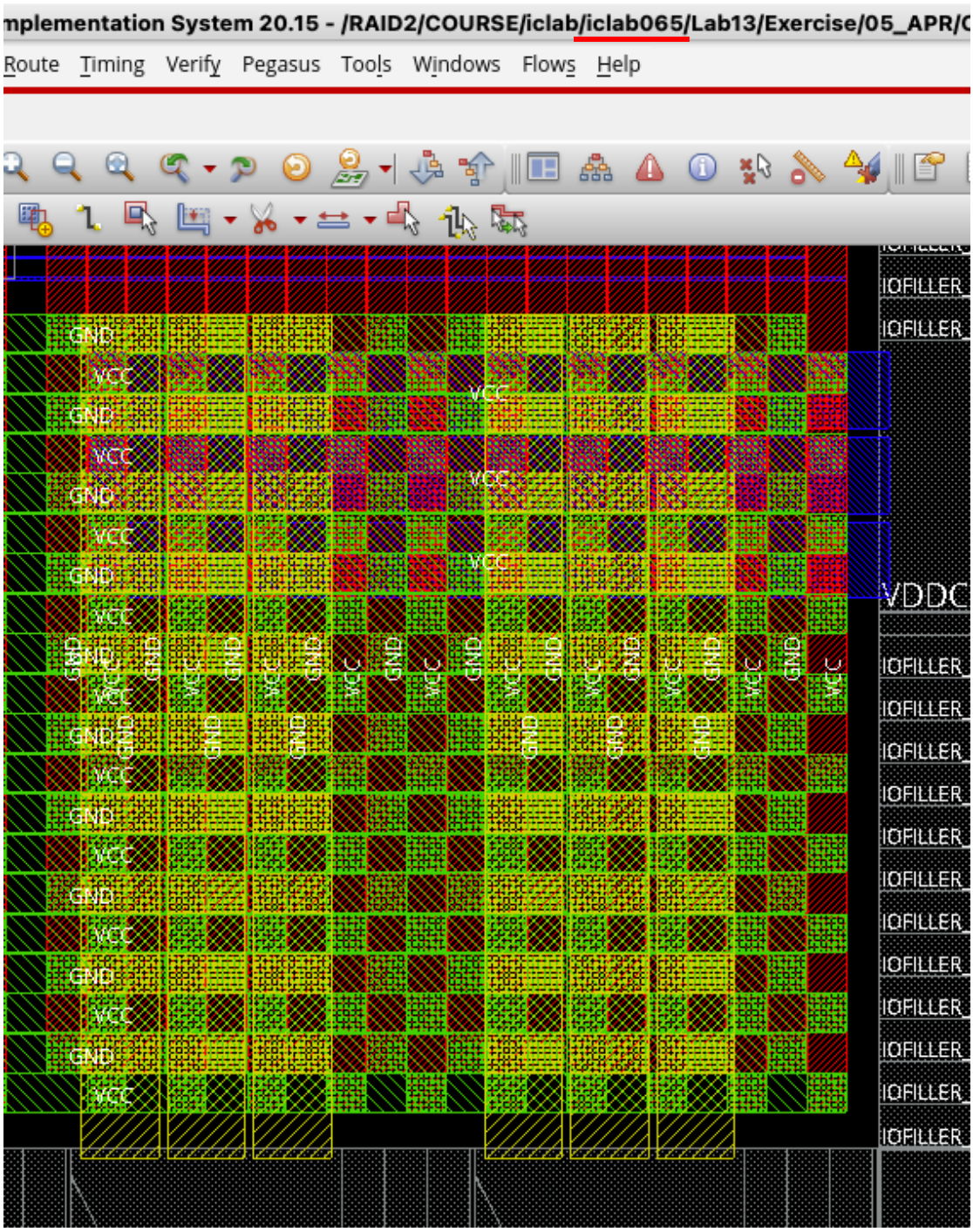

Innovus(TM) Implementation System 20.15 - /RAID2/COURSE/iclab/iclab065/Lab13/Exercise/05_APR
ECO Clock Route Timing Verify Pegasus Tools Windows Flows Help
topleft
VDDC8
GNDC8
VDDC0
GNDC0
VDDP0
I_CLK
GNDP0
VDDC1
GNDC1
VDDC9
GNDC9
topright
GNDC12
GNDC5
VDDC5
GNDC7
VDDC7
GNDP3
I_RST_N
VDDP3
GNDC6
VDDC6
VDDC12
CORE
GNDC10
GNDC3
VDDC3
GNDP1
O_CODE
O_VALID
VDDP1
GNDC2
VDDC2
VDDC10
bottomleft
VDDC11
VDDC4
VDDP2
I_IN_VALID
...T_MODE
...EIGHT_0
...EIGHT_1
...EIGHT_2
GNDP2
GNDC4
GNDC11
...tomright

2. Core to IO boundary :

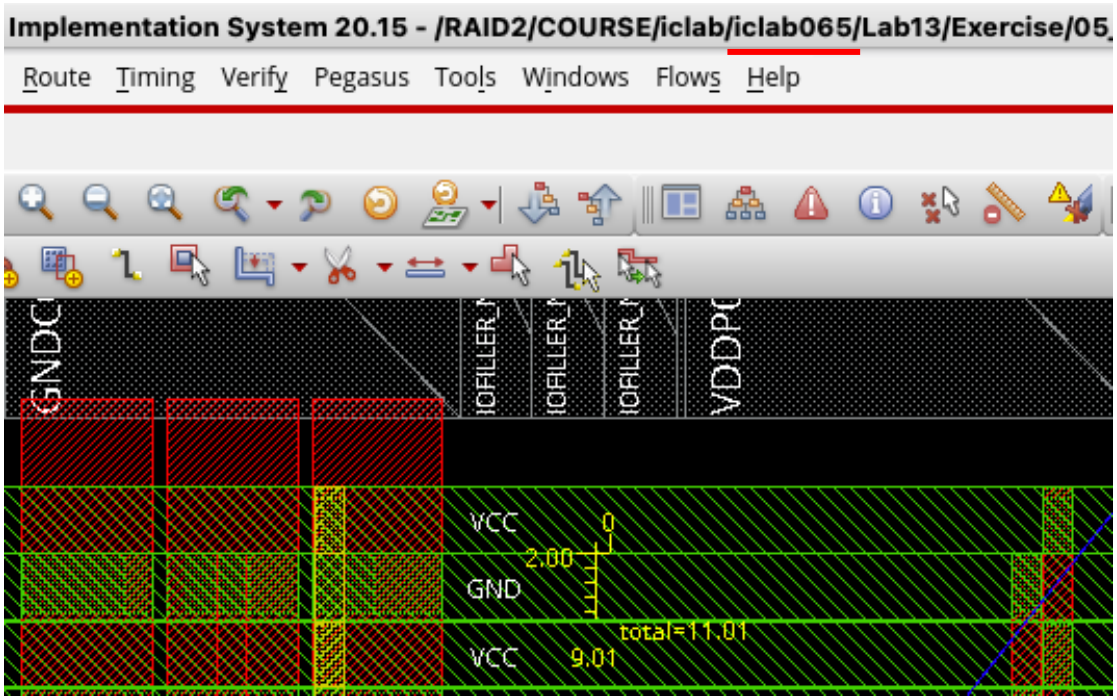


3. Core Ring :

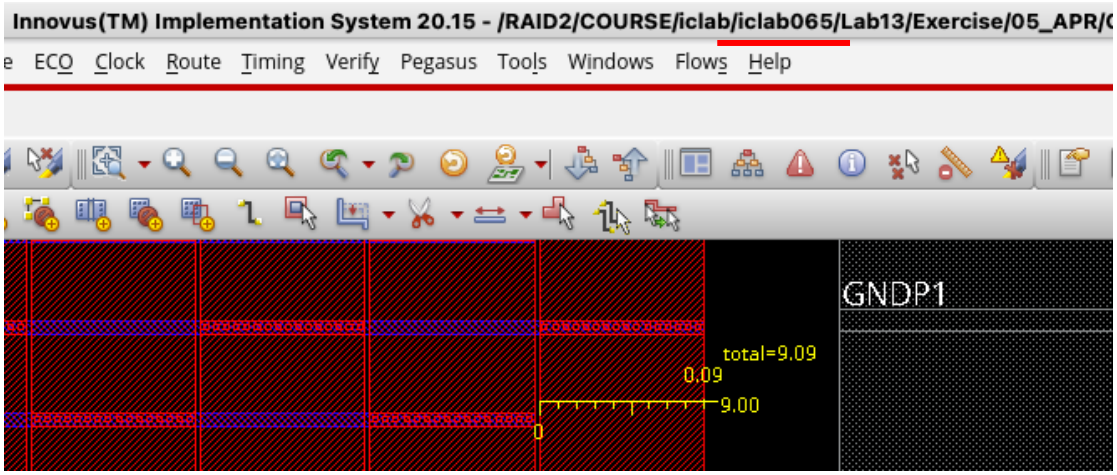
10 pairs & interleaving power ring



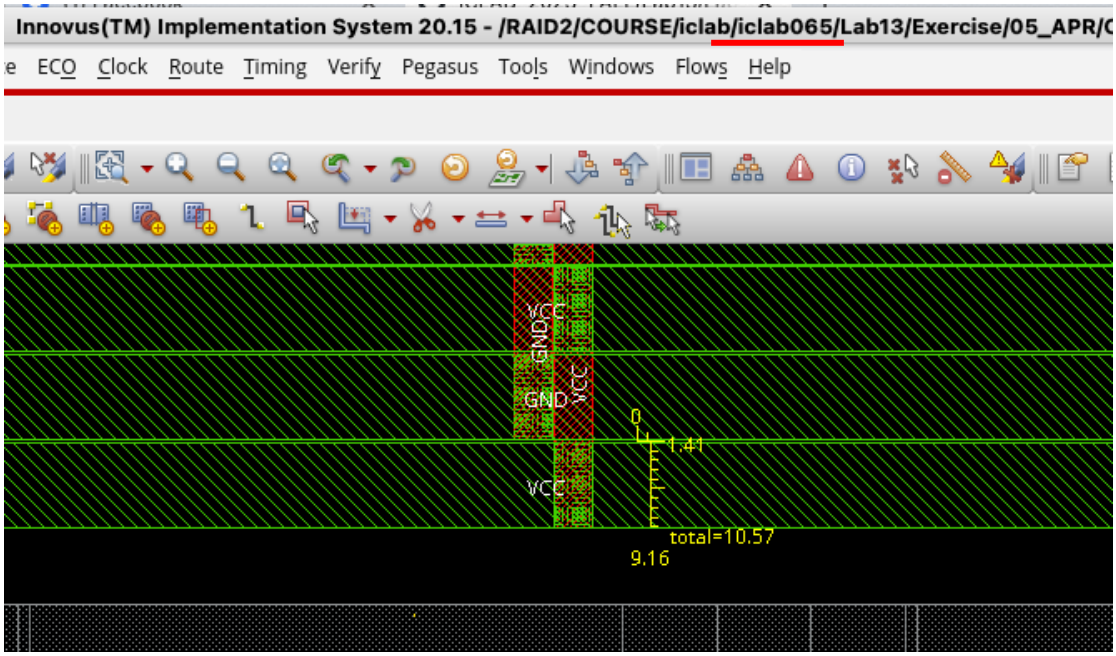
Top


Implementation System 20.15 - /RAID2/COURSE/iclab/iclab065/Lab13/Exercise/05_
Route Timing Verify Pegasus Tools Windows Flows Help
VCC
0
2.00
GND
total=11.01
VCC
9.01

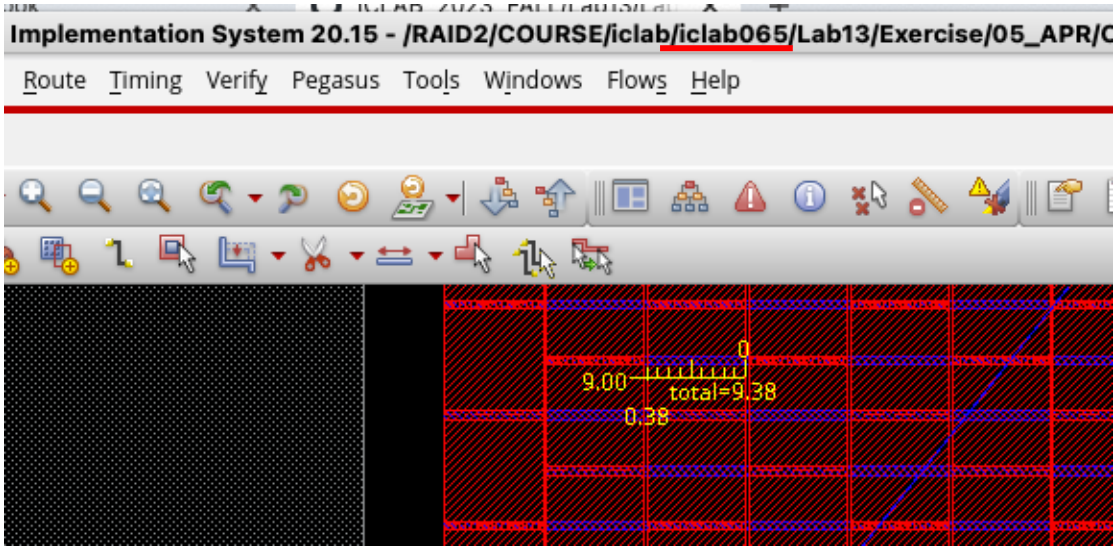
Right


Innovus(TM) Implementation System 20.15 - /RAID2/COURSE/iclab/iclab065/Lab13/Exercise/05_APR/
e ECO Clock Route Timing Verify Pegasus Tools Windows Flows Help
GNDP1
total=9.09
0.09
9.00
0

Bottom

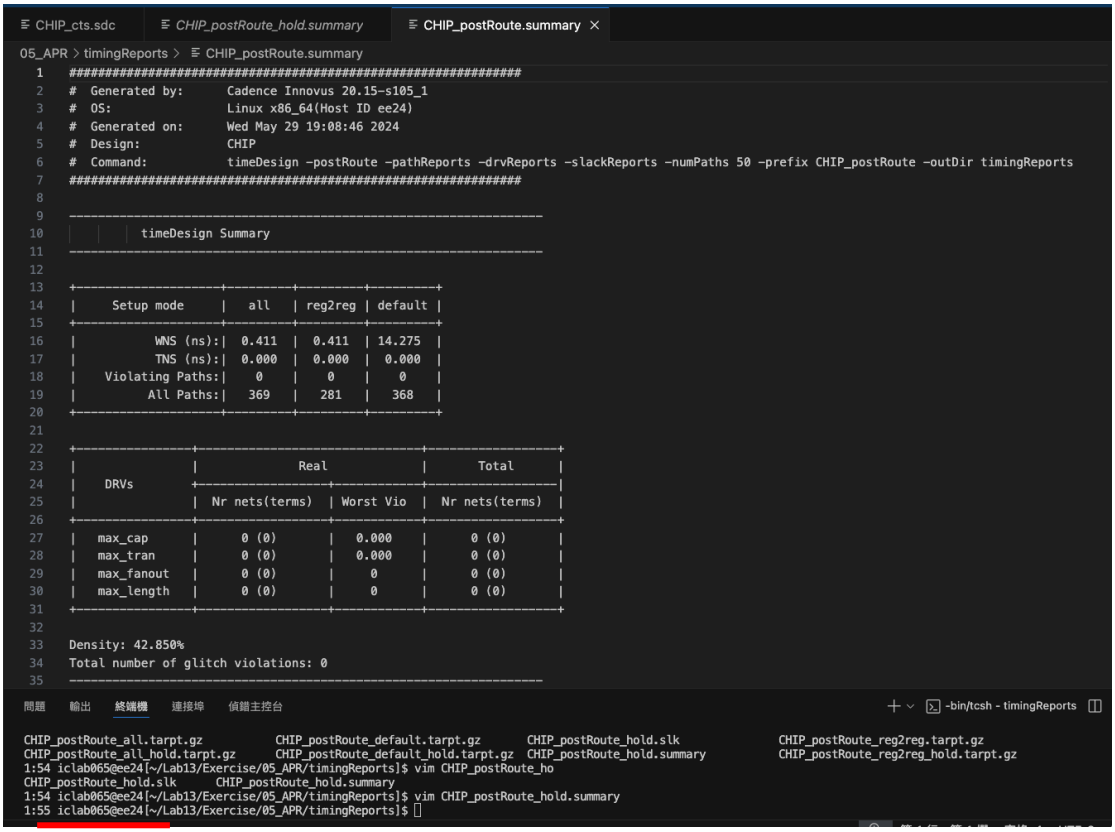


Left

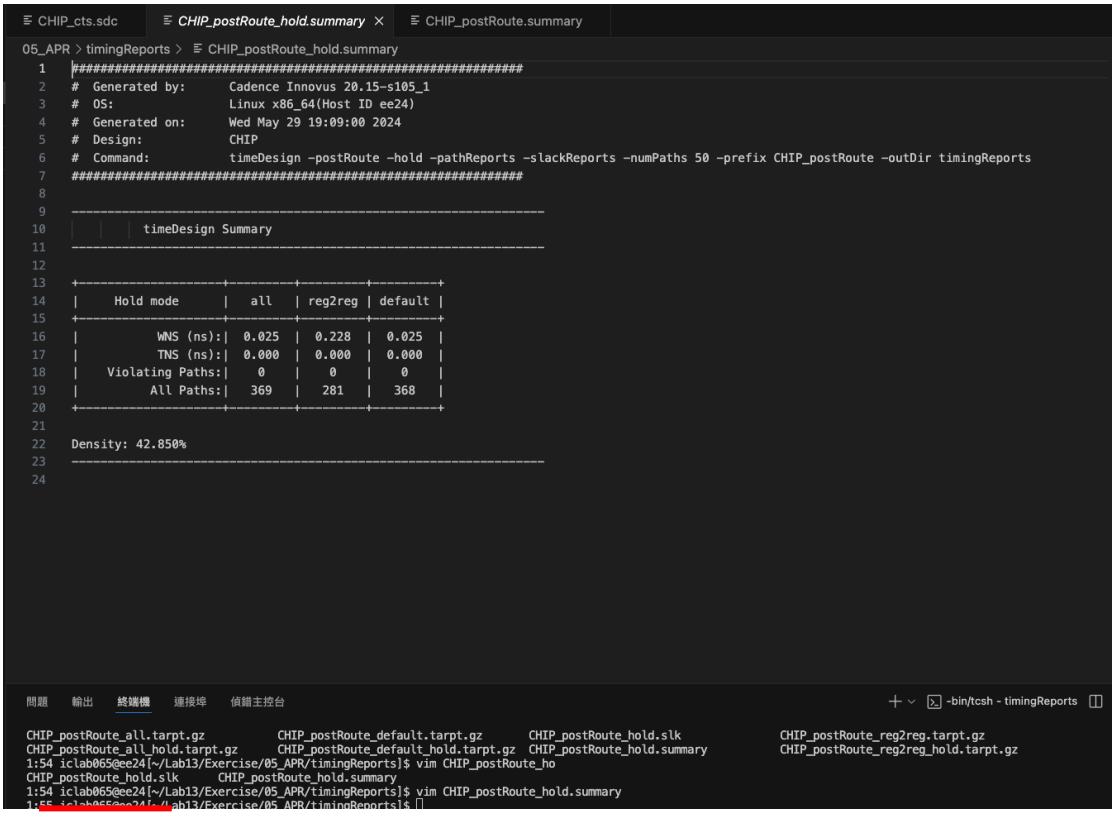


(Width settings are all 9)

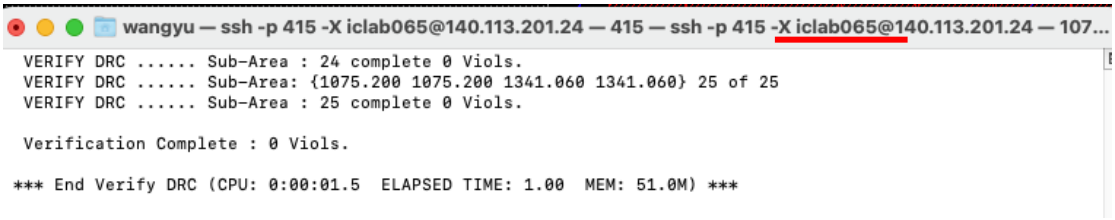
4. Post-Route setup time analysis :



5. Post-Route hold time analysis :

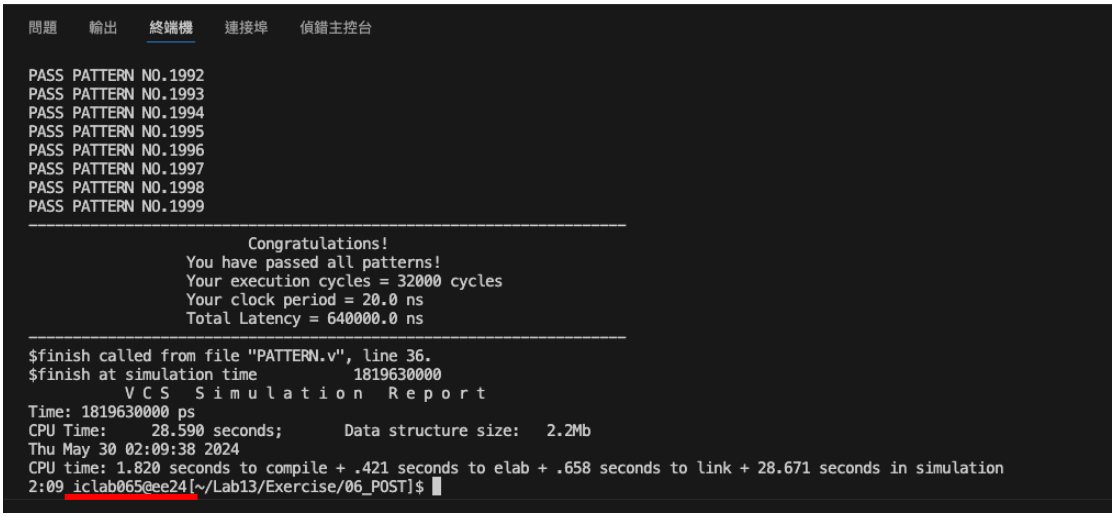


6. DRC result :

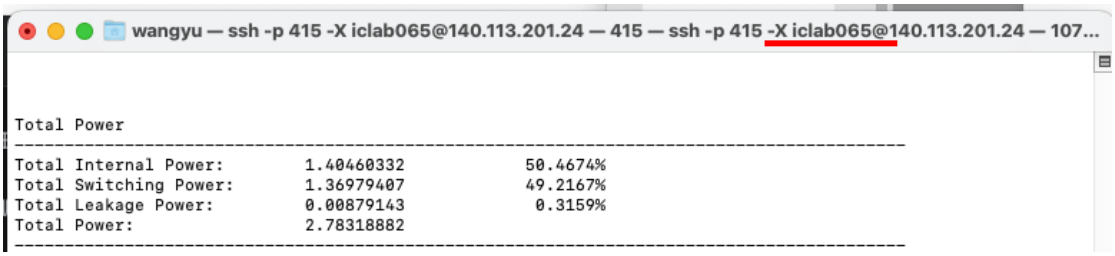


7. LVS result :

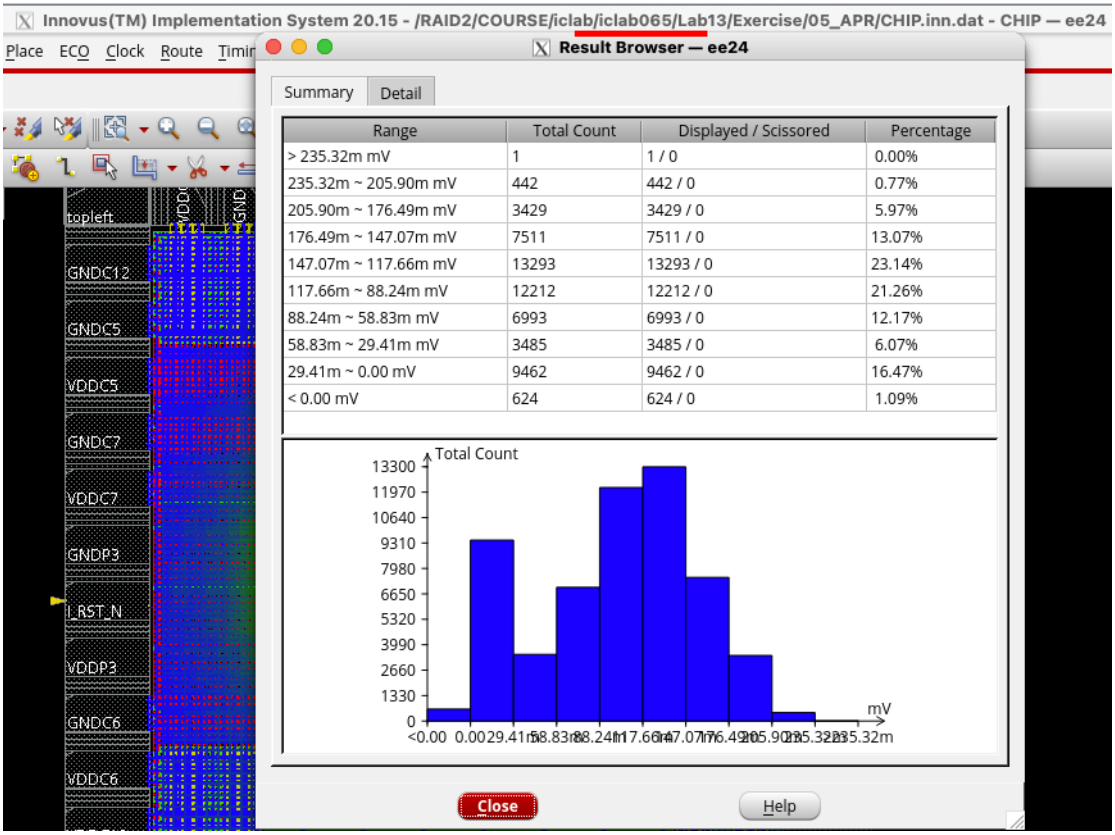
8. Post Layout simulation result :

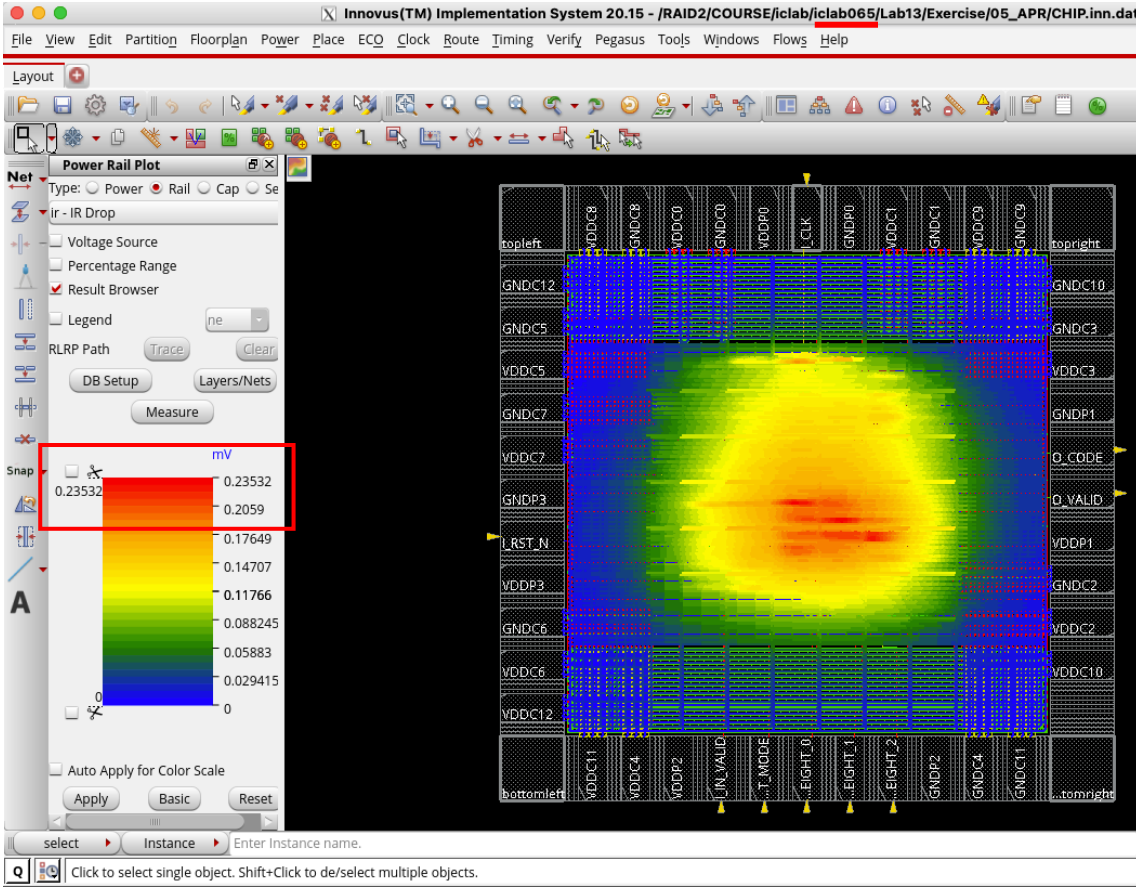


9. Power result :



10. IR Drop Results :





Method :

IR drop refers to the voltage reduction that happens as current travels through a conductor. It follows Ohm's Law (V = IR), where V is voltage, I is current, and R is resistance. In simpler terms, some voltage is "lost" due to the resistance of the wires.

To cope with this problem, I placed 13 sets of core power pads and set up tighter stripes.

These methods worked very well and the final IR drop was less than 0.25mV.