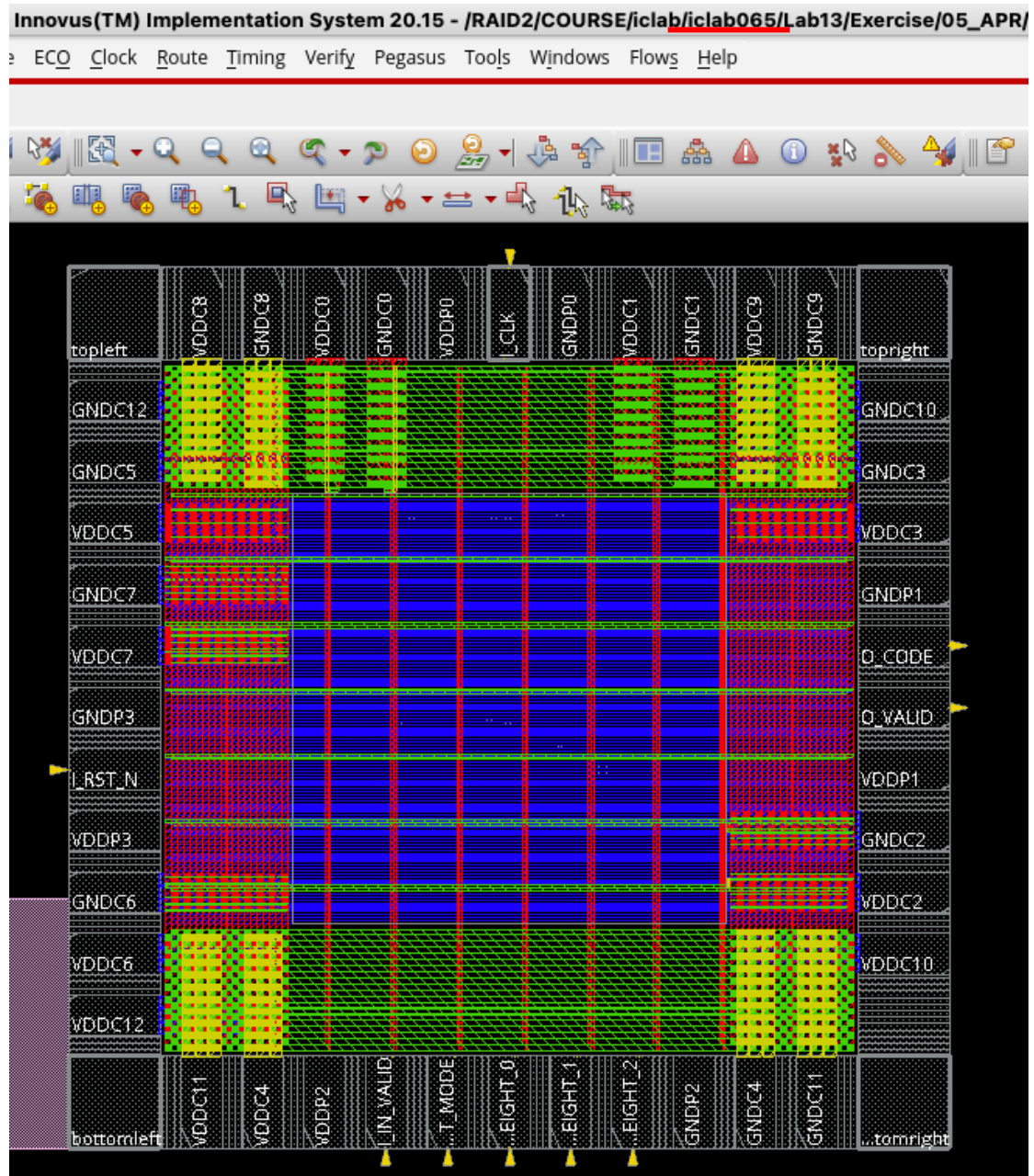
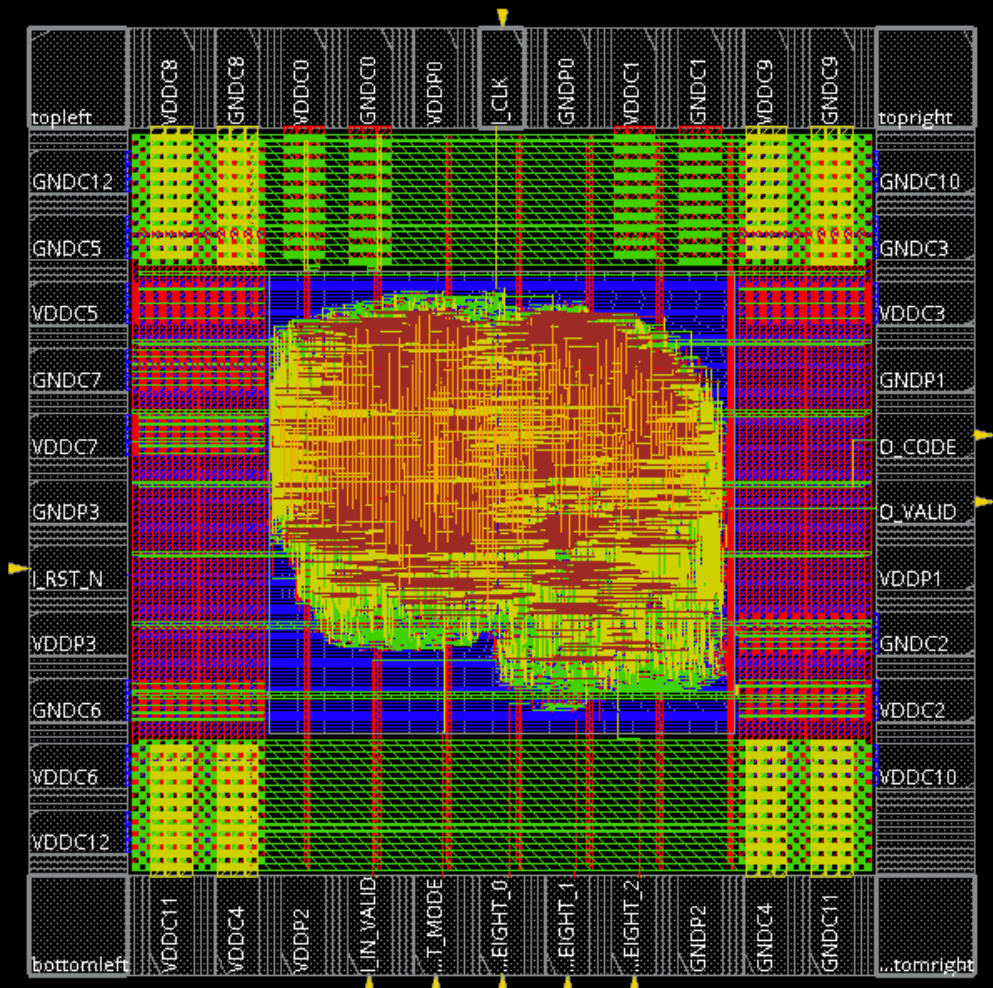
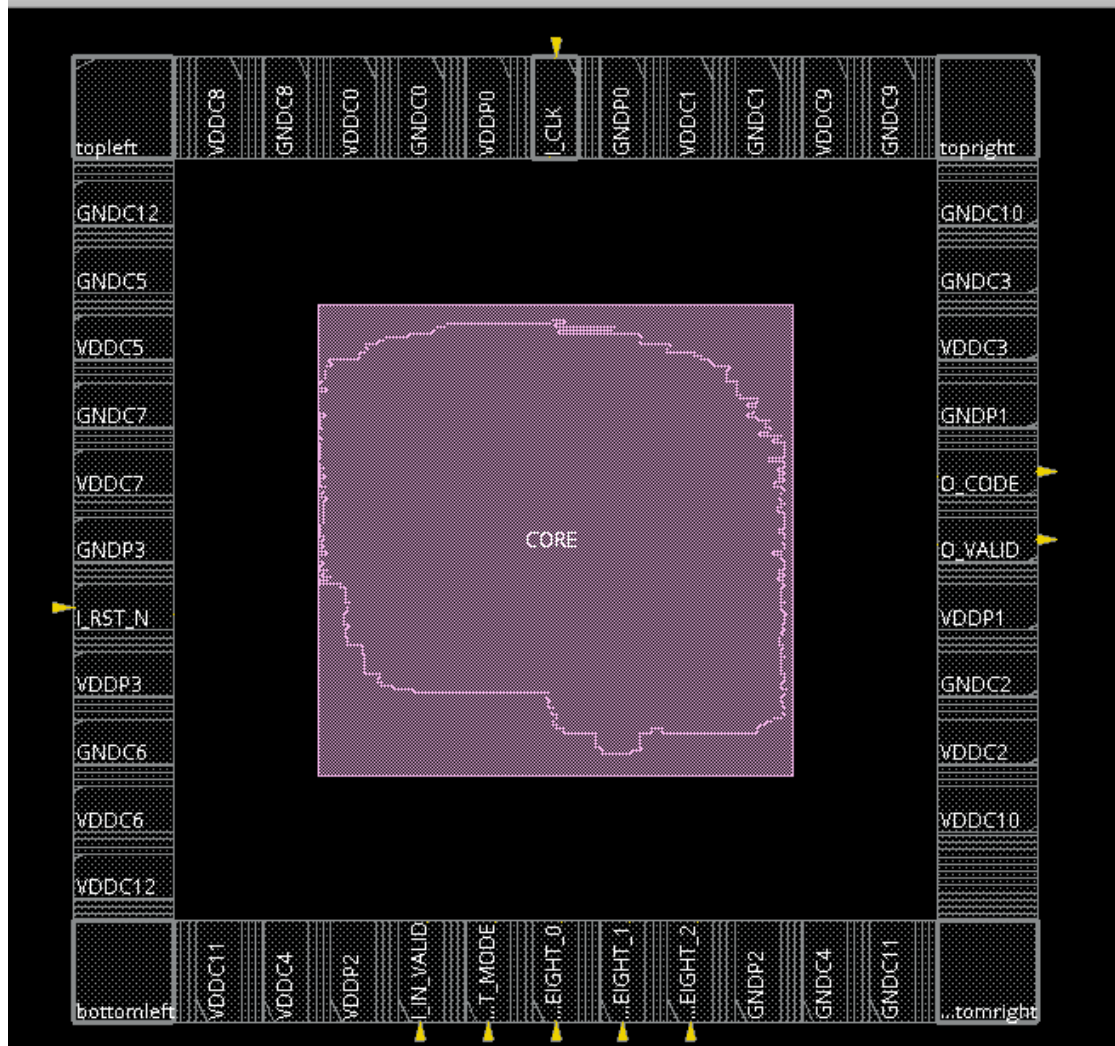


Report

1. Chip Layout View :







2. Core to IO boundary :

tion System 20.15 - /RAID2/COURSE/iclab/iclab065/Lab13/Exercise/05_APP

Specify Floorplan — ee24

Basic Advanced

Design Dimensions

Specify By: ☒ Size ☐ Die/IO/Core Coordinates

☒ Core Size by: ☒ Aspect Ratio: Ratio (H/W): 276238074

☒ Core Utilization: 1.0

☐ Cell Utilization: 1.0

☐ Dimension: Width: 660.3

Height: 655.2

☐ Die Size by: Width: 1341.06

Height: 1341.06

Core Margins by: ☒ Core to IO Boundary

☐ Core to Die Boundary

Core to Left: 200.26 Core to Top: 204.14

Core to Right: 200.26 Core to Bottom: 201.48

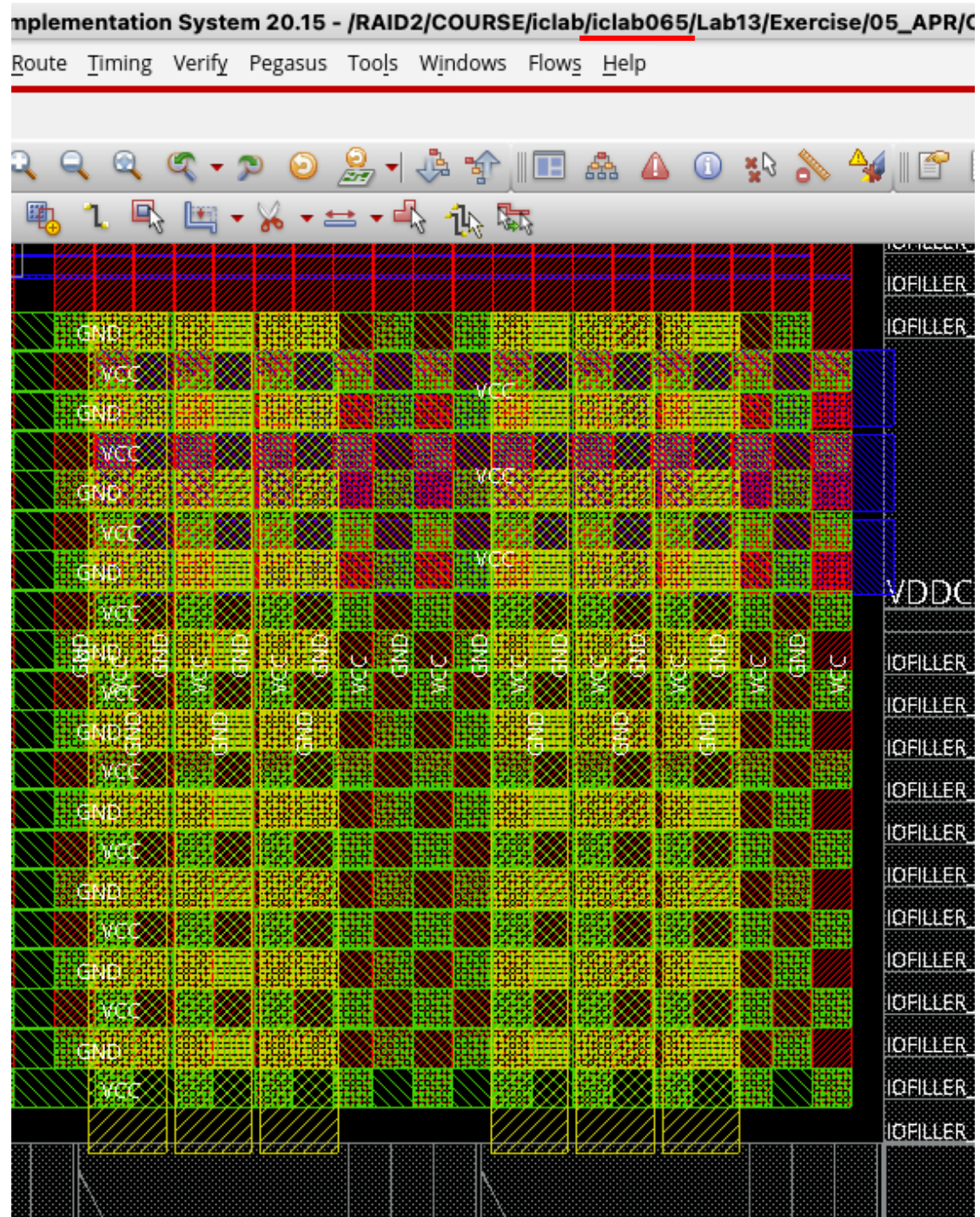
Die Size Calculation Use: ☐ Max IO Height ☒ Min IO Height

Floorplan Origin at: ☒ Lower Left Corner ☐ Center

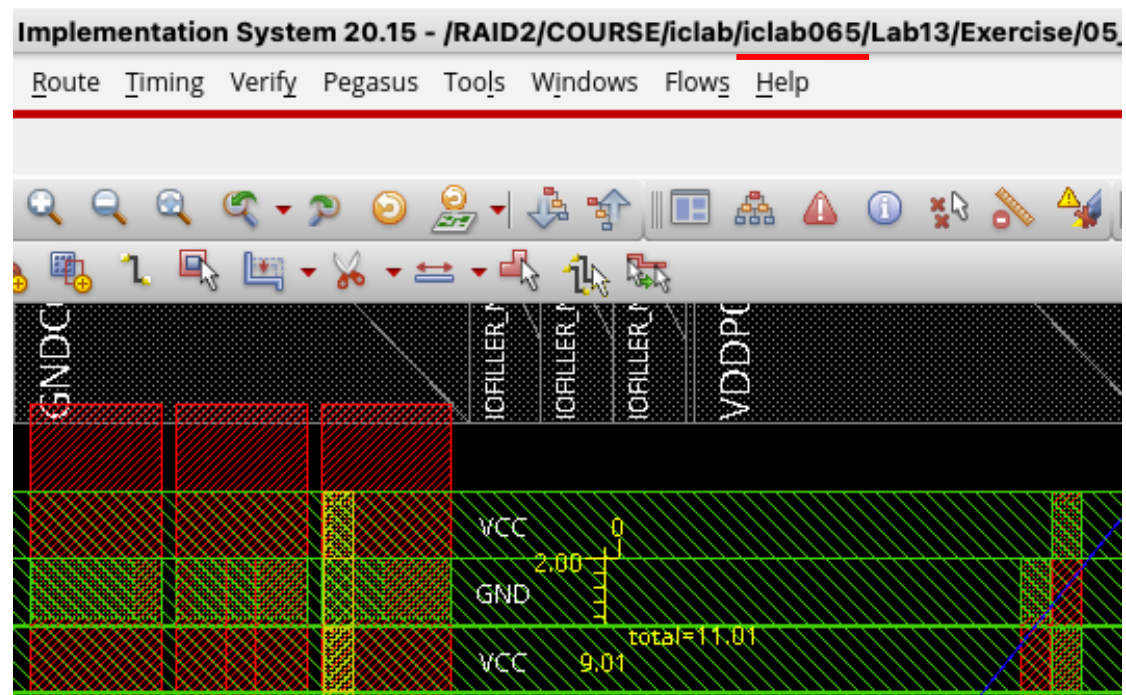
Unit: Micron

3. Core Ring :

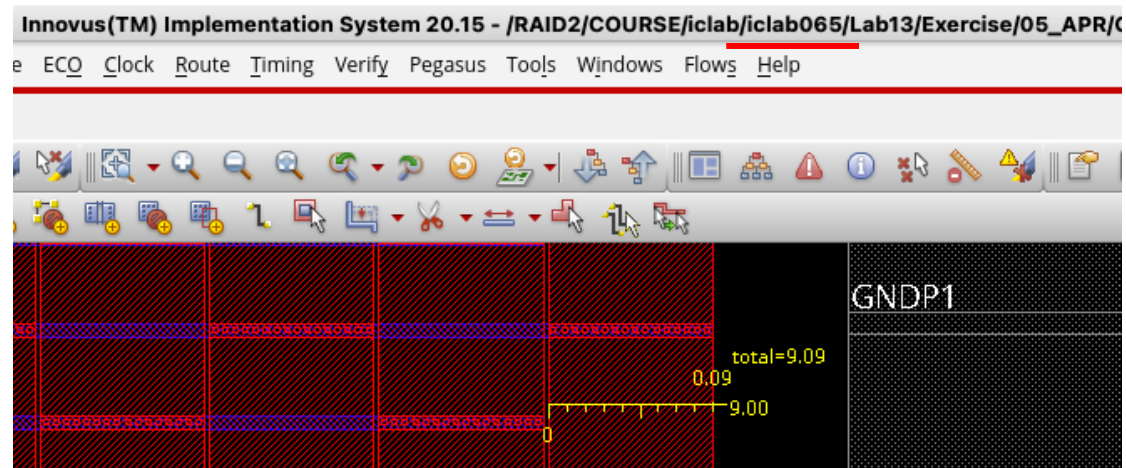
10 pairs & interleaving power ring



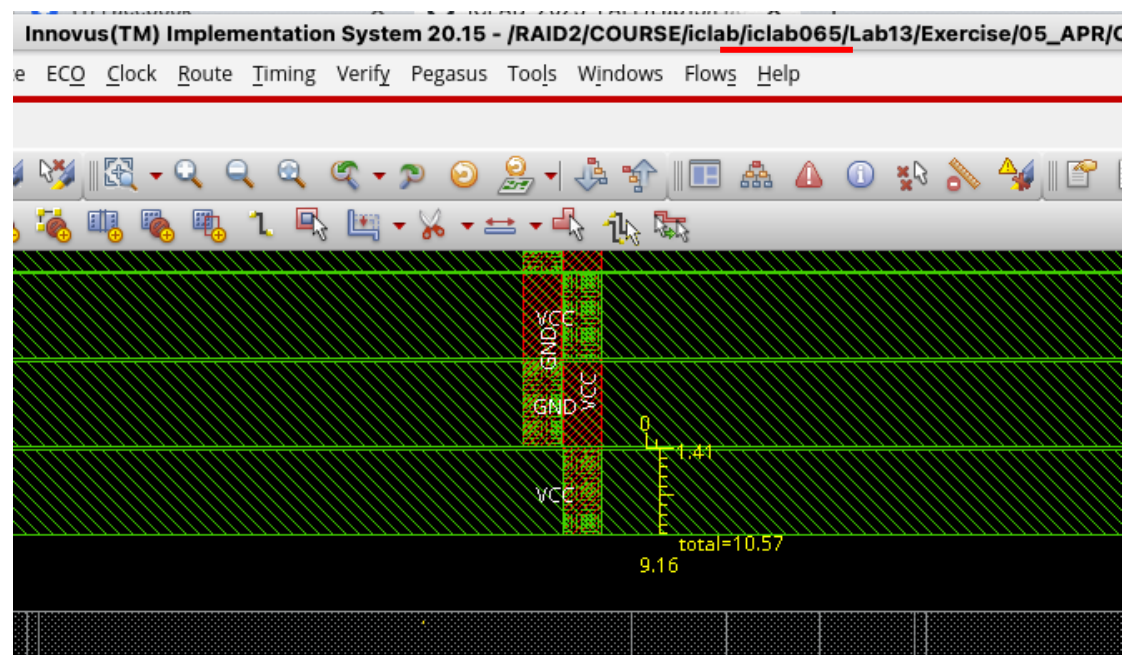
Top



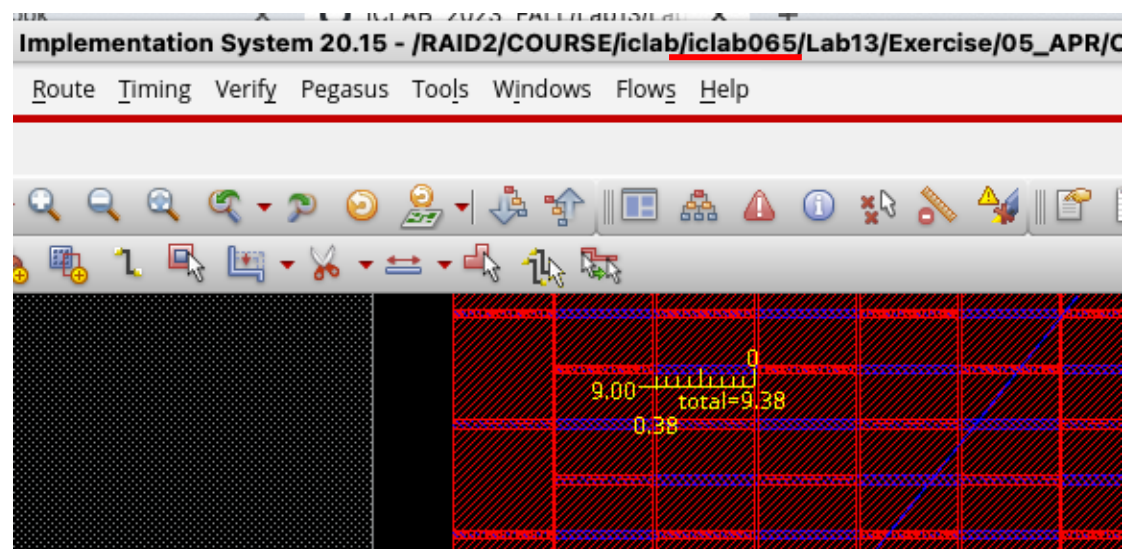
Right



Bottom



Left



(Width settings are all 9)

4. Post-Route setup time analysis :

```
CHIP_cts.sdc  CHIP_postRoute_hold.summary  CHIP_postRoute.summary X
05_APR > timingReports > CHIP_postRoute.summary
1 #####
2 # Generated by: Cadence Innovus 20.15-s105_1
3 # OS: Linux x86_64(Host ID ee24)
4 # Generated on: Wed May 29 19:08:46 2024
5 # Design: CHIP
6 # Command: timeDesign -postRoute -pathReports -drvReports -slackReports -numPaths 50 -prefix CHIP_postRoute -outDir timingReports
7 #####
8
9
10 | | timeDesign Summary
11 |-----|
12
13 |-----|
14 | Setup mode | all | reg2reg | default |
15 |-----|
16 | WNS (ns): | 0.411 | 0.411 | 14.275 |
17 | TNS (ns): | 0.000 | 0.000 | 0.000 |
18 | Violating Paths: | 0 | 0 | 0 |
19 | All Paths: | 369 | 281 | 368 |
20 |-----|
21
22 |-----|
23 | | Real | Total |
24 | |-----|-----|
25 | | Nr nets(terms) | Worst Vio | Nr nets(terms) |
26 |-----|-----|
27 | max_cap | 0 (0) | 0.000 | 0 (0) |
28 | max_tran | 0 (0) | 0.000 | 0 (0) |
29 | max_fanout | 0 (0) | 0 | 0 (0) |
30 | max_length | 0 (0) | 0 | 0 (0) |
31 |-----|-----|
32
33 Density: 42.850%
34 Total number of glitch violations: 0
35
-----
問題 輸出 終端機 連接埠 偵錯主控台 + v -bin/tcsh - timingReports []
CHIP_postRoute_all.tarpt.gz CHIP_postRoute_default.tarpt.gz CHIP_postRoute_hold.slk CHIP_postRoute_reg2reg.tarpt.gz
CHIP_postRoute_all_hold.tarpt.gz CHIP_postRoute_default_hold.tarpt.gz CHIP_postRoute_hold.summary CHIP_postRoute_reg2reg_hold.tarpt.gz
1:54 iclab065@ee24[~/Lab13/Exercise/05_APR/timingReports]$ vim CHIP_postRoute_hold.slk CHIP_postRoute_hold.summary
1:54 iclab065@ee24[~/Lab13/Exercise/05_APR/timingReports]$ vim CHIP_postRoute_hold.summary
1:55 iclab065@ee24[~/Lab13/Exercise/05_APR/timingReports]$
```

5. Post-Route hold time analysis :

```
CHIP_cts.sdc  CHIP_postRoute_hold.summary X  CHIP_postRoute.summary
05_APR > timingReports > CHIP_postRoute_hold.summary
1 #####
2 # Generated by: Cadence Innovus 20.15-s105_1
3 # OS: Linux x86_64(Host ID ee24)
4 # Generated on: Wed May 29 19:09:00 2024
5 # Design: CHIP
6 # Command: timeDesign -postRoute -hold -pathReports -slackReports -numPaths 50 -prefix CHIP_postRoute -outDir timingReports
7 #####
8
9
10 | | timeDesign Summary
11 |-----|
12
13 |-----|
14 | Hold mode | all | reg2reg | default |
15 |-----|
16 | WNS (ns): | 0.025 | 0.228 | 0.025 |
17 | TNS (ns): | 0.000 | 0.000 | 0.000 |
18 | Violating Paths: | 0 | 0 | 0 |
19 | All Paths: | 369 | 281 | 368 |
20 |-----|
21
22 Density: 42.850%
23
24
-----
問題 輸出 終端機 連接埠 偵錯主控台 + v -bin/tcsh - timingReports []
CHIP_postRoute_all.tarpt.gz CHIP_postRoute_default.tarpt.gz CHIP_postRoute_hold.slk CHIP_postRoute_reg2reg.tarpt.gz
CHIP_postRoute_all_hold.tarpt.gz CHIP_postRoute_default_hold.tarpt.gz CHIP_postRoute_hold.summary CHIP_postRoute_reg2reg_hold.tarpt.gz
1:54 iclab065@ee24[~/Lab13/Exercise/05_APR/timingReports]$ vim CHIP_postRoute_hold.slk CHIP_postRoute_hold.summary
1:54 iclab065@ee24[~/Lab13/Exercise/05_APR/timingReports]$ vim CHIP_postRoute_hold.summary
1:55 iclab065@ee24[~/Lab13/Exercise/05_APR/timingReports]$
```


6. DRC result :

```
wangyu — ssh -p 415 -X iclab065@140.113.201.24 — 415 — ssh -p 415 -X iclab065@140.113.201.24 — 107...  
VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.  
VERIFY DRC ..... Sub-Area: {1075.200 1075.200 1341.060 1341.060} 25 of 25  
VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.  
  
Verification Complete : 0 Viols.  
  
*** End Verify DRC (CPU: 0:00:01.5 ELAPSED TIME: 1.00 MEM: 51.0M) ***
```

7. LVS result :

```
wangyu — ssh -p 415 -X iclab065@140.113.201.24 — 415 — ssh -p 415 -X iclab065@140.113.201.24 — 107...  
  
End Time: Thu May 30 02:07:42 2024  
Time Elapsed: 0:00:01.0  
  
***** End: VERIFY CONNECTIVITY *****  
Verification Complete : 0 Viols. 0 Wrngs.  
(CPU Time: 0:00:00.4 MEM: 3.000M)
```

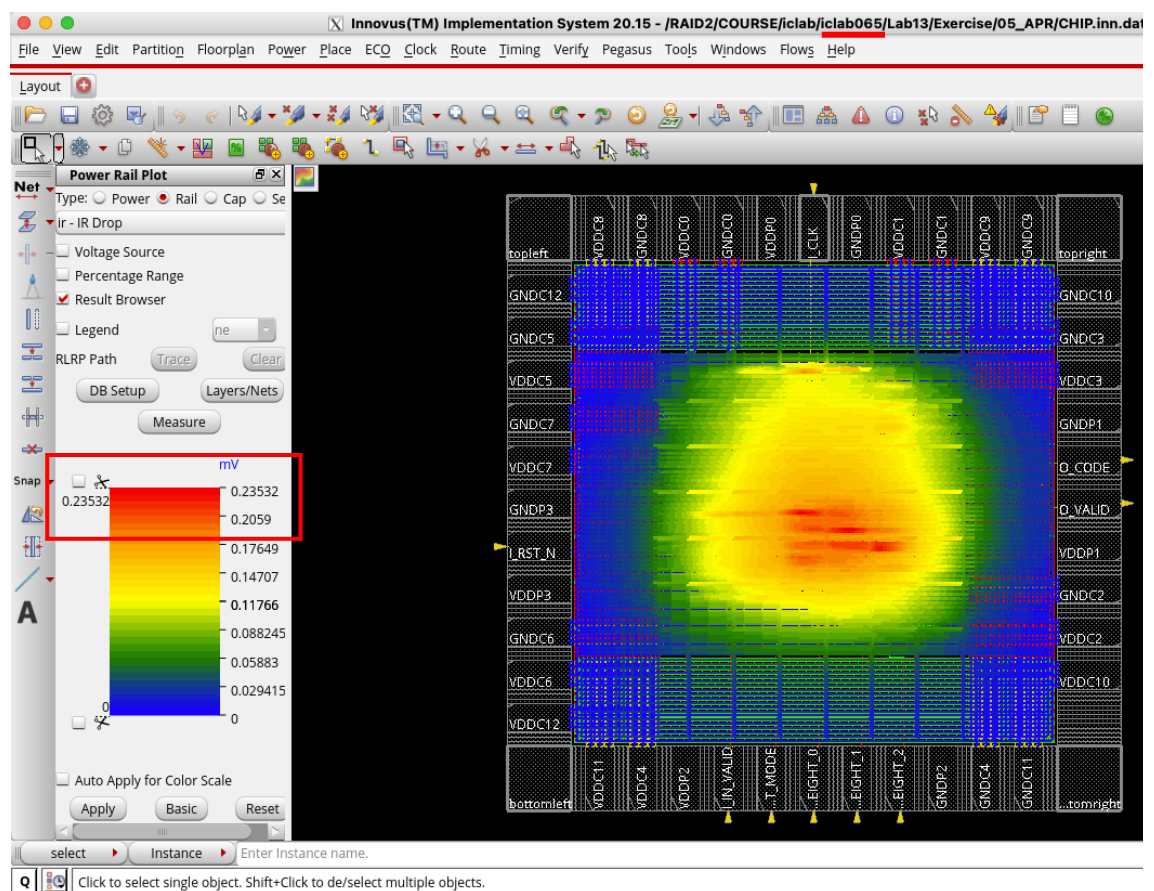
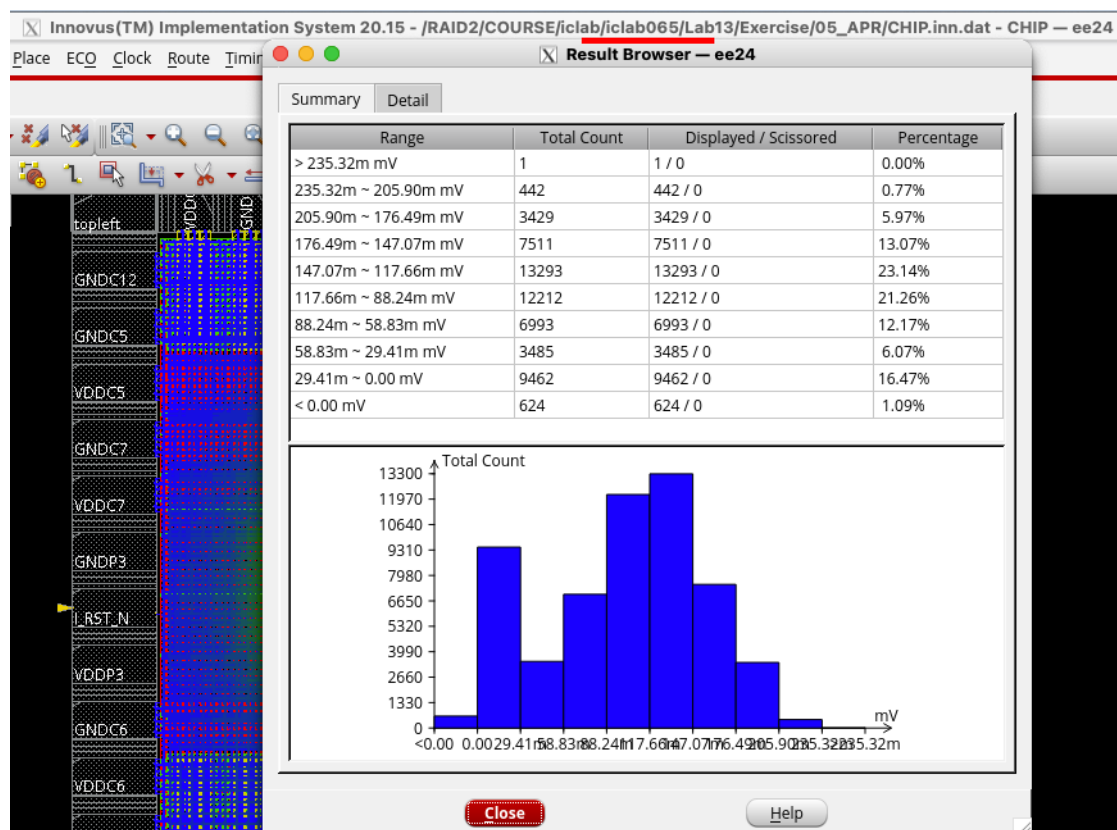
8. Post Layout simulation result :

```
問題 輸出 終端機 連接埠 偵錯主控台  
  
PASS PATTERN NO.1992  
PASS PATTERN NO.1993  
PASS PATTERN NO.1994  
PASS PATTERN NO.1995  
PASS PATTERN NO.1996  
PASS PATTERN NO.1997  
PASS PATTERN NO.1998  
PASS PATTERN NO.1999  
  
-----  
Congratulations!  
You have passed all patterns!  
Your execution cycles = 32000 cycles  
Your clock period = 20.0 ns  
Total Latency = 640000.0 ns  
-----  
  
$finish called from file "PATTERN.v", line 36.  
$finish at simulation time 1819630000  
V C S Simulation Report  
Time: 1819630000 ps  
CPU Time: 28.590 seconds; Data structure size: 2.2Mb  
Thu May 30 02:09:38 2024  
CPU time: 1.820 seconds to compile + .421 seconds to elab + .658 seconds to link + 28.671 seconds in simulation  
2:09 iclab065@ee24[~/Lab13/Exercise/06_POST]$
```

9. Power result :

```
wangyu — ssh -p 415 -X iclab065@140.113.201.24 — 415 — ssh -p 415 -X iclab065@140.113.201.24 — 107...  
  
-----  
Total Power  
-----  
Total Internal Power: 1.40460332 50.4674%  
Total Switching Power: 1.36979407 49.2167%  
Total Leakage Power: 0.00879143 0.3159%  
Total Power: 2.78318882  
-----
```

10. IR Drop Results :



Method :

IR drop refers to the voltage reduction that happens as current travels through a conductor. It follows Ohm's Law ($V = IR$), where V is voltage, I is current, and R is resistance. In simpler terms, some voltage is "lost" due to the resistance of the wires.

To cope with this problem, I placed 13 sets of core power pads and set up tighter stripes.

These methods worked very well and the final IR drop was less than 0.25mV.