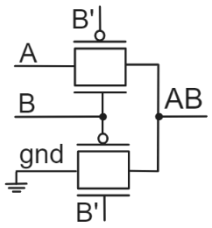
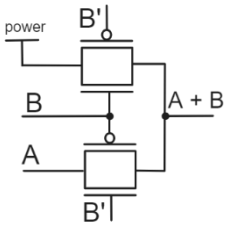
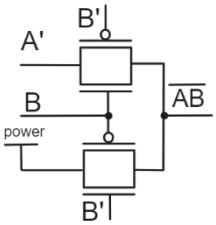
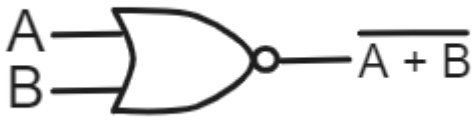
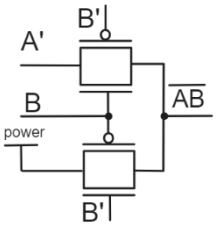
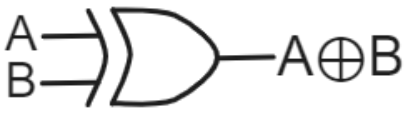
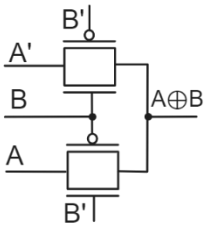
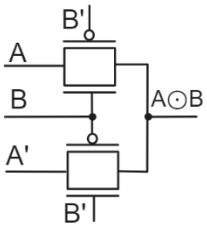
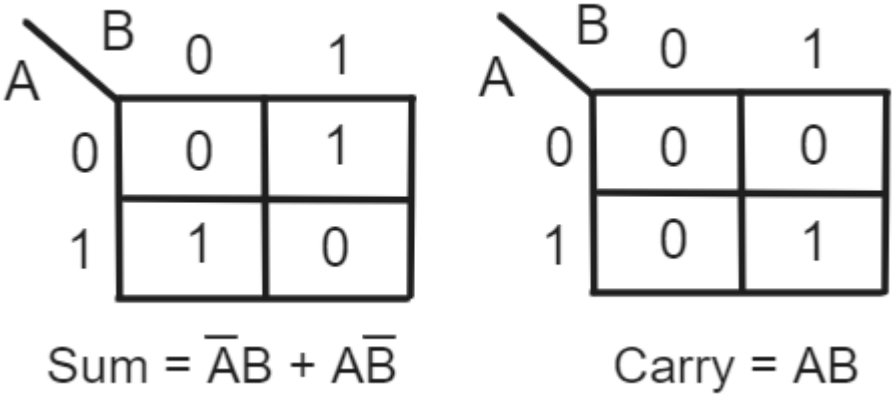
Transmission Gate(基本代換，節省 MOS 數量)

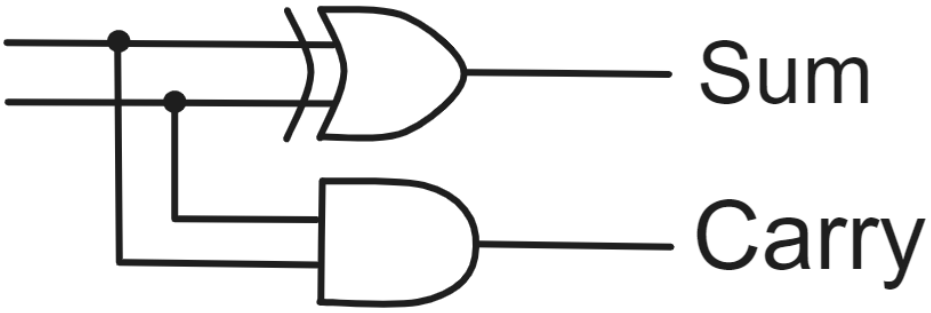
	
	
	
	
	
	

1 位元加法器/半加器(傳輸閘)

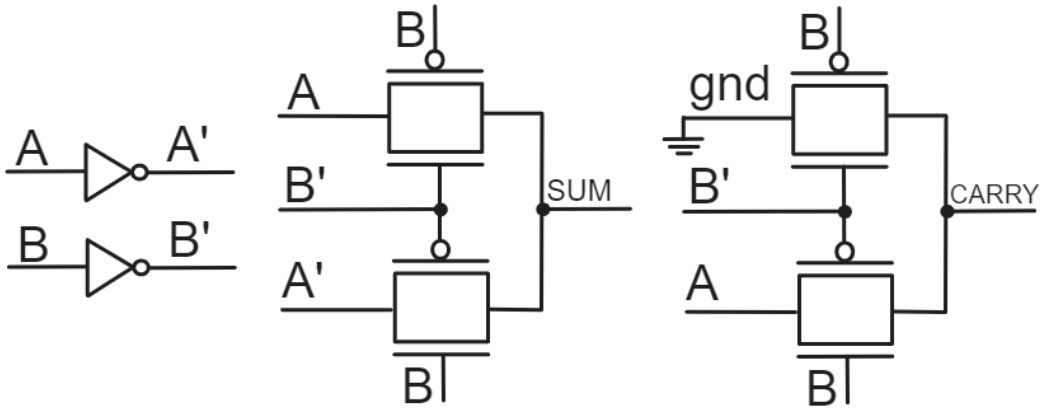
卡諾圖畫簡電路



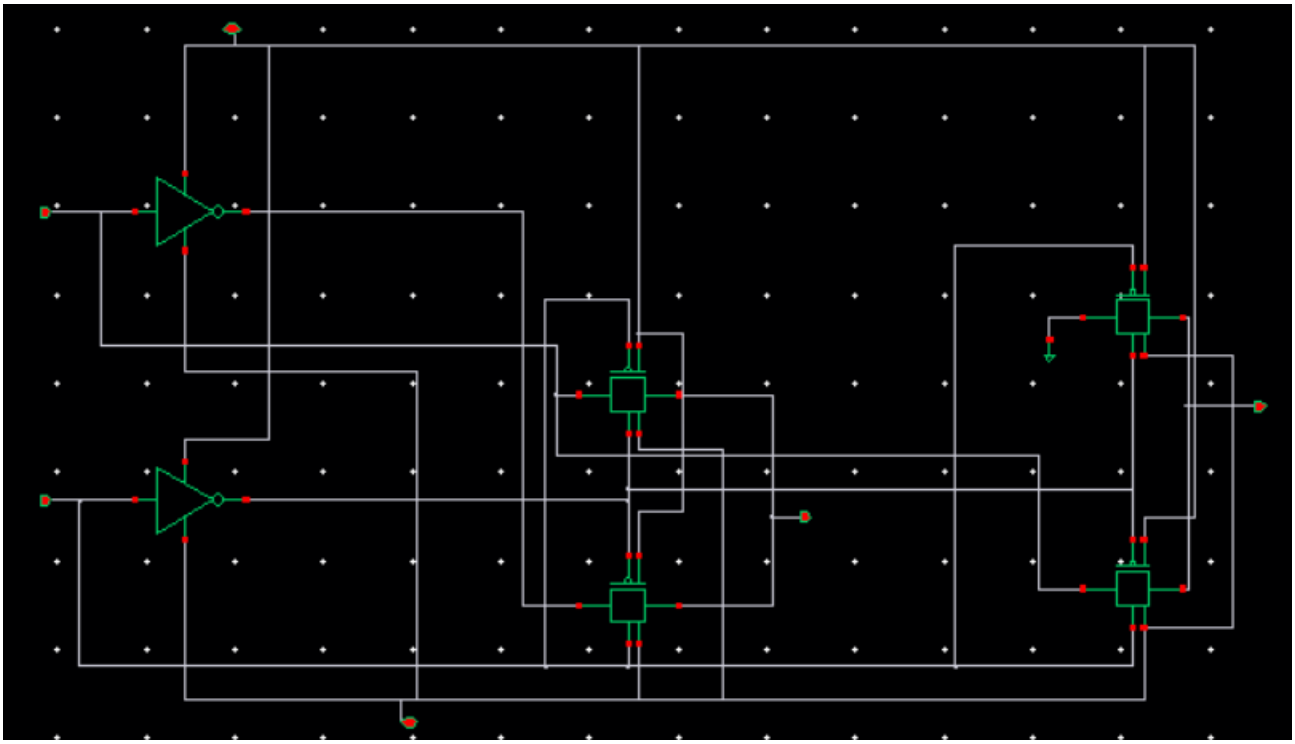
一般邏輯閘



透過 Transmission gate 進行化簡



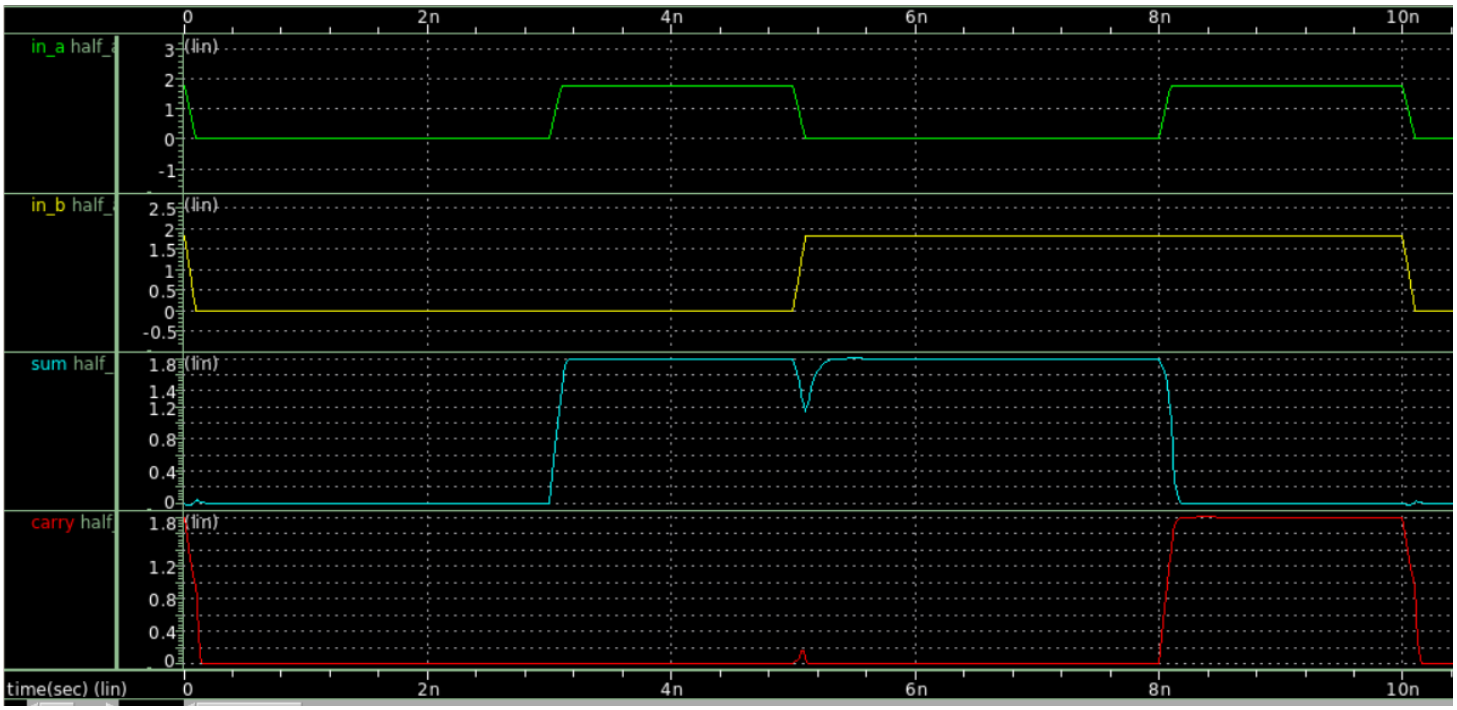
Schematic 電路



.sp 檔

```
** Library name: LOGIC
** Cell name: INV
** View name: schematic
.subckt INV in out vdd vss
m0 out in vdd vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m1 out in vss vss nch l=180e-9 w=220e-9 m=1 ad=198.4e-15 as=198.4e-15 pd=1.88e-6 ps=1.88e-6 nrd=1.40909 nrs=1.40909
.ends INV
** End of subcircuit definition.

** Library name: LOGIC
** Cell name: TRAN
** View name: schematic
.subckt TRAN intput output s sbar vdd vss
m2 intput sbar output vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m0 intput s output vss nch l=180e-9 w=220e-9 m=1 ad=198.4e-15 as=198.4e-15 pd=1.88e-6 ps=1.88e-6 nrd=1.40909 nrs=1.40909
.ends TRAN
** End of subcircuit definition.

** Library name: LOGIC
** Cell name: half_adder
** View name: schematic
xi1 in_b net2 vdd vss INV
xi0 in_a net1 vdd vss INV
xi7 0 carry net2 in_b vdd vss TRAN
xi6 in_a carry in_b net2 vdd vss TRAN
xi3 net1 sum in_b net2 vdd vss TRAN
xi2 in_a sum net2 in_b vdd vss TRAN
V0 VDD 0 1.8
V1 VSS 0 0
V2 IN_A 0 pulse 1.8 0 0n 100p 100p 2.9n 5n
V3 IN_B 0 pulse 1.8 0 0n 100p 100p 4.9n 10n

.END
```

Hspice 波形圖



2 位元加法器 (傳輸閘)

卡諾圖畫簡電路

A \ BC	00	01	11	10
0	0	1	0	1
1	1	0	1	0

A \ BC	00	01	11	10
0	0	0	1	0
1	0	1	1	1

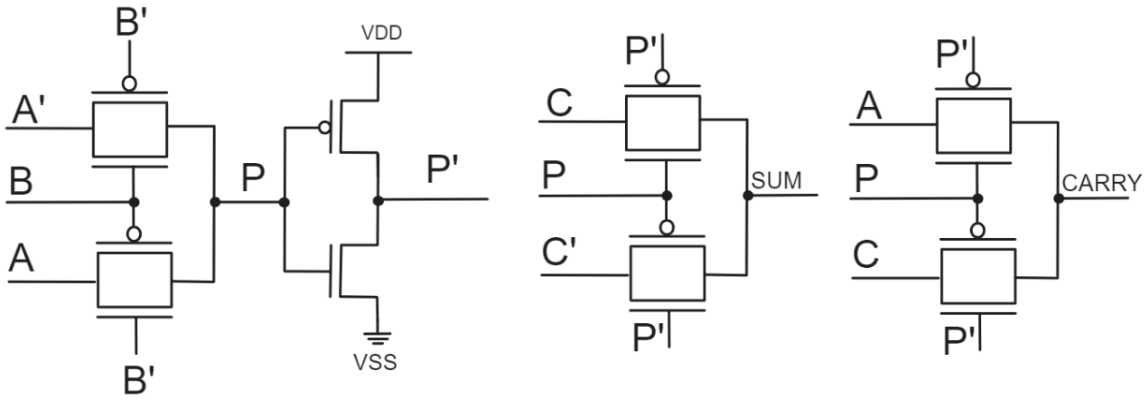
$$Sum = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$$

$$Sum = C(AB + \overline{A}\overline{B}) + C(\overline{A}B + A\overline{B})$$
$$= C(\overline{A \oplus B}) + C(A \oplus B)$$
$$= \overline{C}P + C\overline{P}$$
$$= A \oplus B \oplus C$$
$$= P \oplus C$$

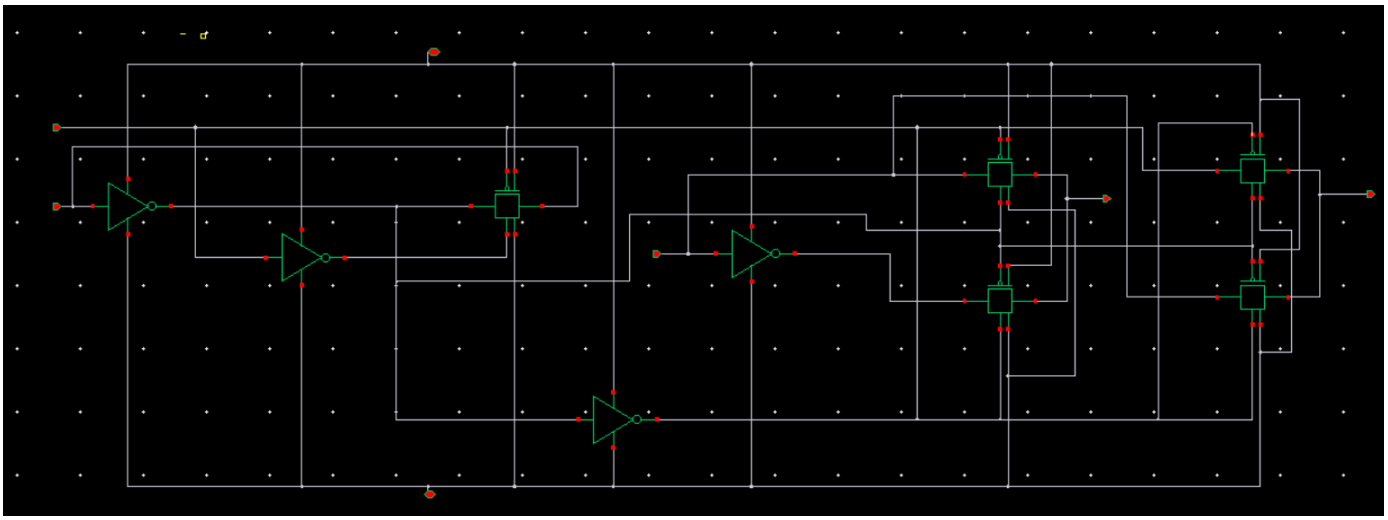
$$Carry = BC + AC + AB$$

$$Carry = AB + C(A + B)$$
$$= AB + CP$$

透過 Transmission gate 進行化簡



Schematic 電路



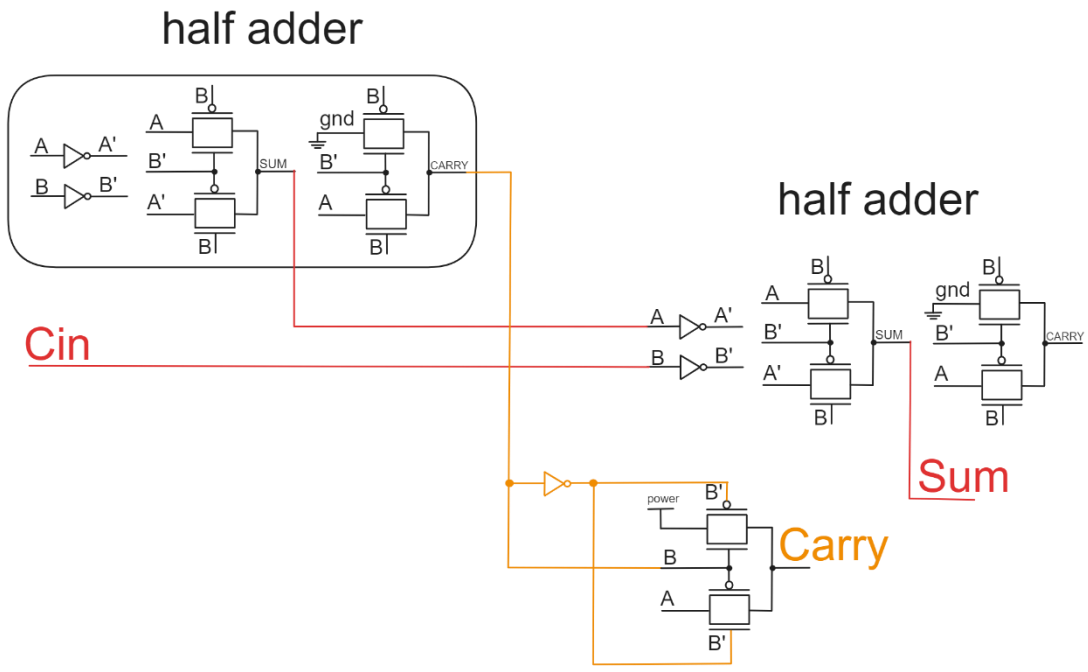
.sp 檔

```
.subckt TRAN intput output s sbar vdd vss
m2 intput sbar output vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m0 intput s output vss nch l=180e-9 w=220e-9 m=1 ad=198.4e-15 as=198.4e-15 pd=1.88e-6 ps=1.88e-6 nrd=1.40909 nrs=1.40909
.ends TRAN
** End of subcircuit definition.

** Library name: LOGIC
** Cell name: INV
** View name: schematic
.subckt INV in out vdd vss
m0 out in vdd vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m1 out in vss vss nch l=180e-9 w=220e-9 m=1 ad=198.4e-15 as=198.4e-15 pd=1.88e-6 ps=1.88e-6 nrd=1.40909 nrs=1.40909
.ends INV
** End of subcircuit definition.

** Library name: LOGIC
** Cell name: full_adder
** View name: schematic
xi21 in_a carry net1 net3 vdd vss TRAN
xi20 in_c carry net3 net1 vdd vss TRAN
xi17 in_c sum net1 net3 vdd vss TRAN
xi16 net2 sum net3 net1 vdd vss TRAN
xi12 in_a net3 net5 in_b vdd vss TRAN
xi11 net4 net3 in_b net5 vdd vss TRAN
xi18 in_c net2 vdd vss INV
xi15 net3 net1 vdd vss INV
xi14 in_b net5 vdd vss INV
xi13 in_a net4 vdd vss INV

V0 VDD 0 1.8
V1 VSS 0 0
V2 IN_A 0 pulse 1.8 0 0n 100p 100p 9.9n 20n
V3 IN_B 0 pulse 1.8 0 0n 100p 100p 4.9n 10n
V4 IN_C 0 pulse 1.8 0 0n 100p 100p 2.9n 5n
```

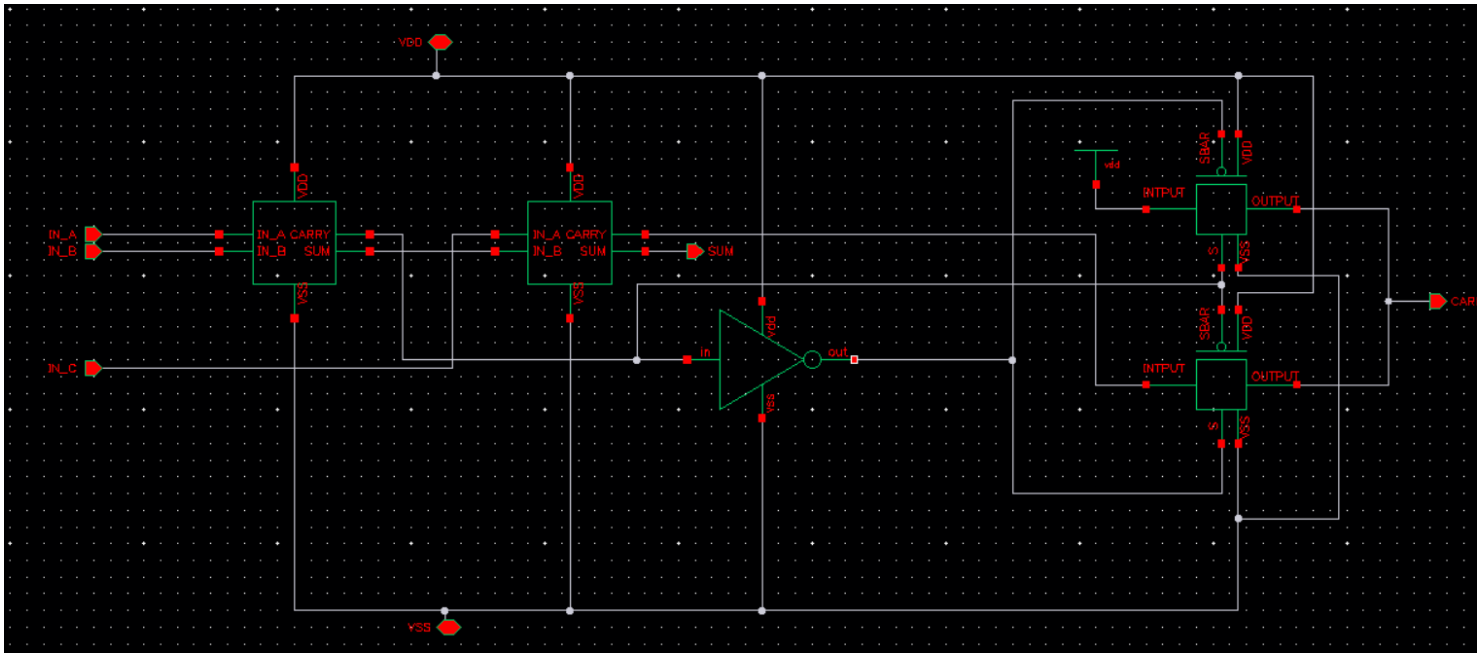
Hspice 波形圖

2 位元加法器 (透過半加器)

電路圖



Schematic 電路



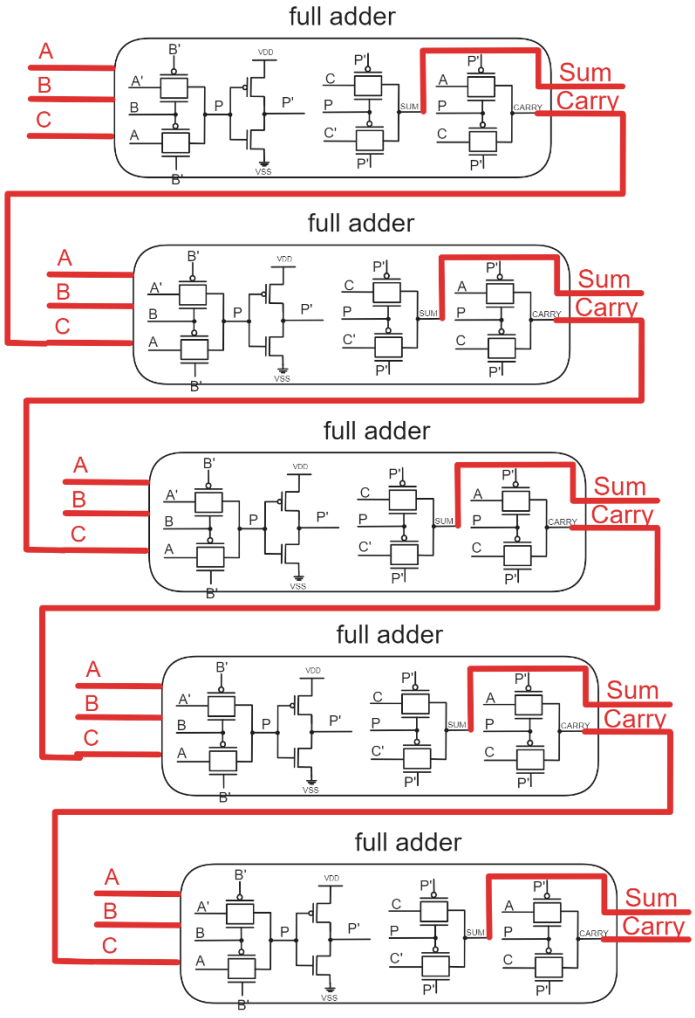
.sp 檔

```
.subckt INV in out vdd vss
m0 out in vdd vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m1 out in vss vss nch l=180e-9 w=220e-9 m=1 ad=198.4e-15 as=198.4e-15 pd=1.88e-6 ps=1.88e-6 nrd=1.40909 nrs=1.40909
.ends INV

.subckt TRAN intput output s sbar vdd vss
m2 intput sbar output vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m0 intput s output vss nch l=180e-9 w=220e-9 m=1 ad=198.4e-15 as=198.4e-15 pd=1.88e-6 ps=1.88e-6 nrd=1.40909 nrs=1.40909
.ends TRAN

.subckt half_adder carry in_a in_b sum vdd vss
xi1 in_b net2 vdd vss INV
xi0 in_a net1 vdd vss INV
xi7 0 carry net2 in_b vdd vss TRAN
xi6 in_a carry in_b net2 vdd vss TRAN
xi3 net1 sum in_b net2 vdd vss TRAN
xi2 in_a sum net2 in_b vdd vss TRAN
.ends half_adder

xi1 net3 in_c net1 sum vdd vss half_adder
xi0 net2 in_a in_b net1 vdd vss half_adder
xi3 net3 carry net4 net2 vdd vss TRAN
xi2 vdd carry net2 net4 vdd vss TRAN
xi5 net2 net4 vdd vss INV

V0 VDD 0 1.8
V1 VSS 0 0
V2 IN_A 0 pulse 1.8 0 0n 100p 100p 9.9n 20n
V3 IN_B 0 pulse 1.8 0 0n 100p 100p 4.9n 10n
V4 IN_C 0 pulse 1.8 0 0n 100p 100p 2.9n 5n

.END
```

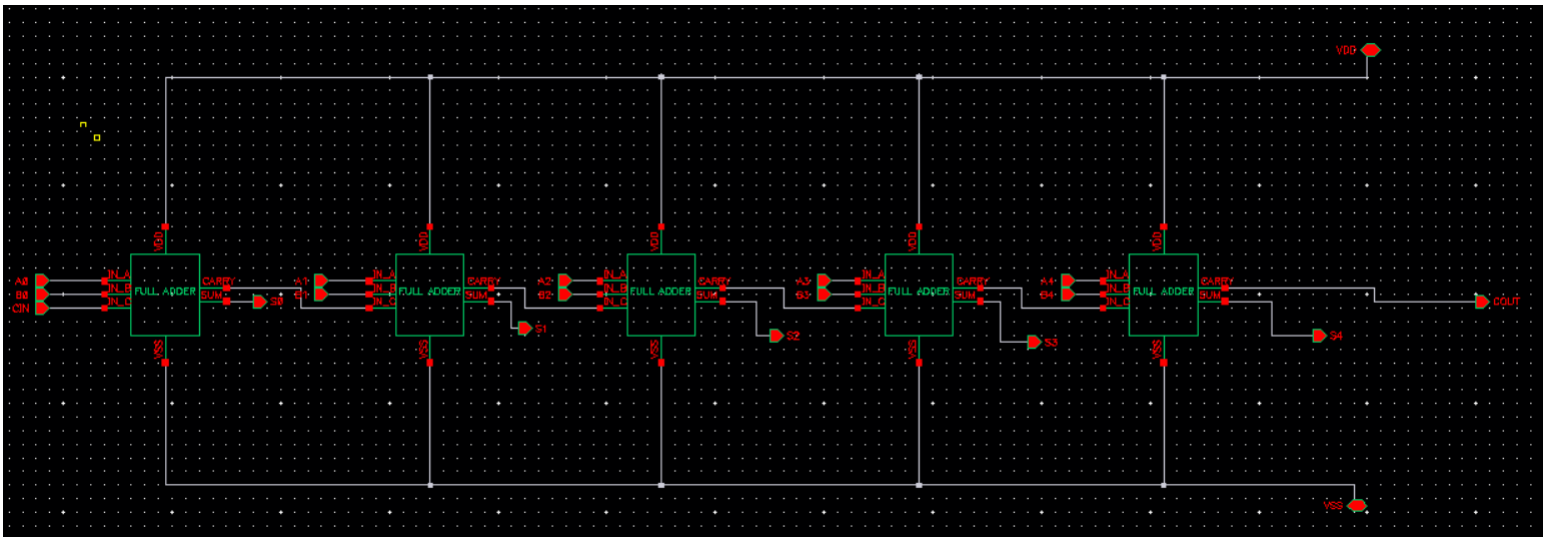
Hspice 波形圖

10 位元加法器(透過連波方式)

電路圖



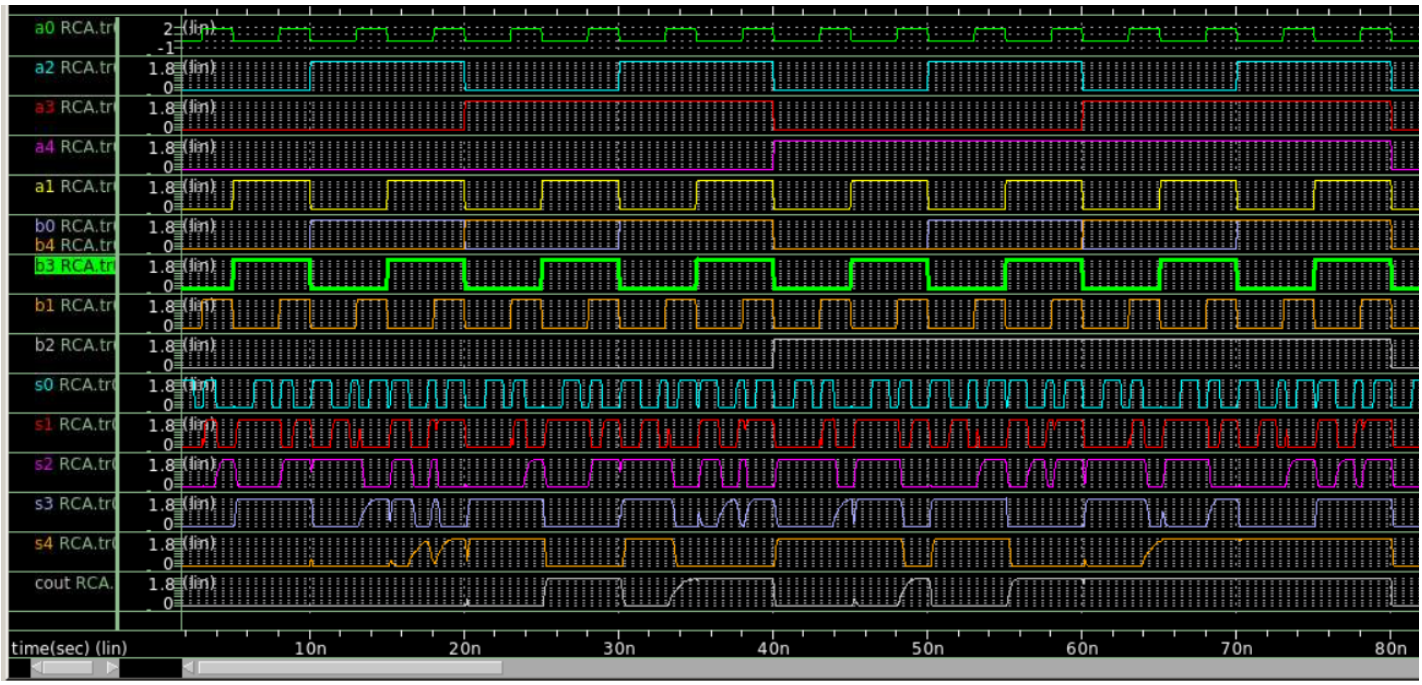
Schematic 電路圖



.sp 檔

```
.subckt TRAN intput output s sbar vdd vss
m2 intput sbar output vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m0 intput s output vss nch l=180e-9 w=220e-9 m=1 ad=198.4e-15 as=198.4e-15 pd=1.88e-6 ps=1.88e-6 nrd=1.40909 nrs=1.40909
.ends TRAN

.subckt INV in out vdd vss
m0 out in vdd vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m1 out in vss vss nch l=180e-9 w=220e-9 m=1 ad=198.4e-15 as=198.4e-15 pd=1.88e-6 ps=1.88e-6 nrd=1.40909 nrs=1.40909
.ends INV

.subckt full_adder carry in_a in_b in_c sum vdd vss
xi20 in_c carry net3 net1 vdd vss TRAN
xi17 in_c sum net1 net3 vdd vss TRAN
xi16 net2 sum net3 net1 vdd vss TRAN
xi12 in_a net3 net5 in_b vdd vss TRAN
xi11 net4 net3 in_b net5 vdd vss TRAN
xi21 in_a carry net1 net3 vdd vss TRAN
xi18 in_c net2 vdd vss INV
xi15 net3 net1 vdd vss INV
xi14 in_b net5 vdd vss INV
xi13 in_a net4 vdd vss INV
.ends full_adder

xi11 net9 a0 b0 cin s0 vdd vss full_adder
xi4 cout a4 b4 net3 s4 vdd vss full_adder
xi3 net3 a3 b3 net2 s3 vdd vss full_adder
xi2 net2 a2 b2 net1 s2 vdd vss full_adder
xi1 net1 a1 b1 net9 s1 vdd vss full_adder
```

Hspice 波形圖



我們會發現，透過 RCA(Recursive Lookahead Carry Adder)方法，當位元數越高，輸出所需要的時間要越長，不然會有問題!!!

10 位元加法器(Manchester 進位鏈加法器)

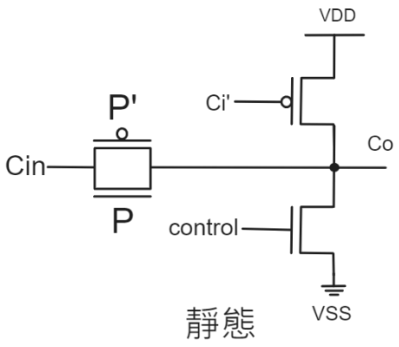
參考文件：

https://zhuanlan.zhihu.com/p/602684164

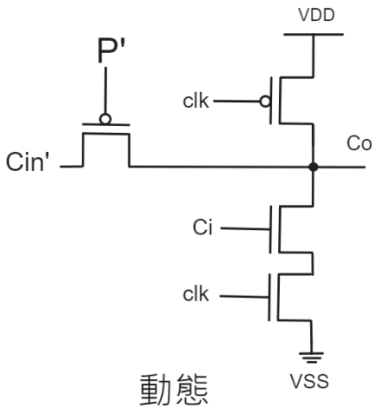
http://staff.ustc.edu.cn/~huxw/VLSI%BF%CE%BC%FE/vlsi_chapter12.pdf

https://zhuanlan.zhihu.com/p/376387699

設計架構



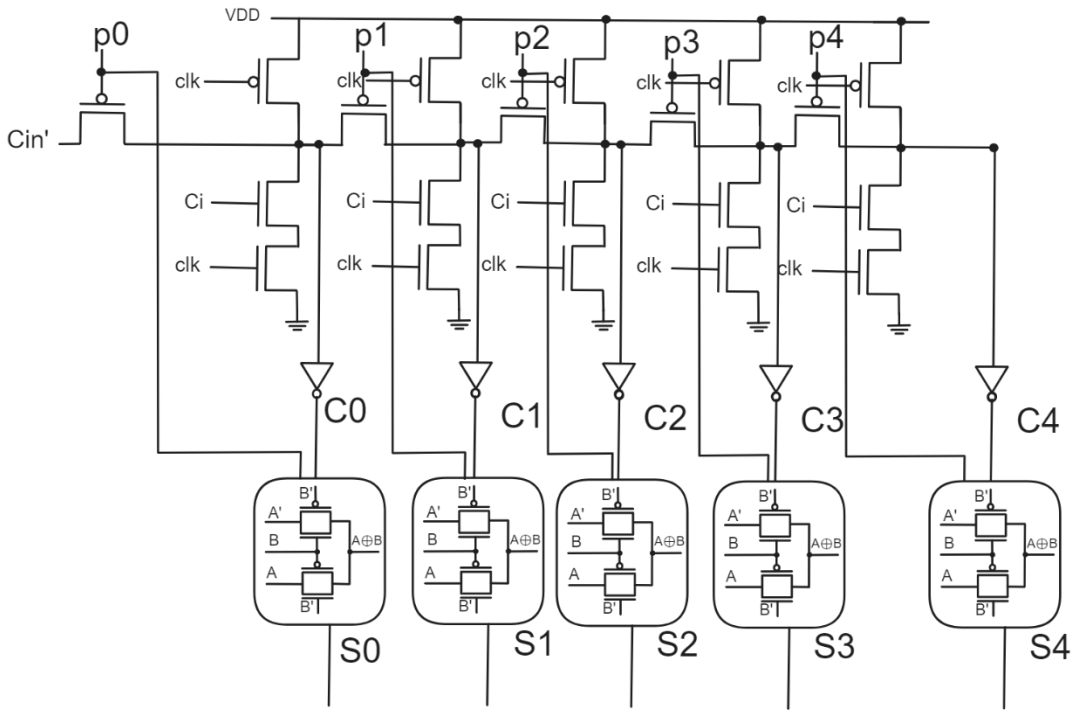
靜態



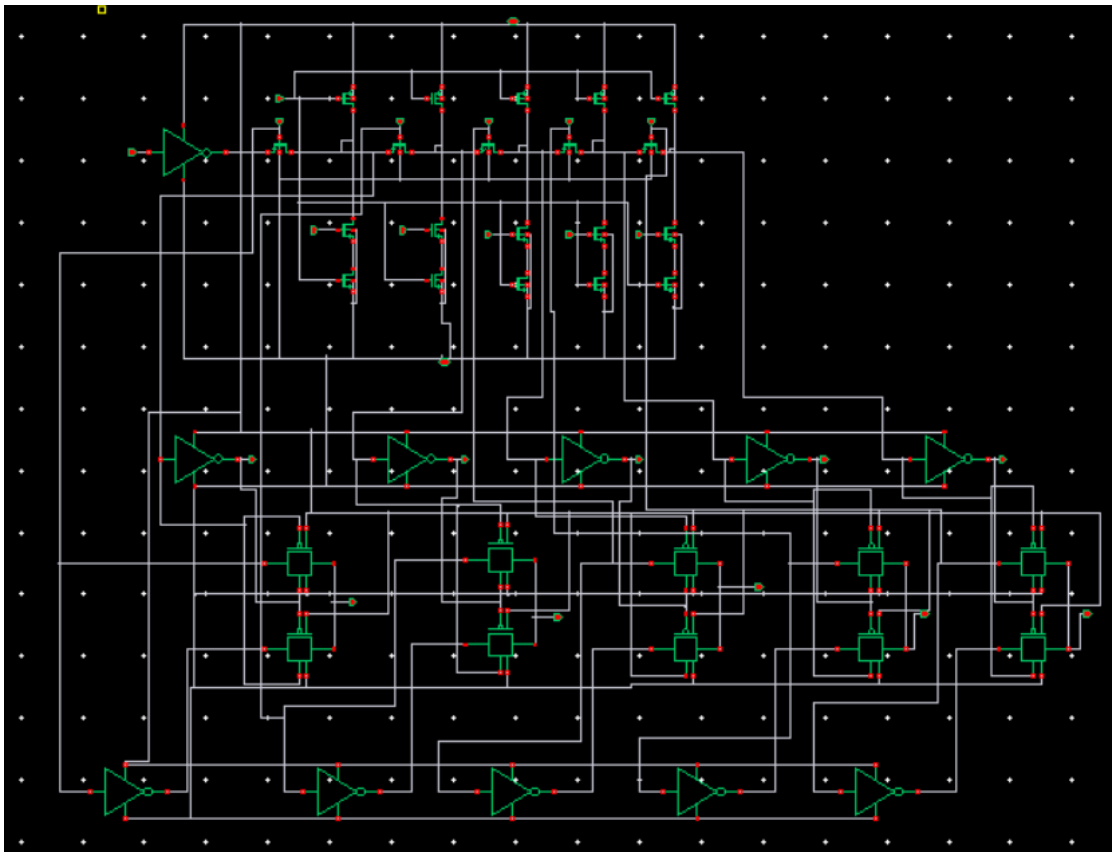
動態

以動態、pass-transistors 基礎的 Manchester 進位鏈加法器、有最少的電晶體數，此架構將可以用最少的電晶體數來製成多位元的高速加法器!

電路圖



Schematic 電路圖

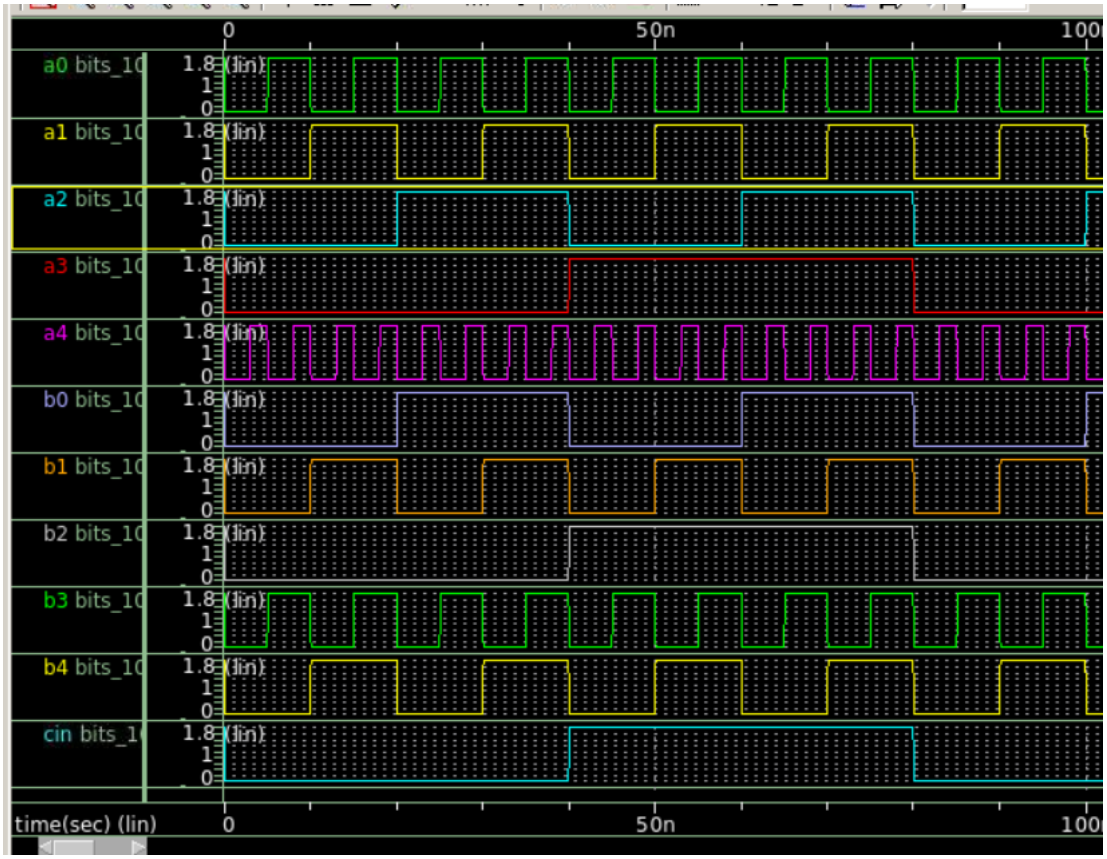


.sp 檔

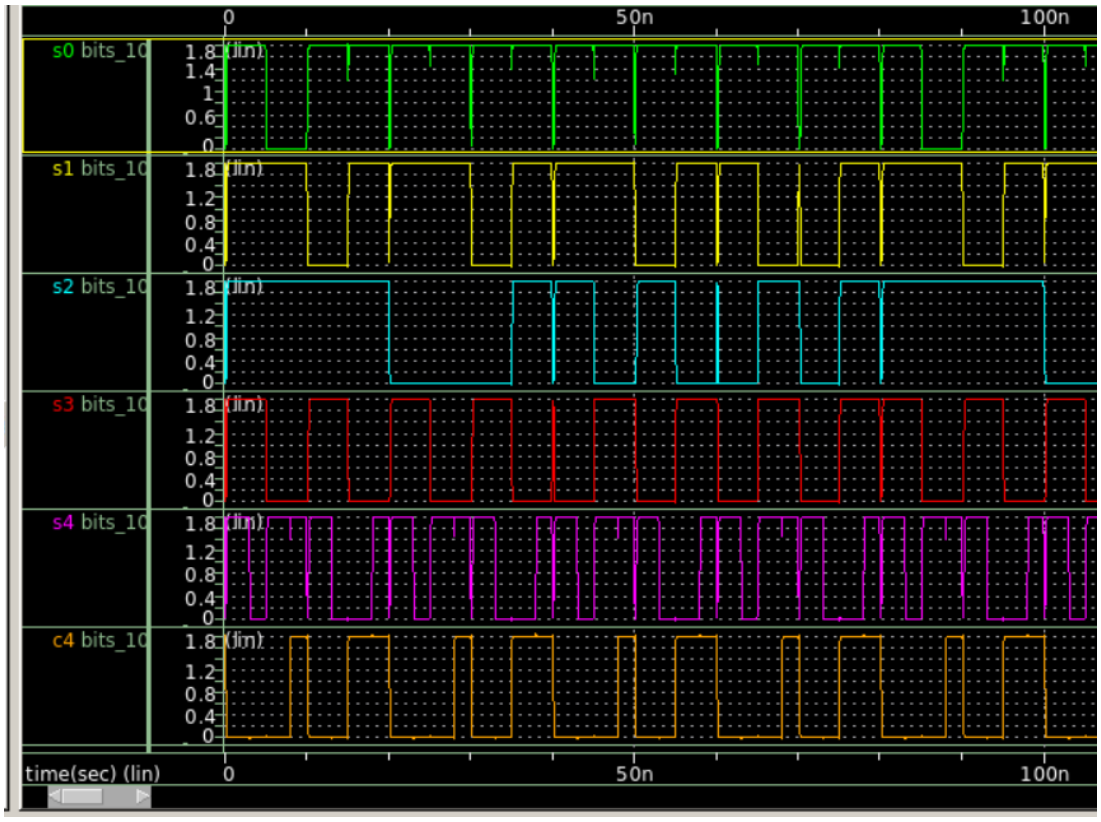
```
** View name: schematic
.subckt INV in out vdd vss
m0 out in vdd vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m1 out in vss vss nch l=180e-9 w=220e-9 m=1 ad=198.4e-15 as=198.4e-15 pd=1.88e-6 ps=1.88e-6 nrd=1.40909 nrs=1.40909
.ends INV
** End of subcircuit definition.

** Library name: LOGIC
** Cell name: TRAN
** View name: schematic
.subckt TRAN intput output s sbar vdd vss
m2 intput sbar output vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m0 intput s output vss nch l=180e-9 w=220e-9 m=1 ad=198.4e-15 as=198.4e-15 pd=1.88e-6 ps=1.88e-6 nrd=1.40909 nrs=1.40909
.ends TRAN
** End of subcircuit definition.

** Library name: LOGIC
** Cell name: bits10_best
** View name: schematic
m4 net14 clk vdd vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m3 net13 clk vdd vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m2 net12 clk vdd vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m1 net11 clk vdd vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m0 net1 clk vdd vdd pch l=180e-9 w=420e-9 m=1 ad=201.6e-15 as=201.6e-15 pd=1.8e-6 ps=1.8e-6 nrd=642.857e-3 nrs=642.857e-3
m27 net14 a4 net13 vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m26 net13 a3 net12 vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m25 net12 a2 net11 vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m24 net11 a1 net1 vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m19 net14 b4 net10 vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m18 net10 clk vss vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m17 net9 clk vss vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m16 net13 b3 net9 vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m15 net12 b2 net8 vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m14 net8 clk vss vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m13 net7 clk vss vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m12 net11 b1 net7 vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m11 net6 clk vss vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m10 net1 b0 net6 vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
m5 net1 a0 net5 vss nch l=180e-9 w=2e-6 m=1 ad=960e-15 as=960e-15 pd=4.96e-6 ps=4.96e-6 nrd=135e-3 nrs=135e-3
xi5 net14 c4 vdd vss INV
xi20 a4 net46 vdd vss INV
xi19 a1 net15 vdd vss INV
xi18 a3 net44 vdd vss INV
xi17 a2 net43 vdd vss INV
xi16 a0 net45 vdd vss INV
xi4 net13 c3 vdd vss INV
xi3 net12 c2 vdd vss INV
xi2 net11 c1 vdd vss INV
xi1 net1 c0 vdd vss INV
xi0 cin net5 vdd vss INV
xi15 net46 s4 net14 c4 vdd vss TRAN
xi14 a4 s4 c4 net14 vdd vss TRAN
xi13 a3 s3 c3 net13 vdd vss TRAN
xi12 net44 s3 net13 c3 vdd vss TRAN
xi11 net43 s2 net12 c2 vdd vss TRAN
xi10 a2 s2 c2 net12 vdd vss TRAN
xi9 a1 s1 c1 net11 vdd vss TRAN
xi8 net15 s1 net11 c1 vdd vss TRAN
xi7 net45 s0 net1 c0 vdd vss TRAN
xi6 a0 s0 c0 net1 vdd vss TRAN
```

```
V0 VDD 0 1.8
V1 VSS 0 0
V2 CIN 0 pulse 1.8 0 0n 100p 100p 39.9n 80n
V3 A0 0 pulse 1.8 0 0n 100p 100p 4.9n 10n
V4 A1 0 pulse 1.8 0 0n 100p 100p 9.9n 20n
V5 A2 0 pulse 1.8 0 0n 100p 100p 19.9n 40n
V6 A3 0 pulse 1.8 0 0n 100p 100p 39.9n 80n
V7 A4 0 pulse 1.8 0 0n 100p 100p 2.9n 5n
V8 B0 0 pulse 1.8 0 0n 100p 100p 19.9n 40n
V9 B1 0 pulse 1.8 0 0n 100p 100p 9.9n 20n
V10 B2 0 pulse 1.8 0 0n 100p 100p 39.9n 80n
V11 B3 0 pulse 1.8 0 0n 100p 100p 4.9n 10n
V12 B4 0 pulse 1.8 0 0n 100p 100p 9.9n 20n
V13 CLK 0 pulse 1.8 0 0n 100p 100p 4.9n 10n
```

Hspice 波形圖(輸入)



Hspice 波形圖(輸出)



總結：

電路	mos 數量	最長延遲
1 位元加法器 (傳輸閘)	12	1*傳輸閘+1*反向器
2 位元加法器 (傳輸閘)	18	2*傳輸閘+1*反向器
2 位元加法器 (2 個半加器)	30	3*傳輸閘+2*反向器
10 位元加法器 (Recursive Lookahead Carry Adder)	90	10*傳輸閘+5*反向器
10 位元加法器 (Manchester 進位鏈加法器)	62	1 * Manchester + 2 * 反向器+ 1 * 傳輸閘