CSCI 4591: Computer Architecture

Spring
2021 Final
Exam

Name: _____

Score: _____ / 104

This is a take home test. Please make a note of the following:

- This is open book / open notes exam.
- You can use a calculator.
- You must submit your work using the quiz on the Canvas
- PDF file is provided for your reference only.

Due Date: May 15, 2021 @ 11:55 PM – You must submit the test before this deadline. I am not going to make any exception to this rule.

GOOD LUCK!

Multiple Choice Questions: Please select the best answer from the given list for the following statements/questions. **(1 point each)**

1) An instruction can be divided into 5 stages. These stages are (select all that applies)
   i. Instruction Fetch
   ii. Instruction Development
   iii. Read Register
   iv. Read History
   v. Execute
   vi. Memory Access
   vii. MemoryDevelop ment
   viii. Write Back
   ix. Write History

2) _____is an important technique for increasing the throughput of a computer
   i. Branching
   ii. Running
   iii. Pipelining
   iv. Standing

3) The ideal memory:
   i. has low access time and is very robust
   ii. has high access time
   iii. consumes lots of power
   iv. keeps on misplacing data

4) Data can be shred between two processor using shared memory.
   i. True
   ii. False

5) If we use NUMA then all processors can access the memory in same amount of time.
   i. True
   ii. False - it can access the memory in its proximity faster

6) Amdahl's Law states that increasing the number of processors in a system is futile unless the value of f can be made very low.
   i. True
   ii. False

7) Bus topology is the simplest to implement.
   i. True
   ii. False

8) When silicon chips are fabricated, defects in materials (e.g., silicon) and manufacturing errors can result in defective circuits. A very common defect is for one signal wire to get "broken" and always register a logical 0. This is often called a "stuck-at-0" fault.

Which instructions fail to operate correctly if the ALUOp1 wire is stuck at 0?

i. R-format instructions
ii. LDUR
iii. CBZ
iv. STUR

Please fill in the blanks in the following statements: **(1 point each)**

9) When an instruction in a pipeline is rejected we say that a HAZARD/STALL has been introduces.

10) Given a direct-mapped cache with following specifications:
Number of Blocks: 32 → 2^5
Number of Words per Block: 1
Word Size: 8 bits
Byte Address: 1010 1101
Cache Index is: 5 bits for number of blocks in cache
(Block address) modulo (#Blocks in cache) → 0

11) A cache miss is called a cache miss? A request for data from the cache that cannot be filled because the data are not present in the cache but results in a stall

12) A virtual memory miss is called page fault.

13) There are three kinds of hazards associated with a pipeline processor. These hazards are: structure hazard, data hazard , and control hazard.

14) Temporal locality is the fact that items accessed recently are likely to be accessed again.

15) Virtual memory is managed by CPU hardware and Operating System.

16) Consider the following instruction mix:

R-Type	I-Type	LDUR	STUR	CBZ	B
50%	20%	5%	10%	10%	5%

i. What fraction of all instructions use data memory?
   - LDUR and STUR use data memory → 15%_____
ii. What fraction of all instructions use instruction memory? _____
   - Everything → 100%
iii. What fraction of all instructions use the sign extend? _____
   - I, LDUR, STUR, CBZ and B → 50%

17) List two differences between Von Neumann Architecture and Harvard Architecture?

(5 Points)

- Von Neumann - Used in CISC. An instruction fetch and a data operation cannot occur at the same time because they share a common bus(memory and pathways), but it is simpler
- Harvard - Used in RISC. It has separate storage and signal pathways for instructions and data

18) Assume that R1 is initialized to 11 and R2 is initialized to 22. Suppose you executed the code below on a version of the five stage pipeline. Assume that processor does not handle data hazards (i.e., the programmer is responsible for addressing data hazards by inserting NOP instructions where necessary). What would the final values of registers X3 and X4 be? **Scan and upload the solution using the upload button. (10 Points)**

solve it as normal
No NOPs needed since each of the ALUs can pass off the information down to the next code without issue.

ADDI R1, R2, #5
- R1 ← 22 + 5 = 27

ADD R3, R1, R2
- R3 ← 27 + 22 = 49

ADDI R4, R1, #15
- R4 ← 27 + 15 = 42

19) Given a cache with the following specifications: Number of Blocks: 8
Number of Words per Block: 2
Word Size: 32 bits
Address Size: 16 bits
Identify block index and tag for the following addresses:
Scan and upload the solution using the upload button. (15 points)

Address	Binary Address	Tag	Block Index
0x0003	0000 0000 0000 0011	0000 0000 00	00 0
0x112b	0001 0001 0010 1011	0001 0001 00	10 1
0x1002	0010 000 0000 0010	0010 000 00	00 0
0xFFbf	1111 1111 1011 1111	1111 1111 10	11 1
0xABCD	1010 1011 1100 1101	1010 1011 11	00 1

20) For a direct-mapped cache design with a 64-bit address, the following bits of the address are used to access the cache:

Tag(44)	Index(10)	Offset (10)
63 – 20	19 – 11	9 – 0

i. What is the cache block size in bytes? **(5 Points)**
   - 2^10 = 1024
   - 1024bytes /8bytes = 128

ii. What is the cache block size in words (assuming 64 bit word size)? **(5 Points)**
   - 128/64 = 2

iii. How many blocks does the cache have? **(5 Points)**
   - 2^10 = 1024

iv. What is the ratio between total bits required for such a cache implementation over the data storage bits? **(10 Points)**
   v = 1
   tag = 44
   data = 2 words = 16 bytes = 128 bits
   Total bits = 1 + 44 + 128 = 173 bits
   Ratio = total/data = 1.35
   Scan and upload the solution using the upload button.

21) Consider the calculation: ((A+B)*(C+D)*(E+F)*(G+H)) / ((I+J)*(K+L)). This calculation will be performed on a multiprocessor system with n processors. Calculate speedup and efficiency for an n processor system. The n is as follows: **(15 Points)**
   6 Addition steps
   4 Multiplication steps
   1 Division steps

i. n = 2
   PE1 = A A A M M D
   PE2 = A A A M M

   done in 6 unit time
   Speed up = 11 tasks/ 6 unit time = 1.833
   Efficiency = 1.833/ 2 processors = 0.916

ii. n = 6
   PE1 = A M D
   PE2 = A M
   PE3 = A M
   PE4 = A M
   PE5 = A M
   PE6 = A

done in 3 unit time
Speed up = 11 tasks/ 3 unit time = 3.66
Efficiency = 1.833/ 6 processors = 0.61

iii. n = 20
done in 3 unit time
Speed up = 11 tasks/ 3 unit time = 3.66
Efficiency = 1.833/ 20 processors = 0.183

Scan and upload the solution using the upload button.

22) A computer system has 64 microprocessor and the fraction of the code that is carried out serially is 10%. Suppose you wish to run the same code on a system with 30 processors. What fraction of the code may be executed serially to maintain the same speedup ratio?

(10 Points)

Scan and upload the solution using the upload button.

10% of 64 = 6.4 running serially
64-6.4 = 57.6 running parallel

6.4 = x/30
6.4/30 = 21.33% serially to run the same as 30 processors

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