

CSCI 4591: Computer Architecture
HW Assignment # 4

Due Date: February 28, 2021 @ 12:55 PM

1) Provide the instruction type and assembly language instruction for the following
hex value: $8B050024_{16}$
convert to binary = 8 11 0 5 0 0 2 4

1000 1011 0000 0101 0000 0000 0010 0100

opcode :

1	0	0	0	1	0	1	1	0	0	0
---	---	---	---	---	---	---	---	---	---	---

Instruction type R and ADD

Rm: 0 0 1 0 1 = 5

shamt: 0 0 0 0 0 0

Rn: 0 0 0 0 1 = 1

Rd: 0 0 1 0 0 = 4

Add Rd, Rn, Rm

Add = R4 <- R1 + R5

2) Provide the instruction type and hexadecimal representation of the following instructions:

1) STUR X12, [X10]

- Instruction Type D

Stur	Address	op2	Rn	Rt
	0	N/A	x10	x12
11111000000	000000000	00?	01010	01100

- Hex format = F800014C

2) ADDI X11, X12, #45

- Instruction Type: I

opcode	immediate(45)	Rn(12)	Rd(11)
1001000100	000000101101	01100	01011

- Hex format: 9100B58B

3) SUBS X13, X14, X15

*Dr.L's way

- Instruction Type: R

SUBS	Rm-x14	shamt	Rn-x15	Rd-x13
11101011000	01110	000000	01111	01101

- Hex format: EB0E01ED

*BOOK WAY

- Instruction Type: R

SUBS	Rm-x15	shamt	Rn-x14	Rd-x13
11101011000	01111	000000	01110	01101

- Hex format: EB0F01CD

4) B.Next (Next is 0x1010)

- Instruction Type: B

opcode address = 1010 -> binary

000101 0000000000 0001 0000 0001 0000

- Hex format: 14001010

5) B.NE Next (Next is 0x1010) NE is condition

- Instruction Type: CB

condition code = NE 00001

0x1010 = 0001 0000 0001 0000

opcode	address	Rt/Condition code
01010100	000 0001 0000 0001 0000	00001

- Hex format: 54020201

6) LDUR X15, [X13, # 45]

- Instruction Type: D

LDUR	Address(45)	op2	Rn(x13)	Rt(x15)
11111000010	000101101	00	01101	01111

- Hex format: F842D1AF

7) CBNZ X12, Next (Next is 0x1010)

- Instruction Type: CB

opcode	address	Rt/Condition code(12)
10110101	000 0001 0000 0001 0000	01100

- Hex format: B502020C

3) Assume that we would like to expand the LEGv8 register file to 128 registers and expand the instruction set to contain four times as many instructions.

1) How this would affect the size of each of the bit fields in the R-type instructions?

- For R type, we would have to increase each of the fields to 7 bits. So Rm, Rn and Rd would have to increase from 5 to 7. There are 6 bits extra so you can split them up between the 3.
- There's also an option to keeping Rm, Rn and Rd at 5 bits and moving all of the bits to shamt. So shamt would equal 12 bits

2) How this would affect the size of each of the bit fields in the I-type instructions?

- For I type, it will still be the same as part 1, where Rd and Rn would have to increase to 7 bits and put the extra 2 bits into Rd and Rn

4) Assume the following register contents:

```
R10 = 0x00000000AAAAAAAA, R11 = 0x12345678 12345678
```

$$R_{10} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix}_2$$

```
R11 = 0001 0010 0011 0100 0101 0110 0111 1000 0001 0010 0011
0100 0101 0110 0111 1000
```

2

1) For the register values shown above, what is the value of X12 for the following sequence of instructions?

convert to binary first

```
LSL R12, R10, #4
```

Rd(R12) = 0000 0000 0000 0000 0000 0000 0000 1010 1010 1010
1010 1010 1010 1010 1010 0000

ORR R12, R12, R11

R12 first line, R11 2nd line

```

000000000000000000000000000101010101010101010101010100000
0001001000110100010101100111100000010010001101000101011001111000
-----
000100100011010001010110011110101011101010111110111111011111000
^new R12

```

2) For the register values shown above, what is the value of X12 for the following sequence of instructions?

```
LSL R12, R11, #4
```

$$\begin{array}{cccccccccc} \text{Rd(R12)} & = & 0010 & 0011 & 0100 & 0101 & 0110 & 0111 & 1000 & 0001 & 0010 \\ & & 0011 & 0100 & 0101 & 0110 & 0111 & 1000 & 0000 & & \end{array}$$

3) For the register values shown above, what is the value of X12 for the following sequence of instructions?

```
LSR R12, R10, #3
```

$$\text{Rd}(\text{R12}) = \begin{matrix} 0000 & 0000 & 0000 & 000 & 0000 & 0000 & 0000 & 0000 & 0000 \\ 1010 & 1010 & 1010 & 1010 & 1010 & 1010 & 1010 & 1_2 \end{matrix}$$

```
ANDI R12, R12, 0xFE = 1111 1110 1111
```

shifted R12 + 0xFF

[illegible]

[illegible]

Create the text file using Microsoft Word, Open Office Writer, or a text editor. Name the document as follows:

FirstName_LastName_HW4

Rubric for Grading:

Description	Points
Question 1	10
Question 2	70
Question 3	20
Question 4	30
Total Points	130