|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name/Id of Program/Project | : | Brake Pedal Transmitter Unit (BPTU) | | |
| Title of Document | : | Board Requirement Data (BRD) for | | |
|  | : | BPTU | | |
|  | : |  | | |
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# Scope

## Identification

This document is the Board Requirement Data (**BRD**) of the Hardware Item named Brake Pedal Transmitter Unit (**BPTU**). This product will be developed according to DO-254 standards. The Design Assurance Level (DAL) of this development will be level D.

## Hardware Item Overview

### System presentation

The **BPTU** is the system which measures and sends the brake orders of the left and the right brake pedals of the X4 helicopter. It also provides a proportional load feeling on the brake pedals. It is linked to the helicopter rudder pedals mechanism. The brake pedal mechanism is illustrated by the figure below:

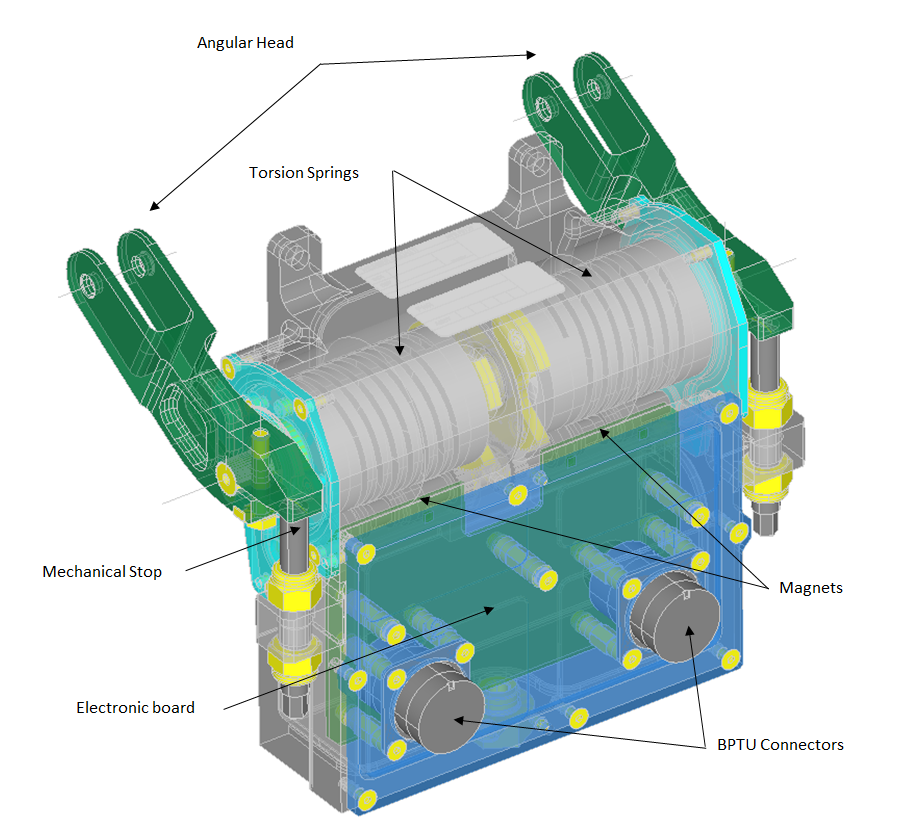


Figure 1‑1: Physical BPTU view

### System functions

The BPTU offers the following functions:

* Measures and sends brake orders (pedal angles) of the left and right brake pedals,
* Provides a proportional load feeling on each one of the brake pedals to the Pilots,
* Integrates an adjustable (during development) preload mechanism,
* Provides a local monitoring with CBIT and PBIT.
* Equipment localization (Pilot or Co-Pilot),
* Digital filtering of pedal deflections,
* Emission of data through CAN1 and CAN2 buses,
* Provide a mechanical zero,
* Provide a mechanical stop, when the pedal is released

The BPTU integrates two independent and dissymmetrical acquisition electronic modules on the same board, these modules provide information on two segregated CAN Buses. The figure below provides a synoptic of BPTU architecture (‘α’ is the angle resulting from the rotation of the Left pedal and ‘β’ is the angle resulting from the rotation of the right pedal):



Figure 1‑2: Board architecture

As shown in the figure 2 the COM and MON channels are performed with different components, for example the COM channel uses a PROASIC3 FPGA and the MON channel uses an IGLOO2 FPGA family component. The same treatment is applied for the ADC, hall-effect sensors, CAN transceivers and power supply components, in order to avoid common mode failures.

### Mission profile

|  |  |  |
| --- | --- | --- |
| **Phase** | **Duration phase per year** | **Mean temperature** |
| In flight operating | tARW = 1200h | 50°C |
| On ground Operating | tGF = 100h | 40°C |
| On ground not operating | tNO = 7460h | 40°C |

5 flights = 1 FH (6000 flights/year)

## Document Overview

The Board Requirement Data is the definition of the Board Requirements including the derived requirements. It includes:

* The system design and safety requirements allocated to the board.
* Identification of applicable standards for the board.
* Board functional and performance requirements, including derived requirements and stress limits for normal use.

This document is written according to the Hardware Requirements Standards (HRS) [IAD1]

This document includes also the implementation of requirements which concern the board components.

## Identification of requirements

Each requirement is identified as follows:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| BRD-BPTU-Num-Type | | | Title | Version: | 1 |
|  | Covers: | « mother requirement », derived or N/A when no upper level specification exists. | | Verification : | Analysis |
| Definition:  Requirement definition  Rationale:  Requirement justification if required (derived requirements or additional information)  or  This requirement is justified at upper level. | | | | | |
| End\_Req | | | | | |
| Notes: | | | | | |

Where the “BRD-BPTU-Num” is the capability to be specified:

“Num” is a 4 digits numbers that uniquely identifies the requirement in the document.

“Type” is a single letter that represents special requirements

* + D for derived requirements
  + S for Safety requirements
  + R for Robustness requirements

“Version” is the release number of that requirement.

“Verification” is the proposed qualification method used to verify that requirement: analysis, review or test. It may be changed by the verification responsible.

“Covers” is the mother requirement from which that requirement depends. If none, that requirement is “derived” and “N/A” if not applicable. Coverage can be partial.

Example:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| BRD-BPTU-XXXX | | | Input clock | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_XXXX partial | | Verification : | Analysis |
| Definition:  The design shall be synchronous to one 1MHz (±100ppm) clock which is provided as an input.  Rationale:  Upper level requirement is refined by design decision to store data received from the ARINC 825 CAN Bus and destined to be sent through the APB interface. | | | | | |
| End\_Req | | | | | |
| Notes: This clock will further be referred as CLK | | | | | |

The first requirement is numbered: 0010.

New Requirement: each time a new requirement is added the number “Num” shall be incremented by 10 and the “version” set to 1.

Requirement insertion: an additional requirement can be inserted, using the last digit for numbering (e.g. \_0015 between \_0010 and \_0020).

Requirement deletion: each time a requirement is deleted the number “Num” shall not be reused and the “text” shall be to “deleted”.

## Interpretation

“Shall”, the imperative form of the verb, is used throughout this BRD whenever a requirement is intended to express a provision that is mandatory. Deviation from a “shall” requirement may be considered if sufficient data is supplied to justify the exception.

The words “should” and “may” are used whenever it is necessary to express non-mandatory provisions. “Will” is used to express a declaration of purpose.

# Applicable and Reference Documents

This chapter gives the list of documents referenced in this document. Projects documents are referred to without their issue number. Applicable revisions are identified in the corresponding Board Configuration Index (**BCI**) for a given board version. Other documents are referred to with their issue number.

## External Applicable Documents

|  |  |  |
| --- | --- | --- |
| Title | Reference | Origin |
| 1. Design Assurance Guidance for Airborne Electronic Hardware | DO-254 / ED-80 | RTCA / EUROCAE |
| 1. EASA CM-SWCEH-001 Development Assurance of Airborne Electronic Hardware issue 01 | EASA CEH memo | EASA |
| 1. General Standardization of CAN (Controller Area Network) bus protocol for airborne use | ARINC SPECIFICATION 825-1  May 10, 2010 | AERONAUTICAL RADIO, INC. |
| 1. CAN 2.0 Specification v2.0 | Bosh CAN2.0A and CAN2.0B | BOSH |
| 1. CAN - Part 1: Data link layer and physical signaling | ISO 11898-1 | ISO |
| 1. Interface Card Drawing | DR75084  Issue 02 | MBD |

## Internal Applicable Documents

|  |  |
| --- | --- |
| Title | Reference |
| 1. Hardware Requirement Standards (HRS) | HRS\_BPTU\_0106 |
| 1. BPTU Interface Control Document | A4155-1311-D24 |
| 1. BPTU Project Management Plan | A4150-1311-D26 |
| 1. BPTU Functional Analysis | A4154-1311-D22 |
| 1. BPTU Board Supplier Recommendation (BSR) | BSR\_BPTU\_0108 |
| 1. BPTU BIT Concept | A4154-1311-D23 |
| 1. BPTU PTS compliance matrix | A4155-1402-D14 |
| 1. Hardware Requirement Data (HRD) | HRD\_BPTU\_0110 |
| 1. BPTU Board Traceability Matrix (BTM) | BTM\_BPTU\_0113 |
| 1. BPTU Development Tests Report – Oven Tests | A4150-1501-D01 |

## Reference Documents

### General documents

|  |  |  |
| --- | --- | --- |
| Title | Reference | Origin |
| 1. System Requirement Distribution | A4150-1401-D01 | SILKAN |
| 1. General Requirements for Equipments using CAN Technology | SPX880AZ130E10 Issue B | AH |
| 1. CAN Bus Message Format Specification | SPX880AZ129E10 Issue A | AH |
| 1. Electrical Interfaces Design General Rules | SPX880AZ126E10 Issue – (02/04/12) | AH |
| 1. Environmental requirements for equipment installed on eurocopter helicopter | SPX902A0002E01(24/06/99) | AH |
| 1. Caractéristiques de l’alimentation électrique des aéronefs | NF EN 2282 mai 1992 | Afnor |
| 1. Electrical Bonding and grounding point for X4 | HS 353 \_ item number 00 | X4 |
| 1. Environmental Conditions and Test Procedures for Airborne Equipment | RTCA DO-160F Supersedes DO-160E December6, 2007 | RTCA |

### Power supply component datasheet

|  |  |  |
| --- | --- | --- |
| Title | Reference | Origin |
| 1. Transient Voltage Suppression Diodes / Axial Leaded – 5000W > 5KP series | Revision: January 09, 2009 | Littelfuse |
| 1. Ultrafast Switching Surface Mount Silicon Rectifier Diodes USL1M | Version 2013-02-05 | Diotec |
| 1. BPTU transformer specification | A4155-1406-D37 | SILKAN |
| 1. SMPS MOSFET IRF7450 | PD- 93893A | International Rectifier |
| 1. N-Channel 200-V (D-S) MOSFET Si4462DY | 72093  S09-0705-Rev. C, 27-Apr-09 | Vishay |
| 1. High-Voltage Current-Mode PWM Controller HV9113 | DSPD-14SOICNG  Version E101708 | Supertex inc. |
| 1. High Performance Industry Standard Single-Ended Current Mode PWM Controller ISL8843A | FN6320.3  April 18,2007 | Intersil |
| 1. Single high-voltage switching diode BAS521 | Rev.2 – 5 November 2010 | NXP |
| 1. 40 V, 1.5 A low VF MEGA Schottky barrier rectifier PMEG4015EPK | Rev.2 – 6 March 2012 | NXP |
| 1. Low VF (MEGA) Schottky barrier diode PMEG2015EA | 03 February 2004 | NXP |
| 1. TLV431x Low-Voltage Adjustable Precision Shunt Regulator | SLVS139U –JULY 1996–REVISED JANUARY 2014 | TI |
| 1. Programmable shunt voltage reference TS2431 | Doc ID 7961 Rev 4  November 2012 | ST |
| 1. Synchronous rectification with enable, 0.7 A, 1.7 MHz fixed or adjustable step-down switching regulator in TSOT23-5L ST1S12GR | Doc ID 14314 Rev 5  February 2012 | ST |
| 1. Optocoupler, Phototransistor Output, High Temperature VO615A | 81753  Rev. 2.2, 09-Sep-13 | Vishay |
| 1. FODM121 Series, FODM124, FODM2701, FODM2705 / 4-Pin Full Pitch Mini-Flat Package Transistor Output Optocouplers | FODMXXX Rev. 1.1.4  February 2012 | Fairchild |

### Acquisition channel component datasheet

|  |  |  |
| --- | --- | --- |
| Title | Reference | Origin |
| 1. Magnet orientation | ECM-SRT-MBD-0025\_BPTU \_ issue 1 | SILKAN |
| 1. Linear Hall-Effect Sensor ICs with Analog Output / Available in a Miniature, Low Profile Surface Mount Package / A1318 | A1318-DS | Allegro |
| 1. Linear Hall-effect sensor ICs / SS39ET | 005850-3-EN march 2013 | Honeywell |
| 1. Wide Supply Range, Rail-to-Rail /Output Instrumentation Amplifier / AD8226 | AD8226 Rev.C | AD |
| 1. Micro-Power (50mA), Zerø-Drift, Rail-to-Rail Out / Instrumentation amplifier / INA333 | SBOS445B–JULY 2008–REVISED OCTOBER 2008 | TI |
| 1. 1 MSPS, Ultralow Power,12-Bit ADC in 8-Lead LFCSP / AD7091 | AD7091 Rev. A | AD |
| 1. Low-power, 12-bit, 1MHz, single/dual unipolar input, analog-to-digital converters with serial interface / ADS7229 | ADS7229 SBAS437A – may 2008 – Revised June 2009 | TI |

### Processing component datasheet

|  |  |  |
| --- | --- | --- |
| Title | Reference | Origin |
| 1. ProASIC3 Flash Family FPGAs with Optional Soft ARM Support | Revision 13 | Microsemi |
| 1. Igloo2 FPGAs | Revision 2 | Microsemi |
| 1. 64K I2C™ Serial EEPROM / 24LC64-EST | DS21189T | Microship |
| 1. 64-Kbit serial I²C bus EEPROM / M24C64 | DocID16891 Rev 28 | ST |
| 1. Crystal Oscillator / SG310 series |  | Epson Toyocom |
| 1. XO32 Series Oscillators |  | Euroquartz |
| 1. .050 x .050 cl double vertical smt terminal strip / FTSH-1XX-XX-XXX-DV-XXX-XXX | Revision EV | Samtec |
| 1. Surface Mount, Schottky Power Rectifier / MBR0520LT3G | MBR0520LT1/D  January, 2012 − Rev. 6 | ON Semiconductor |

### CAN interface component datasheet

|  |  |  |
| --- | --- | --- |
| Title | Reference | Origin |
| 1. CAN transceiver MAX13054 | 19-3598; Rev 1; 2/13 | Maxim |
| 1. CAN transceiver AMIS-30663 | AMIS−30663/D  January, 2009 − Rev. 6 | On Semiconductor |
| 1. Transient Voltage Suppression Diodes / Surface mount – 5000W > 5.0SMDJ series | Revision: January 09, 2009 | Littelfuse |
| 1. ES3A – ES3J Fast rectifiers | MBR0520LT1/D | Fairchild |

### Monitoring component datasheet

|  |  |  |
| --- | --- | --- |
| Title | Reference | Origin |
| 1. ADC AD7922 | AD7922 Rev.0 | AD |

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# Terminology

## Definitions

Some terms shall be defined:

**ARINC 825**

General Standardization of CAN (Controller Area Network) Bus Protocol for Airborne Use.

**CAN**

The **C**ontroller **A**rea **N**etwork is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high speed networks to low cost multiplex wiring.

**FPGA**

A **F**ield **P**rogrammable **G**ate **A**rray is an integrated circuit designed to be configured by the customer or designer after manufacturing.

## List of acronyms

|  |  |
| --- | --- |
| **AD** | **A**nalog **D**evices |
| **ADC** | **A**nalog to **D**igital **C**onverter |
| **BCI** | **B**oard **C**onfiguration **I**ndex |
| **BIT** | **B**uilt-**I**n **T**est |
| **BPTU** | **B**rake **P**edal **T**ransmitter **U**nit |
| **BRD** | **B**oard **R**equirement **D**ata |
| **BWI** | **B**and**WI**dth |
| **CAN** | **C**ontroller **A**rea **N**etwork |
| **CBIT** | **C**ontinuous **B**uilt-**I**n **T**est |
| **CLK** | **C**lock |
| **COM** | Channel which provide information on CAN1 bus |
| **CRC** | **C**yclic **R**edundancy **C**heck |
| **DAL** | **D**esign **A**ssurance **L**evel |
| **DC** | **D**irect **C**urrent |
| **DNL** | **D**ifferential **N**on **L**inearity |
| **AH** | **A**irbus **H**elicopter |
| **EEPROM** | **E**lectrically-**E**rasable **P**rogrammable **R**ead-**O**nly **M**emory |
| **EMC** | **E**lectro**M**agnetic **C**ompatibility |
| **EMI** | **E**lectro**M**agnetic **I**nterference |
| **ETS** | **E**quipement **T**echnical **S**pecification |
| **EUROCAE** | **EUR**opean **O**rganization for **C**ivil **A**viation **E**quipment |
| **FPGA** | **F**ield-**P**rogrammable **G**ate **A**rray |
| **FSR** | **F**ull **S**cale **R**ange |
| **G** | **G**auss |
| **GND** | **G**round |
| **HRS** | **H**ardware **R**equirements **S**tandards |
| **HW** | **H**ard**w**are |
| **I/O** | **I**nput**/O**utput |
| **IAD** | **I**nternal **A**pplicable **D**ocuments |
| **ID** | **Id**entification |
| **JTAG** | **J**oint **T**est **A**ction **G**roup |
| **LSB** | **L**east **S**ignificant **B**it |
| **MBD** | **M**essier **B**ugatti **D**owty |
| **MON** | Channel which provide information on CAN2 bus |
| **NA** | **N**ot **A**pplicable (or N/A) |
| **NC** | **N**on **C**ompliant |
| **OOR** | **O**ut **O**f **R**ange |
| **PBIT** | **P**ower **B**uilt-**I**n **T**est |
| **PLD** | **P**rogrammable **L**ogic **D**evice |
| **RD** | **R**eference **D**ocuments |
| **RF** | **R**adio **F**requency |
| **SEU** | **S**ingle **E**vent **U**pset |
| **SOIC** | **S**mall **O**utline **I**ntegrated **C**ircuit |
| **ST** | **ST**microelectronics |
| **SVN** | **S**ub**V**ersio**N** |
| **TAMB** | **A**mbiant **T**emperature |
| **TBC** | **T**o **B**e **C**onfirmed |
| **TBD** | **T**o **B**e **D**efined |
| **TI** | **T**exas **I**nstrument |
| **TSTORAGE** | **S**torage **T**emperature |
| **VDC** | **D**irect **C**urrent **V**oltage |

## Convention

The following table details number convention:

|  |  |
| --- | --- |
| Number type | Convention |
| Decimal | The decimal number followed by “d”. *Ex: 15d* |
| Hexadecimal | The hexadecimal number followed by “h”. *Ex: Fh* |
| The hexadecimal address after “0x”. *Ex: 0xF* |
| Binary | The binary number followed by “b”. *Ex: 1111b* |

Table 3‑1: Numbers convention

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# Board Requirements

## Scope

This development specification (hereafter referred BRD) defines the requirements for BPTU board. These requirements are grouped as functional, performance, environmental, test and safety requirements. The requirements’ implementation is explained on this document.

Referred to [IAD4] , the board is represented by the two following functions:

* FP1\_BrakeAnglesMeasuringAndSending: this function transforms electromagnetic information produced by pedal rotation through magnet motion into data sent to CAN buses.
* FC1\_Protection: BPTU’s board needs some physical protection.

Upper level requirements are located in [RD1] .

## Architecture

### BPTU functions

Referred to [IAD4] , board includes the following functions:

* **Acquisition channel** which:
  + Supply two angular position sensors for α (left pedal) and β (right pedal),
  + Perform the signal conditioning and analog to digital conversion of the angular positions sensor feedback signals,
* Perform a data **processing**,
* Send the digital signals on a CAN bus through a **CAN interface**,
* Elaborate internal **power supplies** from 28 VDC input,
* **Monitor** power supply,
* **Protection** with:
  + Filtering;
  + Galvanic Insulation;
  + Lightning Protection.

The following figure represents the BPTU functions implemented on the board:



Figure 4‑1: BPTU functions

### Independent channels: COM and MON

To guarantee the safety of the equipment it is necessary to incorporate two pairs of segregated and dissimilar angle position sensors and electronic modules. BPTU integrates two independents channels named COM and MON (see [IAD4] ).

Requirements

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0050 | | BPTU architecture | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0001 partial | Verification : | Analysis |
| Definition:  The BPTU shall incorporate two pairs of segregated and dissimilar angle position sensors and electronic modules.   * A COM channel module – providing α1 and β1 * A MON channel module – providing α2 and β2   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Each channel is compliant with the architecture presented in §4.2.1:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0060 | | COM channel function | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0002 | Verification : | Analysis |
| Definition:  The COM channel module shall:   * Perform I/O filtering (lightning, EMI), * Elaborate internal power supplies (segregated from MON power supplies) from 28 VDC input, * Supply two COM angular position sensors for α and β, * Perform the signal conditioning and analog to digital conversion of the COM angular positions sensor feedback signals, * Send the COM digital signals (α1 and β1) on a first CAN bus (CAN1).   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| BRD-BPTU-0070 | | | MON channel function | Version: | 1 |
|  | Covers: | | MBD\_X4\_BPTU\_ETS\_0003 | Verification : | Analysis |
| Definition:  The MON channel module shall:   * Perform I/O filtering (lightning, EMI), * Elaborate internal power supplies (segregated from COM power supplies) from 28 VDC input, * Supply two MON angular position sensors for α and β, * Perform the signal conditioning and analog to digital conversion of the MON angular positions sensor feedback signals, * Send the MON digital signals (α2 and β2) on a first CAN bus (CAN2).   Rationale:  This requirement is justified at upper level. | | | | | |
| End\_Req | | | | | |
| Notes: | | | | | |
| BRD-BPTU-0460 | | Number of programmable logic devices | | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0095  MBD\_X4\_BPTU\_ETS\_0001 partial | | Verification : | Analysis |
| Definition:  BPTU programmable logic device(s) should not be dedicated to compute a single pedal deflection.  Rationale:  This requirement is justified at upper level. | | | | | |
| End\_Req | | | | | |
| Notes: | | | | | |

Implementation

The following figure represents the BPTU architecture with two different acquisitions channels for each angle.



Legend:



Figure 4‑2: Transmitter system architecture

The following table shows the components and their channel:



Table 4‑1: Components table

### Board interfaces

#### Electronic board size

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1050-D | | Electronic board size | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  Electronic board size shall comply with [IAD2] paragraph “Electrical connections”, sub-paragraph “Electronic board size".  Rationale:  This requirement is justified by mechanical interfaces specifications. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

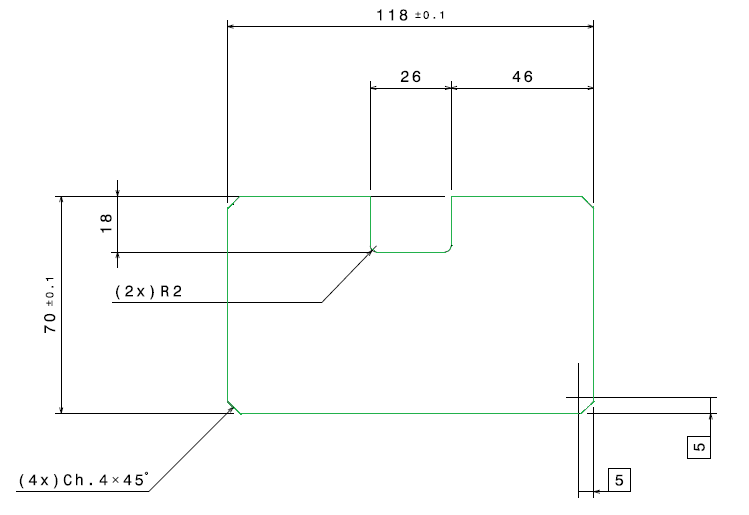


Figure 4‑3: Electronic board size

Note: on the following document, the **TOP** face of the electronic board represents the face where connectors are mounted and the **BOTTOM** face of the electronic board represents the face where hall-effect sensors are mounted.

#### Board’s studs

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1055-D | | Board’s studs | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  Board’s studs localization shall comply with [IAD2] paragraph “Electrical connections”, sub-paragraph “Board’s studs localizations".  Rationale:  This requirement is justified by mechanical interfaces specifications. | | | | |
| End\_Req | | | | |
| Notes: see [EAD6] . | | | | |

Implementation

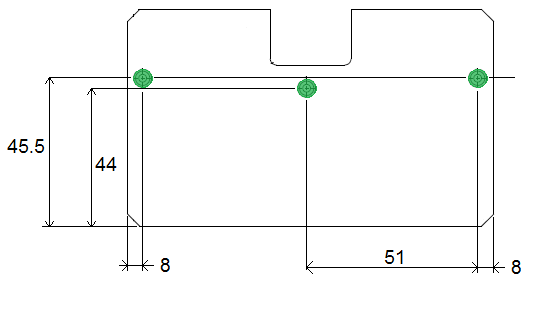


Figure 4‑4: Board’s studs localizations

Studs information:

(3x) Ø7.5mm for metallization

(3x) Ø5.01mm H7 for drill holes

#### Connectors

BPTU connectors provide:

* 28VDC power supply,
* PIN\_PROG to distinguish the pilot BPTU from the co-pilot BPTU,
* BUS\_CAN1,
* BUS\_CAN2,
* SILKAN\_PROG to calibrate EEPROM in maintenance mode (see 4.4.7 to have more information about this mode)
* A safety wire.

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1060 | | Connectors localization | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0155 | Verification : | Analysis |
| Definition:  Connectors localization shall comply with [IAD2] paragraph Electrical connections”, sub-paragraph “Connectors’ studs localizations".  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

The input and the output of the board are provided by two connectors named J1 and J2.

Hereafter a figure of connectors’ location on TOP board:

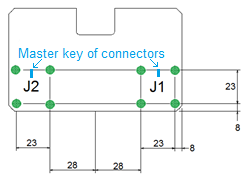


Figure 4‑5: BPTU connectors’ localization

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0010 | | Connectors pin allocation | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0154 | Verification : | Analysis |
| Definition:  Connectors nets shall comply with [IAD2] paragraph “Signal and wires definition”.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0020 | | Connectors connection | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0066 | Verification : | Analysis |
| Definition:  Connectors shall be polarized and identified so that incorrect connection is impossible. It shall not be necessary to refer to manuals or drawings to correctly assemble a unit.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0030 | | Connectors locking | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0067 | Verification : | Analysis |
| Definition:  Equipment electrical plugs and receptacles shall be equipped with a self-locking device that has a visual means of verifying correct engagement and locking.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0040 | | CAN segregation on connectors | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0068 | Verification : | Analysis |
| Definition:  The type of BPTU connectors shall be:   * Connector J1 : 8525 10 N 14B19 PNH 009 * Connector J2 : 8525 10 N 14B19 PWH 009   Segregation between CAN1 and CAN2 signals shall be taken into account at BPTU connectors’ level.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: The non-conformity is described on [IAD7] | | | | |

Implementation

Hereafter the definition of connectors signals:



Table 4‑2: BPTU connector’s description

Note:

BUS\_CAN1 correspond to the bus of the COM channel.

BUS\_CAN2 correspond to the bus of the MON channel.

The two connectors have not the same polarization to ensure they cannot be confused.

|  |  |
| --- | --- |
| **J2** | **J1** |
|  |  |

Figure 4‑6: BPTU connector’s pin allocation overview

#### Connectors’ studs

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1065-D | | Connectors’ studs | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  Connectors’ studs localization shall comply with [IAD2] paragraph “Electrical connections”, sub-paragraph “Connectors’ studs localizations".  Rationale:  This requirement is justified by mechanical interfaces specifications. | | | | |
| End\_Req | | | | |
| Notes: see [EAD6] . | | | | |

Implementation



Figure 4‑7: Connectors’ studs localizations

Studs information:

(2x4) Ø6.5mm for metallization

(2x4) Ø3.5mm for drill holes

Connectors J1 and J2 are on the board’s top face.

### Grounding and bonding

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0260 | | Bounding resistance | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0094 | Verification : | Test |
| Definition:  The BPTU bonding resistances shall be lower than 2.5 mOhm:   * From connector to housings, * From equipment box to parts between themselves, * From equipment grounding interface to nearest equipment box face.   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0265 | | Mechanical and electrical ground | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0096 | Verification : | Test |
| Definition:  Mechanical and electrical ground shall be linked by studs’ metallization.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0270 | | Insulation resistance | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0148 partial | Verification : | Test |
| Definition:  Equipment shall be designed for the insulation resistance as measured between the following points not to be lower than 10 mega Ohms:  Case 1 – Between all insulated terminals  Case 2 – Between all interconnected terminals and the reference case ground  Case 3 – Between electrical grounds and the reference case ground  Severity level  For case 1, the measurement shall be taken on equipment that may include no electronic component (i.e. just internal wiring and connectors) under 500V, according to MIL STD 202F.  For cases 2 and 3, the measurement shall be taken on complete equipment under 30V, according to MIL STD 202F. The measurement voltage tolerance is + or – 10%.  Test procedure MIL STD 202 F, method 302, condition B  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: “Terminal” means “Connector interface”. | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0280 | | Voltage test | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0149 | Verification : | Analysis and Test |
| Definition:  Tests conditions:   * Temperature: 15 to 25°C * Relative humidity: 40 to 70% * Pressure: 800 to 1100 hPa * Stabilisation time: 1 hour minimum   The test shall be performed:   * between electrical grounds and the reference case ground, * between insulated terminals, * between insulated terminals (including electrical supply terminals) and the reference case ground.   Severity level 28VDC power supply equipment shall withstand a voltage test higher or equal than 500VDC or 380VAC with duration between 0,1s to 60s.  Additional info: SPX240AV001E99 §6.4.2  Test procedure MIL STD 202 F, method 301  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation



Figure 4‑8: BPTU equipment grounding

The power supply is isolated from the rest of the board function (see 4.7.2).

HF link is represented by coupling capacitors (see 4.5 and 4.7).

## Acquisition channel

Acquisition channel’s input is an electromagnetic flow provided by a magnet. It is necessary to transform this electromagnetic flow into a voltage signal by a sensor. This voltage signal needs to be transformed into data to be sent to CAN controller. Referred to [IAD4] acquisition channel function has to implement:

* A function to detect the electromagnetic flow and to transform it into an electronic signal (§4.3.2 Magnet detection)
* A function to increase the electronic signal (§4.3.3 Instrumentation amplifier)
* A filter for the electronic signal (§4.3.4 Anti-aliasing filter)
* A function to transform the electronic signal into a digital information (§4.3.5 Analog to digital conversion)

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0370 | | Acquisitions channels architecture | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0045 | Verification : | Analysis |
| Definition:  The two sensor acquisitions and management of a same pedal shall be dissymmetrical.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

BPTU has two different acquisitions channels:

* Acquisition\_channel\_1 provides for α\_COM and β\_MON
* Acquisition\_channel\_2 provides for α\_MON and β\_COM

### Electromagnetic flow

The electromagnetic flow is provided by magnets. All magnets on BPTU have the same characteristics. However, for a same pedal, magnets are mounted in opposition phase.

For Acquisition\_channel\_1 the magnets are mounted for having a decreasing curve. **Magnet\_1 represents the magnet in front of Acquisition\_channel\_1.**

For Acquisition\_channel\_2 the magnets are mounted for having an increasing curve. **Magnet\_2 represents the magnet in front of Acquisition\_channel\_2.**

The magnetic air gap between magnet and sensor is 3.7mm ± 0.4mm (see [EAD6] )

The following table represents the electromagnetic flow for Magnet\_1 and Magnet\_2 when the pedal deflection is -16° to +16°:

|  |  |  |
| --- | --- | --- |
| Angle (°) | Magnet\_1 (Gauss) | Magnet\_2 (Gauss) |
| 16 | -160 | 160 |
| 10 | -110 | 110 |
| 6 | -55 | 55 |
| 0 | 0 | 0 |
| -6 | 55 | -55 |
| -10 | 110 | -110 |
| -16 | 160 | -160 |

Table 4‑3: Electromagnetic flow

### Magnet detection

In order to convert electromagnetic flow from magnet into analog signal, sensors are placed in front of magnet. The technology chosen is the hall-effect technology which is a sensor without contact.

**Note**: Quiescent Voltage Output represents the output when the input is BMagnet = 0 G.

Requirements

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0380 | | Sensor characteristics | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0005 | Verification : | Analysis |
| Definition:  Sensors characteristics shall be:   * Technology: Hall-effect technology * Sensitivity: 0.7 mV/Gauss < Sens < 1.7mV/Gauss * Supply voltage: VCC(nom) = 3.3V * Quiescent Voltage Output: VOUT(Q) = 1.65V ±0.05V.   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0390 | | Sensor duplication | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0006 partial  MBD\_X4\_BPTU\_ETS\_0001 partial | Verification : | Analysis |
| Definition:  Sensors shall be duplicated and dissimilar to provide two redundant position data:   * α1 sensor and α2 sensor shall be dissimilar, * β1 sensor and β2 sensor shall be dissimilar.   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes:   * α1 sensor and β2 sensor could be identical, * β1 sensor and α2 sensor could be identical. | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1070-D | | Sensors localization | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  Sensors localization shall comply with [IAD2] paragraph Electrical connections”, sub-paragraph “Sensors localizations".  Rationale:  This requirement is justified by mechanical interfaces specifications. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

To assure the segregation of COM and MON channel it is necessary to have two different hall-effect sensors, they will be named Hall-effect\_sensor\_1 and Hall-effect\_sensor\_2.

**Hall-effect\_sensor\_1 is used for α1 (COM) and β2 (MON).**

**Hall-effect\_sensor\_2 is used for α2 (MON) and β1 (COM).**

The following figure represents the hall-effect sensors localization on **BOTTOM** face and them identifications:

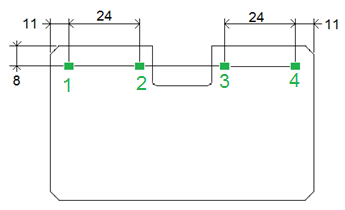
****

Figure 4‑9: Hall-effect sensors localization and identification

* α1 is referred 1,
* α2 is referred 2,
* β1 is referred 3, and,
* β2 is referred 4.

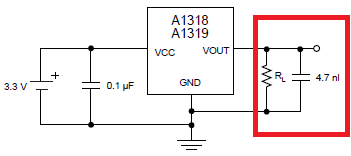
#### Hall-effect\_sensor\_1

The first source of hall-effect sensor is **A1318LLHLX-1-T** from **Allegro** (see [RD25] ). It will be named Hall-effect\_sensor\_1.

It has the following characteristic:

* **Sensor characteristic**:
  + Technology: Hall-effect technology
  + Sensitivity: Sens = 1.35mV/G
  + Noise: Ns = 2.3mG/
  + Quiescent Voltage Output: VOUT(Q) = 1.65V
* **Power supply characteristic**:
  + Absolute maximum ratings: VCC(max) = 8V
  + Supply voltage: VCC(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 10mA
  + Power supply: P = 33mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 150°C
  + Storage temperature: -65°C < TSTORAGE < 170°C

The datasheet of the Hall-effect\_sensor\_1 [RD25] shows a typical application circuit:



The output of the Hall-effect\_sensor\_1 is regulated by a 4.7nF capacitor and a 4.7kΩ resistor.

**Output:**

The following figure represents the theoretical output of Hall-effect\_sensor\_1:

Sensitivity: Sens = 1.35mV/G

Quiescent Voltage Output: VOUT(Q) = 1.65V

Formula:

Figure 4‑10: Hall-effect\_sensor\_1 output

#### Hall-effect\_sensor\_2

The second source of hall-effect sensor is **SS39ET-1-T** from **Honeywell** (see [RD26] ). It will be named Hall-effect\_sensor\_2.

It has the following characteristic:

* **Sensor characteristic**:
  + Technology: Hall-effect technology
  + Sensitivity: Sens = 0.891mV/G (see figure 7 of [RD26] and the following note)
  + Quiescent Voltage Output: VOUT(Q) = 1.65V
* **Power supply characteristic**:
  + Absolute maximum ratings: VCC(max) = 8V
  + Supply voltage: VCC(nom) = 3.3V
  + Stress default: S
  + Supply current: ICC(max) = 10mA
  + Power supply: P = 33mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 100°C
  + Storage temperature: -55°C < TSTORAGE < 165°C

The output of the Hall-effect\_sensor\_2 is regulated by a 4.7nF capacitor and a 4.7kΩ resistor.

Note: The sensitivity describe on table 1 of [RD26] is done for a power supply of 5V. To have the sensitivity when the hall-effect sensor is power supply by 3.3V, it is necessary to see the figure 7 of [RD26] .

**Output:**

The following figure represents the theoretical output of Hall-effect\_sensor\_2:

Sensitivity: Sens = 0.891mV/G

Quiescent Voltage Output: VOUT(Q) = 1.65V

Formula:

Figure 4‑11: Hall-effect\_sensor\_2 output

### Instrumentation amplifier

The Full Scale Range (FSR) of the data sent to CAN bus is -16° to +15.875° on 8 bits.

The outputs of the both hall-effect sensors have a too small FSR (Figure 4‑10and Figure 4‑11). It is necessary that the input of the ADC have a sufficient FSR.

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0400-D | | Acquisition channel FSR | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  The Hall-effect sensor output voltage shall be increased with an instrumentation amplifier before entering on ADCs inputs for each channel.  Rationale:  This requirement is justified by using the maximum FSR of ADC. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0410-D | | Instrumentation amplifier characteristics | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  The instrumentation amplifier shall have the following characteristics:   * Supply voltage: VCC(nom) = 3.3V * A gain defined by a resistor   Rationale:  This requirement is justified by having double source for each instrumentation amplifier | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0420 | | Instrumentation amplifier duplication | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0006 partial  MBD\_X4\_BPTU\_ETS\_0001 partial | Verification : | Analysis |
| Definition:  Instrumentation amplifier shall be duplicated and dissimilar to provide two redundant position data:   * α1 instrumentation amplifier and α2 instrumentation amplifier shall be dissimilar, * β1 instrumentation amplifier and β2 instrumentation amplifier shall be dissimilar.   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes:   * α1 instrumentation amplifier and β2 instrumentation amplifier could be identical, * β1 instrumentation amplifier and α2 instrumentation amplifier could be identical. | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0425-D | | Analogic gain | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  An adapted analogic gain shall be implemented for each channel.  Rationale:  This requirement is justified by having double source for each instrumentation amplifier | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

To assure the segregation of COM and MON channel it is necessary to have two different instrumentation amplifiers, they will be named Instrumentation\_amplifier\_1and Instrumentation\_amplifier\_2.

**Instrumentation\_amplifier\_1 is used for α1(COM) and β2(MON).**

**Instrumentation\_amplifier\_2 is used for α2(MON) and β1(COM).**

#### Instrumentation amplifier methodology

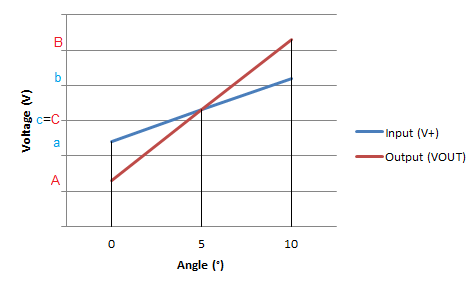


Figure 4‑12: The input and the output of instrumentation amplifier

|  |  |
| --- | --- |
|  | VOUT = (V+ - V-) x G + VREF  VOUT = (V+   * V- = * VREF = * G = |

Figure 4‑13: Instrumentation amplifier characteristics calculation

#### Instrumentation\_amplifier\_1

The first source of instrumentation amplifier is **INA333AIDGKT** from **Burr-Brown Corporation** (see [RD28] ). It will be named Instrumentation\_amplifier\_1.

It has the following characteristic:

* **Instrumentation amplifier characteristic**:
  + Gain:
* **Power supply characteristic**:
  + Absolute maximum ratings: VCC(max) = 7V
  + Supply voltage: VCC(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 0.075mA
  + Power supply: P = 0.2475mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 150°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

The datasheet of Instrumentation\_amplifier\_1 gives that information: so .

The output values of Hall-effect\_sensor\_1 are represented on Figure 4‑10.

Referred to Figure 4‑12 (instrumentation amplifier methodology):

Input and output elements:

a = 1.43

b = 1.85

c = 1.65 this represent Quiescent Voltage Output (VOUT(Q))

C = 1.65 this represent the middle of the full scale range wanted for the ADC

The output of instrumentation amplifier takes account the offset generate by preload pedal and electronic components. So, to do not amplify too much the signal and saturate it, the gain is chosen to represent the following full scale range:

A = 0.85

B = 2.50

So:

V- = VREF = 1.65V

G =

RG(th) = 34.1kΩ

So, the gain resistor chose is RG = 33kΩ and G = 4.03.

#### Instrumentation\_amplifier\_2

The second source of instrumentation amplifier is **AD8226ARMZ** from **Analog Devices** (see [RD27] ). It will be named Instrumentation\_amplifier\_2.

It has the following characteristic:

* **Instrumentation amplifier characteristic**:
  + Gain:
* **Power supply characteristic**:
  + Absolute maximum ratings: VCC(max) = 18V
  + Supply voltage: VCC(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 0.5mA
  + Power supply: P = 1.65mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 125°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

The datasheet of Instrumentation\_amplifier\_2 gives that information: so .

The output values of Hall-effect\_sensor\_2 are represented on Figure 4‑11.

Referred to Figure 4‑12 (instrumentation amplifier methodology):

Input and output elements:

a = 1.8

b = 1.5

c = 1.65 this represent Quiescent Voltage Output (VOUT(Q))

C = 1.65 this represent the middle of the full scale range wanted for the ADC

The output of instrumentation amplifier takes account the offset generate by preload pedal and electronic components. So, to do not amplify too much the signal and saturate it, the gain is chosen to represent the following full scale range:

A = 0.85

B = 2.50

So:

V- = VREF = 1.65V

G =

RG(th) = 10.98kΩ

So, the gain resistor chose is RG = 11kΩ and G = 5.5.

### Anti-aliasing filter

The acquisition channel includes an anti-aliasing filter before ADC.

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0430 | | Anti-aliasing filter | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0085 | Verification : | Analysis |
| Definition:  Anti-aliasing low-pass filtering shall be implemented before analog to digital conversion.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

An anti-aliasing filter shall be placed before the ADC.

The anti-aliasing filter is a first order low-pass filter (RC) constitute with:

* R = 22kΩ
* C = 330pF

### Analog to digital conversion

Requirements

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0440 | | ADC duplication and dissimilarity | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0006 partial  MBD\_X4\_BPTU\_ETS\_0001 partial | Verification : | Analysis |
| Definition:  ADC shall be duplicated and dissimilar to provide two redundant position data:   * α1 ADC and α2 ADC shall be dissimilar, * β1 ADC and β2 ADC shall be dissimilar.   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes:   * α1 ADC and β2 ADC could be identical, * β1 ADC and α2 ADC could be identical. | | | | |

Note: Beq is the amplifier equivalent noise bandwidth.

Accuracy calculation for Acquisition\_channel\_1:

* Sensor sensitivity: Sens = 1.35mV/G (see 4.3.2.1)
* Sensor noise: Ns = 2.3mG/ (see 4.3.2.1)
* Bandwidth: B-3dB = 22KHz ; Beq = 34.4KHz ( ) (see 4.3.4)
* Amplifier gain: G = 4 (see 4.3.3.2)
* Accuracy for the ADC\_1:

ADC full scale: the ADC will acquire an analogic signal between 0V and 3.3V 🡪 FSR = 3.3V

N ≤ 12

Accuracy calculation for Acquisition\_channel\_2:

* Sensor sensitivity: Sens = 0.891mV/G (see 4.3.2.2)
* Sensor noise: Ns = 2.3mG/ (No information, the noise of Hall-effect\_sensor\_1 is used for the accuracy calculation)
* Bandwidth: B-3dB = 22KHz ; Beq = 34.4KHz ( ) (see 4.3.4)
* Amplifier gain: G = 4.29 (see 4.3.3.2)
* Accuracy for the ADC\_2:

ADC full scale: the ADC will acquire an analogic signal between 0V and 3.3V 🡪 FSR = 3.3V

N ≤ 12

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0450-D | | ADC accuracy | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  The accuracy of ADC shall be 12bits.  Rationale:  This requirement is justified by calculation. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0455-D | | ADC characteristics | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  ADC characteristics shall be:   * DNL: < 1 LSB * Conversion time: < 2µs * Interface: Serial * Supply voltage: VCC(nom) = 3.3V   Rationale:  This requirement is justified by the inter-operability between components. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

The anti-aliasing filter (see 4.3.4) has a bandwidth frequency of .

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0458-D | | ADC sample rate | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  System acquisition sample rate shall be lower than 22 kHz.  Rationale:  This requirement is justified by the inter-operability between components. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

To assure the segregation of COM and MON channel it is necessary to have two different ADC, they will be named ADC\_1 and ADC\_2.

**ADC\_1 is used for α1(COM) and β2(MON).**

**ADC\_2 is used for α2(MON) and β1(COM).**

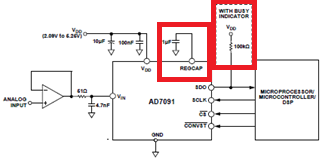
#### ADC\_1

The first source of ADC is **AD7091BCPZ** from **Analog Devices** (see [RD29] ). It will be named ADC\_1.

It has the following characteristic:

* **ADC characteristic**:
  + Accuracy: 12 bits
  + DNL: ±0.9 LSB
  + Conversion time: 650ns
  + Interface: Serial
  + Low level output voltage: VOL(max) = 0.4V
  + High level output voltage: VOH(min) = 3.1V
  + Low level input voltage: VIL(max) = 0.99V
  + High level input voltage: VIH(min) = 2.31V
* **Power supply characteristic**:
  + Absolute maximum ratings: VCC(max) = 7V
  + Supply voltage: VCC(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 0.4mA
  + Power supply: P = 1.32mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 125°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

The datasheet of the ADC\_1 shows a typical application circuit:



A capacitor of 1µF is connected between the net REGCAP and the ground.

A resistor of 100kΩ is connected between the net SDO and the power supply.

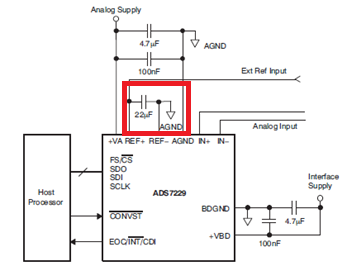
#### ADC\_2

The second source of ADC is **ADS7229\_TSSOP** from **Texas Instruments** (see [RD30] ). It will be named ADC\_2.

It has the following characteristic:

* **ADC characteristic**:
  + Accuracy: 12 bits
  + DNL: ±0.5 LSB
  + Conversion time: 1125ns
  + Interface: Serial
  + Low level output voltage: VOL(max) = 0.4V
  + High level output voltage: VOH(min) = 2.7V
  + Low level input voltage: VIL(max) = 1.155 V
  + High level input voltage: VIH(min) = 2.145V
* **Power supply characteristic**:
  + Absolute maximum ratings: VCC(max) = 7V
  + Supply voltage: VCC(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 6mA
  + Power supply: P = 25.2mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 85°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

The datasheet of the ADC\_2 shows a typical application circuit:



A capacitor of 22µF is connected between the net REF- and REF+.

### Acquisition channel conclusion

There are two different acquisition channels:

* Acquisition\_channel\_1 for α1 COM and β2 MON
* Acquisition\_channel\_2 for α2 MON and β1 COM.
* Acquisition\_channel\_1 for α1 COM and β2 MON:



Figure 4‑14: Acquisition\_channel\_1

* Acquisition\_channel\_2 for α2 MON and β1 COM:



Figure 4‑15: Acquisition\_channel\_2

## Processing

Processing function is provided by FPGA (**F**ield-**P**rogrammable **G**ate **A**rray).

To insure the segregation of COM and MON channel it is necessary to have two different FPGA. They will be named on the rest of the document respectively FPGA\_COM and FPGA\_MON.

### FPGA\_COM

#### Component

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0470-D | | FPGA\_COM | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  FPGA for COM channel shall be **ProASIC3 A3P1000 FG144I** from **Microsemi.**  Rationale:  Flash technology used on this component is less sensible to SEU embedded protection. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

The first source of FPGA is **ProASIC3 A3P1000 FG144I** from **Microsemi** (see [RD31] ). It will be named FPGA\_COM.

It has the following characteristic:

* **FPGA characteristic**:
  + I/O number: 144
  + Low level output voltage: VOL(max) = 0.4V
  + High level output voltage: VOH(min) = 2.4V
  + Low level input voltage: VIL(min) = -0.3V to VIL(max) = 0.8V
  + High level input voltage: VIH(min) = 2V to VIH(max) = 3.6V
* **Power supply characteristic for IO voltage**:
  + Absolute maximum ratings: VIO(max) = 3.75V
  + Supply voltage: VIO(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 256.3mA
  + Power supply: P = 384.4mW
* **Power supply characteristic for core voltage**:
  + Absolute maximum ratings: VCC(max) = 1.65V
  + Supply voltage: VCC(nom) = 1.5V
  + Stress default:
  + Supply current: ICC(max) = 6.25mA
  + Power supply: P = 20.63mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 85°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

#### JTAG for FPGA\_COM

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0475-D | | JTAG for FPGA\_COM | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  JTAG connection shall be implemented with a 8 pins connector for FPGA\_COM. JTAG connection shall be compliant with [RD31] .  Rationale:  This requirement is for implemented hardware on FPGA\_COM. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

JTAG connector for FPGA\_COM has a 1.27mm’s spacing instead of usual 2.56mm. It is placed on the BOTTOM face of the board to program FPGA\_COM after the rear cover was mounted.

JTAG connector for FPGA\_COM is **FTSH-104-04-F-DV** from **Samtec** (see [RD37] ).

It has the following characteristic:

Pins number: 8

#### Pinout

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0680-D | | FPGA\_COM pinout | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  FPGA\_COM shall follow the following pinout:    FPGA\_COM pinout  Other FPGA\_COM’s pins shall be in accordance with [RD31] .  Rationale:  This requirement is justified by schematic implementation. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

### FPGA\_MON

#### Components

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0480-D | | FPGA\_MON | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  FPGA for MON channel shall be **IGLOO2 M2GL050 VF400** from **Microsemi.**  Rationale:  Flash technology used on this component is less sensible to SEU embedded protection. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

The second source of FPGA is **IGLOO2 M2GL050 VF400** from **Actel**. It will be named FPGA\_MON.

It has the following characteristic:

* **FPGA characteristic**:
  + I/O number: 400
  + Low level output voltage: VOL(max) = 0.4V
  + High level output voltage: VOH(min) = 2.9V
  + Low level input voltage: VIL(min) = -0.3V to VIL(max) = 0.8V
  + High level input voltage: VIH(min) = 2V to VIH(max) = 3.45V
* **Power supply characteristic for IO voltage**:
  + Absolute maximum ratings: VIO(max) = 3.63V
  + Supply voltage: VIO(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 100mA
  + Power supply: P = 120mW
* **Power supply characteristic for core voltage**:
  + Absolute maximum ratings: VCC(max) = 1.32V
  + Supply voltage: VCC(nom) = 1.2V
  + Stress default:
  + Supply current: ICC(max) = 6.25mA
  + Power supply: P = 20.63mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 100°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

#### JTAG for FPGA\_MON

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0485-D | | JTAG for FPGA\_MON | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  JTAG connection shall be implemented with a 8 pins connector for FPGA\_MON. JTAG connection shall be compliant with [RD32] .  Rationale:  This requirement is for implemented hardware on FPGA\_MON. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

JTAG connector for FPGA\_MON has a 1.27mm’s spacing instead of usual 2.56mm. It is placed on the BOTTOM face of the board to program FPGA\_MON after the rear cover was mounted.

JTAG connector for FPGA\_MON is **FTSH-104-04-F-DV** from **Samtec** (see [RD37] ).

It has the following characteristic:

Pins number: 8

#### Pinout

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0690-D | | FPGA\_MON pinout | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  FPGA\_MON shall follow the following pinout:    FPGA\_MON pinout  Other FPGA\_MON’s pins shall be in accordance with [RD32] .  Rationale:  This requirement is justified by schematic implementation. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

### FPGA reset

At BPTU power up, the FPGA cannot start until input voltage is sufficient. In addition, the FPGA should not operate when BPTU is powered down. To insure these conditions a reset shall be provided.

The two power supplies rise time are different for COM and MON (see 4.7.3.2 and 4.7.4.2) so the reset for each FPGA are different.

#### Reset for FPGA\_COM

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1010-D | | Reset for FPGA\_COM | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  The board shall implement a reset function in order to ensure the correct driving of FPGA\_COM component.  Rationale:  This requirement is for protect data sending by FPGA. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

The reset is provided by a 10µF ± 20% capacitor and a 10kΩ ± 1% resistor from the COM channel 3.3V. A 100Ω resistor is between the reset function and the FPGA to limit the input current.



Figure 4‑16: Reset for FPGA\_COM

± 21ms

High level input voltage of FPGA\_COM: VIH(min) = 2V

The FPGA\_COM will start when:

± 19.5ms

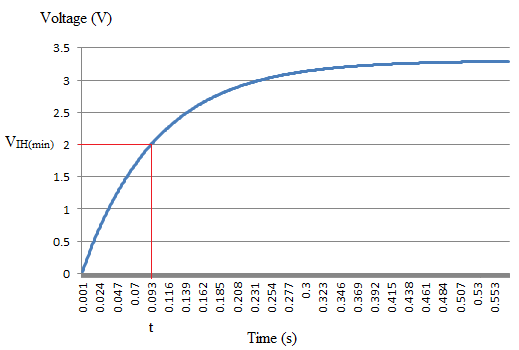


Figure 4‑17: FPGA\_COM reset curve

The reset on FPGA\_COM is on pin G10 (GCC2/IO96PDB1).

To ensure easy transition from powered-off state to the powered-up state, it is necessary that FPGA\_COM has a proper reset signal.

The following information comes from [RD31]

|  |
| --- |
| There are five regions to consider during power-up.  ProASIC3 I/Os are activated only if ALL of the following three conditions are met:  1. VCC and VCCI are above the minimum specified trip points (see the following figure).  2. VCCI > VCC – 0.75 V (typical)  3. Chip is in the operating mode.  VCCI Trip Point:  Ramping up: 0.6 V < trip\_point\_up < 1.2 V  Ramping down: 0.5 V < trip\_point\_down < 1.1 V  VCC Trip Point:  Ramping up: 0.6 V < trip\_point\_up < 1.1 V  Ramping down: 0.5 V < trip\_point\_down < 1 V  VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically  built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:  • During programming, I/Os become tristated and weakly pulled up to VCCI.  • JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O  behavior. |

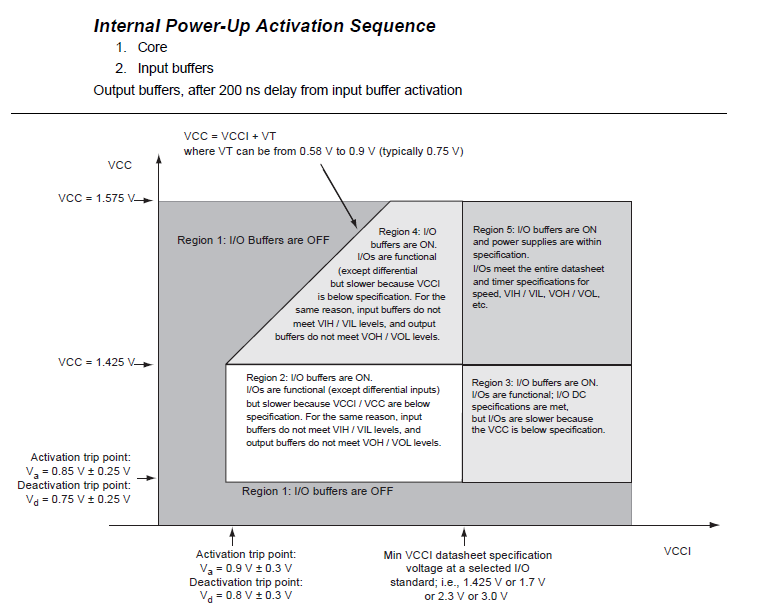


Figure 4‑18: FPGA\_COM Internal Power-Up Activation Sequence

#### Reset for FPGA\_MON

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1030-D | | Reset for FPGA\_MON | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  The board shall implement a reset function in order to ensure the correct driving of FPGA\_MON component.  Rationale:  This requirement is for protect data sending by FPGA. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

The reset is provided by a 4.7µF ± 20% capacitor and a 10kΩ ± 1% resistor from the MON channel 3.3V. A 100Ω resistor is between the reset function and the FPGA to limit the input current.



Figure 4‑19: Reset for FPGA\_MON

± 10ms

High level input voltage of FPGA\_MON: VIH(min) = 2V

The FPGA\_MON will start when:

± 9.2ms

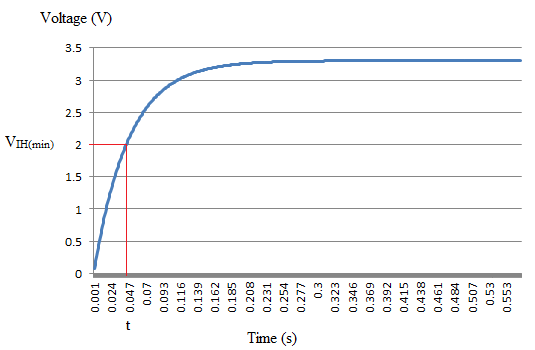


Figure 4‑20: FPGA\_MON reset curve

The reset on FPGA\_MON is on pin H20 (MSIO20NB3/GB13/VCCC\_SE1\_CLKI).

To ensure easy transition from powered-off state to the powered-up state, it is necessary that FPGA\_MON has a proper reset signal.

The following information comes from [RD32] :

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Symbol | Parameter | Limit min | Limits max | Units |
| VDD | DC core supply voltage. Must always power this pin. | –0.3 | 1.32 | V |
| VPP | Power supply for charge pumps (for normal operation and programming). Must always power this pin. | –0.3 | 3.63 | V |

Table 4‑4: FPGA MON Absolute Maximum Ratings

### FPGA\_oscillator

FPGA components need an external clock provided by an oscillator.

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1100 | | Oscillators dissimilarity | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0001 partial | Verification : | Analysis |
| Definition:  Oscillators shall be dissimilar between COM and MON channel.  Rationale:  This requirement provides dissimilarity between COM and MON channels. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1110-D | | Oscillators characteristics | Version: | 1 |
|  | Covers: | Derived | Verification : | Test |
| Definition:  Oscillators characteristics shall be:   * Frequency: 16MHz ± 800Hz (50ppm) * Duty cycle: 50% ± 10% * Supply voltage: VCC(nom) = 3.3V   Rationale:  This requirement provides the clock characteristics of the FPGA. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

#### FPGA\_oscillator\_COM

The first source of oscillator is **SG-310 SCF 16.000000MHzL** from **Epson Toyocom**. It will be named Oscillator\_COM.

It has the following characteristic:

* **Oscillator characteristic**:
  + Frequency: 16MHz
  + Duty cycle: 50% ± 5%
* **Power supply characteristic**:
  + Absolute maximum ratings: VCC(max) = 8V
  + Supply voltage: VCC(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 3.5mA
  + Power supply: P = 11.55mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 85°C
  + Storage temperature: -40°C < TSTORAGE < 125°C

#### FPGA\_oscillator\_MON

The second source of oscillator is **16.000MHz XO32025UITA** from **EuroQuartz**. It will be named Oscillator\_MON.

It has the following characteristic:

* **Oscillator characteristic**:
  + Frequency: 16MHz
  + Duty cycle: 50% ± 5%
* **Power supply characteristic**:
  + Absolute maximum ratings: VCC(max) = 8V
  + Supply voltage: VCC(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 15mA
  + Power supply: P = 49.5mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 85°C
  + Storage temperature: -55°C < TSTORAGE < 100°C

### PIN\_PROG

On a helicopter there are two BPTU modules: one for the pilot and one for the co-pilot. The difference between pilot and co-pilot is given by PIN\_PROG nets on connector J2. BPTU allows Pilot/Copilot frames transmission through pin programming configuration.

The following figure represents the J2 connector with the PIN\_PROG connection:

|  |  |  |
| --- | --- | --- |
| **J2** | | |
|  | | |
| U | PIN\_PROG\_1 | Type: SPX880AZ126 DI003 |
| Pilot BPTU: high impedance (3mA) |
| Co-pilot BPTU: shunted to J2-P on H/C side |
| T | PIN\_PROG\_2 | Type: SPX880AZ126 DI003 |
| Co-pilot BPTU: high impedance (3mA) |
| Pilot BPTU: shunted to J2-P on H/C side |
| P | PIN\_PROG\_COM | Internally grounded |
| Shunted to J2-U or J2-T on H/C side |

Figure 4‑21: PIN\_PROG connection

#### PIN\_PROG\_COM connection

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0510-D | | PIN\_PROG\_COM | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis and Test |
| Definition:  PIN\_PROG\_COM shall be connected to GND\_SYS.  Rationale:  This requirement is justified by [RD4] | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

PIN\_PROG\_COM (pin P of J2 connector) is directly connected to GND\_SYS.

#### PIN\_PROG\_1 and PIN\_PROG\_2 protection

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0515 | | PIN\_PROG EMC protection | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0091 partial | Verification : | Analysis and Test |
| Definition:  PIN\_PROG\_1 and PIN\_PROG\_2 inputs shall implement EMC protection.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

A π filter is placed between:

* PIN\_PROG\_1 and FPGA\_COM,
* PIN\_PROG\_2 and FPGA\_COM and
* PIN\_PROG\_1 and FPGA\_MON,
* PIN\_PROG\_2 and FPGA\_MON.

Each π filter has the following characteristics:

|  |  |
| --- | --- |
|  | * L1 = 11µH * C1 = C2 = 100pF |

Figure 4‑22: PIN\_PROG protection

The π filter reduces the input and the output disturbances.

#### PIN\_PROG\_1 and PIN\_PROG\_2 interface

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0520 | | PIN\_PROG interfaces | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0158 | Verification : | Analysis |
| Definition:  PIN\_PROG\_1 and PIN\_PROG\_2 interfaces shall be in accordance with [RD4] type DI003.  Rationale:  This requirement is justified [RD4] | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

A diode and a 10kΩ pull-up resistor are placed between PIN\_PROG\_1 and each FPGA.

A diode and a 10kΩ pull-up resistor are placed between PIN\_PROG\_2 and each FPGA.

Note: The 10kΩ resistors are pulled-up to 3.3V power supply.



Figure 4‑23: PIN\_PROG interface

Legend: “i” means “1” or “2”.

#### Pilot/Co-pilot identification

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0530 | | PIN\_PROG position | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0009 | Verification : | Analysis and Test |
| Definition:  Each BPTU position shall be identified thanks to its pin-programming bit 1 and 2 according to the following table:   |  |  |  | | --- | --- | --- | | BPTU Position | PIN\_PROG\_2 | PIN\_PROG\_1 | | Pilot | 0 | 1 | | Co-pilot | 1 | 0 |   **BPTU Pilot/Co-pilot information**  Other combinations are inconsistent.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

### DEVICE ID

The board has two different FPGA components which have a unique code.

COM and MON channels transmit respectively on CAN bus 1 and CAN bus2.

ADC\_α\_COM and ADC\_β\_MON are represented by ADC\_1. ADC\_α\_MON and ADC\_β\_COM are represented by ADC\_2.

In order to differentiate frames to send on CAN bus 1 and 2 and to differentiate the angle of each ADC, each FPGA component is configured as FPGA\_COM or FPGA\_MON channel through Device ID configuration pins.

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0540 | | COM/MON programming | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0001 partial | Verification : | Analysis and Test |
| Definition:  To identify the FPGA channel, Device\_ID signals shall be connected in accordance with the following table:   |  |  |  | | --- | --- | --- | | Device\_ID\_COM\_3 | Device\_ID\_COM\_2 | Device\_ID\_COM\_1 | | 1 | 0 | 1 | | Device\_ID\_MON\_3 | Device\_ID\_MON\_2 | Device\_ID\_MON\_1 | | 0 | 1 | 0 |   BPTU COM/MON connections  Rationale:  This requirement is by the common code on FPGA. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

FPGA inputs are connected with:

* a 10kΩ pull-down resistor to GND\_SYS for 0 logic level,
* a 10kΩ pull-up resistor to 3.3V\_COM for 1 logic level on COM channel,
* a 10kΩ pull-up resistor to 3.3V\_MON for 1 logic level on MON channel.

Names nets shall be noted on schematic.

### SILKAN PROG

On each connector there are 6 nets for SILKAN programming:

|  |  |  |  |
| --- | --- | --- | --- |
| **J1** | | **J2** | |
|  | |  | |
| D | SILKAN\_COM\_0 | J | SILKAN\_MON\_0 |
| C | SILKAN\_COM\_1 | H | SILKAN\_MON\_1 |
| B | SILKAN\_COM\_2 | G | SILKAN\_MON\_2 |
| A | SILKAN\_COM\_3 | F | SILKAN\_MON\_3 |
| N | SILKAN\_COM\_4 | E | SILKAN\_MON\_4 |
| P | SILKAN\_COM\_5 | D | SILKAN\_MON\_5 |

Figure 4‑24: SILKAN\_PROG connection

On the current architecture SILKAN\_COM\_4, SILKAN\_COM\_5, SILKAN\_MON\_4 and SILKAN\_MON\_5 nets are not used.

SILKAN nets provide a maintenance mode. In this mode, an external software dialog with the FPGA to load the EEPROM memory contents.

#### SILKAN PROG protection

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0545 | | SILKAN\_PROG EMC protection | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0091 partial | Verification : | Analysis and Test |
| Definition:  SILKAN inputs shall implement EMC protection.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

A π filter is placed between:

* SILKAN\_COM\_0 and each FPGA\_COM,
* SILKAN\_COM\_1 and each FPGA\_COM,
* SILKAN\_COM\_2 and each FPGA\_COM,
* SILKAN\_COM\_3 and each FPGA\_COM and
* SILKAN\_MON\_0 and each FPGA\_MON,
* SILKAN\_MON\_1 and each FPGA\_MON,
* SILKAN\_MON\_2 and each FPGA\_MON,
* SILKAN\_MON\_3 and each FPGA\_MON.

Each π filter has the following characteristics:

|  |  |
| --- | --- |
|  | * L1 = 11µH * C1 = C2 = 100pF |

Figure 4‑25: SILKAN PROG protection

The π filter reduces the input and the output disturbances.

#### COM Channel mode

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0550-D | | Maintenance mode for COM channel | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis and Test |
| Definition:  FPGA\_COM shall be on maintenance mode when SILKAN\_COM\_0 and SILKAN\_COM\_1 signals are tied to ground.  Rationale:  This requirement is by enter having a maintenance mode and a normal mode. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0555-D | | Normal mode for COM channel | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis and Test |
| Definition:  FPGA\_COM shall be on normal mode when SILKAN\_COM\_0 and SILKAN\_COM\_1 signals are pulled to 3.3V.  Rationale:  This requirement is by enter having a maintenance mode and a normal mode. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

To implement the maintenance mode, SILKAN\_COM\_0 and SILKAN\_COM\_1 have the same interface than PIN\_PROG\_1 and PIN\_PROG\_2 (see 4.4.5.3)

A diode and a 10kΩ pull-up resistor are placed between SILKAN\_COM\_0 and FPGA\_COM.

A diode and a 10kΩ pull-up resistor are placed between SILKAN\_COM\_1 and FPGA\_COM.



Figure 4‑26: SILKAN PROG interface

#### COM Channel communication

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0560-D | | Communication on maintenance mode for COM channel | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis and Test |
| Definition:  FPGA\_COM shall communicate through SILKAN\_COM\_2 and SILKAN\_COM\_3 on maintenance mode by RS232 liaison.  Rationale:  This requirement is justified by the necessity of received the offset and the gain information without open BPTU. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

RS-232 liaison needs direct connection to work without diode or pull-up.

#### MON Channel mode

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0570-D | | Maintenance mode for MON channel | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis and Test |
| Definition:  FPGA\_MON shall be on maintenance mode when SILKAN\_MON\_0 and SILKAN\_MON\_1 signals are tied to ground.  Rationale:  This requirement is by enter having a maintenance mode and a normal mode. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0575-D | | Normal mode for MON channel | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis and Test |
| Definition:  FPGA\_MON shall be on normal mode when SILKAN\_MON\_0 and SILKAN\_MON\_1 signals are pulled to 3.3V.  Rationale:  This requirement is by enter having a maintenance mode and a normal mode. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

To implement the maintenance mode, SILKAN\_MON\_0 and SILKAN\_MON\_1 have the same interface than PIN\_PROG\_1 and PIN\_PROG\_2 (see 4.4.5.3)

A diode and a 10kΩ pull-up resistor are placed between SILKAN\_MON\_0 and FPGA\_MON.

A diode and a 10kΩ pull-up resistor are placed between SILKAN\_MON\_1 and FPGA\_MON.



Figure 4‑27: SILKAN PROG interface

#### MON Channel communication

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0580-D | | Communication on maintenance mode for MON channel | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis and Test |
| Definition:  FPGA\_MON shall communicate through SILKAN\_MON\_2 and SILKAN\_MON\_3 on maintenance mode by RS232 liaison.  Rationale:  This requirement is justified by the necessity of received the offset and the gain information without open BPTU. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

RS-232 liaison needs direct connection to work without diode or pull-up.

### FPGA digital processing

Data sending by the two ADC of the acquisition channels shall:

* Take account of channel offset,
* Take account of channel gain,
* Multiply acquisitions and make an average,
* Take account of the magnet orientation,

#### Maintenance mode operation

Each channel has an offset different due to board components and preload adjustment. To guarantee correct measurements, a maintenance mode on each board is available. During this maintenance mode, the offset of each channel is set on an external EEPROM.

Each channel also has a different gain due to mechanic tolerances and components tolerances. To guarantee correct measurements, during the maintenance mode, the gain calibration of each channel is set on an external EEPROM.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0590-D | | Maintenance mode operation for COM channel | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  In the maintenance mode, FPGA\_COM shall sent on 12 bits an average of 0° and 10° for ADC\_1 and ADC\_2 through SILKAN\_COM\_2 (RS232 Tx liaison) to an external program.  Rationale:  This requirement is implemented to increase the accuracy of the measurement. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0600-D | | Offset and gain information for COM channel | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis and Test |
| Definition:  In the maintenance mode, FPGA\_COM shall store into EEPROM\_COM the offset and the gain information for ADC\_1 and ADC\_2 return by RS232 liaison through SILKAN\_COM\_3 (RS232 Rx liaison).  Rationale:  This requirement is implemented to increase the accuracy of the measurement. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0610-D | | Maintenance mode operation for MON channel | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  In the maintenance mode, FPGA\_MON shall sent on 12 bits an average of 0° and 10° for ADC\_1 and ADC\_2 through SILKAN\_MON\_2 (RS232 Tx liaison) to an external program.  Rationale:  This requirement is implemented to increase the accuracy of the measurement. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0620-D | | Offset and gain information for MON channel | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis and Test |
| Definition:  In the maintenance mode, FPGA\_MON shall store into EEPROM\_MON the offset and the gain information for ADC\_1 and ADC\_2 return by RS232 liaison through SILKAN\_MON\_3 (RS232 Rx liaison).  Rationale:  This requirement is implemented to increase the accuracy of the measurement. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

#### Magnet orientation

The [RD24] document shows that magnets are placed in two different ways:

* The negative way for α COM and β MON (ADC\_1)
* The positive way for α MON and β COM (ADC\_2)

The table hereafter shows the correspondence between angle and hexadecimal data for some examples which arrived from ADC to FPGA:

|  |  |
| --- | --- |
| **ADC 1** | |
| **Angle (°)** | **Data (12 bits hexadecimal)** |
| 15.875° | 0x000 |
| 10° | 0x2FF |
| 0° | 0x7FF |
| -10° | 0xCFF |
| -16° | 0xFFF |
| **ADC 2** | |
| **Angle (°)** | **Data (12 bits hexadecimal)** |
| 15.875° | 0xFFF |
| 10° | 0xD00 |
| 0° | 0x800 |
| -10° | 0x300 |
| -16° | 0x000 |

Table 4‑5: Correspondence between hexadecimal data and angle

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0630-D | | Magnet orientation | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  When FPGA receive data from ADC\_1 it shall apply to them the following formula:  Y[11:0] = not X[11:0]  Where:   * X represents the acquisition data * Y represents the acquisition data treated   Rationale:  This requirement is justified by the magnet orientation | | | | |
| End\_Req | | | | |
| Notes: No equal treatment for data from ADC\_2. | | | | |

#### Digital processing

The FPGA makes an adequate average of several data to reduce noise.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0640-D | | Digital processing | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  Adequate digital low-pass filtering of the pedal deflection shall be implemented before sending on the CAN bus.  Rationale:  This requirement is implemented to increase the accuracy of the measurement. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

#### Data treatment

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0650-D | | Data treatment | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  Data treatment shall integer the gain and offset information for each channel with the following formula:  Y = A.X +B  Where:   * A represents the channel gain, * B represents the channel offset, * X represents the acquisition data * Y represents the acquisition data treated   Rationale:  This requirement is implemented to increase the accuracy of the measurement. | | | | |
| End\_Req | | | | |
| Notes: see BRD-BPTU-0600 and BRD-BPTU-0620 | | | | |

#### Acquisition full scale range

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0655 | | Acquisition full scale range | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0025 | Verification : | Analysis |
| Definition:  The BPTU shall measure pilot’s brake order through the pedals angle from MIN to MAX (useful range).  MAX = +15° due to AH tolerances.  MIN is strictly lower than 0° and strictly higher than -3°, the value is to be announced by the supplier, depending on BPTU tolerances  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes:  A monitoring will be triggered at system level when the pedal angle is out of useful range.  When the angle is out of the full scale range (MIN to MAX), the BPTU shall sent the OOR on CAN bus. | | | | |

### EEPROM

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0670 | | EEPROM | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0015  MBD\_X4\_BPTU\_ETS\_0102 | Verification : | Analysis and Test |
| Definition:  EEPROM shall contain:   * HW part number, * HW serial number, * PLD identification number, * Frame ID for CAN bus (36), * Calibration information (offset and gain), * VIN(min), VIN(max), V3.3V(min) and V3.3V(max), * Threshold for Out Of Range.   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0673 | | EEPROM dissimilarity | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0001 partial | Verification : | Analysis |
| Definition:  EEPROM shall be dissimilar between COM and MON channel.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0675-D | | EEPROM characteristics | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  EEPROM characteristics shall be:   * Memory: 64k * Interface: Serial I²C * Supply voltage: VCC(nom) = 3.3V * Package : TSSOP   Rationale:  This requirement is justified by the inter-operability between components. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0678-D | | EEPROM address | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  EEPROM chip address inputs shall be:   * A0 connected to 3.3V * A1 connected to GND\_SYS * A3 connected to 3.3V   Rationale:  This requirement is justified by having a common code for each FPGA. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

#### EEPROM\_COM

The first source of EEPROM is **24LC64-E/ST** from **Microship** (see [RD33] ). It will be named EEPROM\_COM.

It has the following characteristic:

* **EEPROM characteristic**:
  + Memory: 64k
  + Interface: Serial I²C
  + Package : TSSOP
  + Low level output voltage: VOL(max) = 0.4V
  + Low level input voltage: VIL(max) = 0.99V
  + High level input voltage: VIH(min) = 2.31V
* **Power supply characteristic**:
  + Absolute maximum ratings: VCC(max) = 6.5V
  + Supply voltage: VCC(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 3mA
  + Power supply: P = 9.9mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 125°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

A0 is cable to 3.3V\_COM.

A1 is cable to GND\_SYS.

A2 is cable to 3.3V\_COM.

#### EEPROM\_MON

The second source of EEPROM is **M24C64-WDW6TP** from **ST** (see [RD34] ). It will be named EEPROM\_MON.

It has the following characteristic:

* **EEPROM characteristic**:
  + Memory: 64k
  + Interface: Serial I²C
  + Package : TSSOP
  + Low level output voltage: VOL(max) = 0.99V
  + High level output voltage: VOH(min) = 2.31V
  + Low level input voltage: VIL(max) = 0.66V
  + High level input voltage: VIH(min) = 2.64V
* **Power supply characteristic**:
  + Absolute maximum ratings: VCC(max) = 6.5V
  + Supply voltage: VCC(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 2mA
  + Power supply: P = 6.6mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 125°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

A0 is cable to 3.3V\_MON.

A1 is cable to GND\_SYS.

A2 is cable to 3.3V\_MON.

## CAN interface

Hereafter a schematic for the CAN interface:



Figure 4‑28: CAN interface architecture

Bus CAN COM is on J1 connector and bus CAN MON is on J2 connector:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **J1** | | | **J2** | | |
|  | | |  | | |
| K | BUS\_CAN1\_Hi | Iso 11898 interface | A | BUS\_CAN2\_Hi | Iso 11898 interface |
| ARINC 825, CAN 2.0B extended | ARINC 825, CAN 2.0B extended |
| M | BUS\_CAN1\_Lo | 500 Kbps data rate | C | BUS\_CAN2\_Lo | 500 Kbps data rate |
| Big Endian transmission | Big Endian transmission |

### CAN Controller

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0700-D | | Can controller COM | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  CAN controller for COM channel is included on FPGA\_COM.  Rationale:  This requirement optimizes components repartition on the board. It reduces component’s number. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0710-D | | Can controller MON | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  CAN controller for MON channel is included on FPGA\_MON.  Rationale:  This requirement optimizes components repartition on the board. It reduces component’s number. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0715 | | Can controller characteristics | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0074 partial | Verification : | Analysis |
| Definition:  CAN controller shall comply with [RD2] follow this requirements:   * 500 kbps data rate, * Big Endian transmission, * When CAN controller(s) reach(es) Bus off state, the application (i.e. software) shall wait at least one second before initiating a Normal Mode Request of the CAN controller(s). * The maximum number of re-attachments of CAN controllers shall be 3 between a power on and power off cycle. That means 3 re-attachments are allowed for each CAN controller in the defined timeframe.     CAN progress of transmission (Big Endian)  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0720 | | CAN messages COM | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0159  MBD\_X4\_BPTU\_ETS\_0161 | Verification : | Analysis and Test |
| Definition:  CAN messages from COM channel shall comply with the following tables:    Pilot BPTU CAN1 module transmission frames    Co-pilot BPTU CAN1 module transmission frames  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0730 | | CAN messages MON | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0160  MBD\_X4\_BPTU\_ETS\_0162 | Verification : | Analysis and Test |
| Definition:  CAN messages from MON channel shall comply with the following tables:    Pilot BPTU CAN2 module transmission frames    Co-pilot BPTU CAN2 module transmission frames  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0732 | | BPTU modules transmission data | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0163 | Verification : | Analysis and Test |
| Definition:  The BPTU modules transmission data shall be as follows:  xxx = Pil or Copil  j = 1 or 2    BPTU modules transmission data  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0735-D | | BPTU modules PBIT word definition | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis and Test |
| Definition:  The BPTU modules transmission data on PBIT shall be as follows:  xxx = Pil or Copil  j = 1 or 2    BPTU modules PBIT word definition  Rationale:  This requirement develops the PBIT word definition. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0738-D | | BPTU modules CBIT word definition | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis and Test |
| Definition:  The BPTU modules transmission data on CBIT shall be as follows:  xxx = Pil or Copil  j = 1 or 2    BPTU modules CBIT word definition  Rationale:  This requirement develops the CBIT word definition. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0725 | | Can messages format | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0075 | Verification : | Analysis |
| Definition:  CAN messages format shall comply with [RD3] requirements.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

### CAN transceivers

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1120 | | CAN transceivers dissimilarity | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0001 partial | Verification : | Analysis |
| Definition:  CAN transceivers shall be dissimilar between COM and MON channel.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1130 | | CAN transceivers characteristics | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0074 partial | Verification : | Analysis |
| Definition:  CAN transceivers shall comply with :   * Supply voltage for IO: VIO(nom) = 3.3V * Supply voltage for CAN buses: VCC(nom) = 5V * Data rate: 500 kbps * Standard compliance: ISO11898-2 * Propagation delay TxD to RxD from dominant to recessive: td ≤ 260ns * TxD dominant time for time out: 0.2ms ≤ tdom ≤ 1ms   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes:  For Standard compliance see GRECT-042 of [RD2]  For Propagation delay TxD to RxD from dominant to recessive: td ≤ 260ns is NC with GRECT-047 of [RD2] which required td ≤ 240ns, ask for derogation  For TxD dominant time for time out see GRECT-0186 of [RD2] | | | | |

Implementation

To assure the segregation of COM and MON channel it is necessary to have two different CAN Transceiver, they will be named CAN\_transceiver\_COM and CAN\_transceiver\_MON.

#### CAN\_transceiver\_COM

The first source of CAN transceiver is **MAX13054** from **Maxim Integrated** (see [RD39] ). It will be named CAN\_transceiver\_COM.

It has the following characteristic:

* **CAN transceiver characteristic**:
  + High level input voltage: VIH(min) = 2.31V
  + Low level input voltage: VIL(max) = 0.99V
  + Data rate: up to 1 Mbps (according with 500 kbps)
  + Common mode capacitance for CAN-H: CCMH = 20 pF
  + Common mode capacitance for CAN-L: CCML = 20 pF
  + Differential capacitances: CDiff = 10 pF
  + Standard compliance: ISO11898
  + Propagation delay TxD to RxD from dominant to recessive: td = 255ns
  + TxD dominant time for time out: 0.3ms ≤ tdom ≤ 1ms
* **Power supply characteristic for IO voltage (VIO)**:
  + Absolute maximum ratings: VIO(max) = 6V
  + Supply voltage: VIO(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 0.015mA
  + Power supply: P = 0.05mW
* **Power supply characteristic for CAN bus voltage (VDD)**:
  + Absolute maximum ratings: VCC(max) = 6V
  + Supply voltage: VCC(nom) = 5V
  + Stress default:
  + Supply current: ICC(max) = 72mA
  + Power supply: P = 238mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 125°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

#### CAN\_transceiver\_MON

The second source of CAN transceiver is **AMIS-30663** from **On Semiconductor** (see [RD40] ). It will be named CAN\_transceiver\_MON.

It has the following characteristic:

* **CAN transceiver characteristic**:
  + High level input voltage: VIH(min) = 2 V
  + Low level input voltage: VIL(max) = 0.8V
  + Data rate: up to 1 Mbps (according with 500 kbps)
  + Common mode capacitance for CAN-H: CCMH = 20 pF
  + Common mode capacitance for CAN-L: CCML = 20 pF
  + Differential capacitances: CDiff = 10 pF
  + Standard compliance: ISO11898-2
  + Propagation delay TxD to RxD from dominant to recessive: td = 245ns
  + TxD dominant time for time out: 0.25ms ≤ tdom ≤ 0.75ms
* **Power supply characteristic for IO voltage (VIO)**:
  + Absolute maximum ratings: VIO(max) = 7V
  + Supply voltage: VIO(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 0.17mA
  + Power supply: P = 0.56mW
* **Power supply characteristic for CAN bus voltage (VDD)**:
  + Absolute maximum ratings: VCC(max) = 7V
  + Supply voltage: VCC(nom) = 5V
  + Stress default:
  + Supply current: ICC(max) = 65mA
  + Power supply: P = 325mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 125°C
  + Storage temperature: -55°C < TSTORAGE < 155°C

### CAN protection

#### CAN interface EMC protection

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0205 | | CAN interface EMC protection | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0091 partial | Verification : | Analysis and Test |
| Definition:  CAN interface shall implement EMC protection.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0210 | | CAN conducted emissions | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0124 partial | Verification : | Analysis and Test |
| Definition:  The equipment shall not produce unwanted conducted emissions on its wiring.  See [RD5] issue F - §6.3.1  Test procedure: adaptation of DO160F/ED14F, section 21 Cat P.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0220 | | CAN radiated electromagnetic fields | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0125 partial | Verification : | Analysis and Test |
| Definition:  The equipment shall not produce radiated electromagnetic fields directly through box or due to spurious RF currents conducted on its wiring.  See [RD5] issue F - §6.3.2  Test procedure: adaptation of DO160F/ED14F, Chap 21 Cat P  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

|  |  |
| --- | --- |
|  | * L1 = 470µH * C1 = 33pF |

Figure 4‑29: CAN EMC protection

The π filter reduces the input and the output disturbances.

#### CAN interface lightning protection

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0201 | | CAN interface lightning protection | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0091 partial  MBD\_X4\_BPTU\_ETS\_0135 partial | Verification : | Analysis and Test |
| Definition:  CAN interface shall implement lightning protection.  See [RD5] - issue F - §7.1 DAL B level, limit L1 (metallic structure)  Test procedure: DO160F/ED14F, section 22  Pin injection tests: Waveform set A with BPTU: level 3  Functional tests (Pin to case injection and cable bundle injection): Waveform set G or J with level 3  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

VCANH and VCANL DC limit value is ± 58V. The diodes VCL shall be less than 58V.

Transorb for CAN protection is **5.0SMDJ24CA** from **Littelfuse** (see [RD41] ). It will be named Transorb\_can.

It has the following characteristic:

* **Transorb characteristic**:
  + Peak pulse power dissipation at TA = 25°C by 10x1000µs waveform (see fig.1 of [RD41] ): PPPM = 5kW
  + Power Dissipation on infinite heat sink at TA = 50°C: PD = 6.5W
  + Peak forward surge current, 8.3ms single half sine wave: IFSM = 300A
  + Maximum instantaneous forward voltage at 100A for unidirectional only: VF = 5.0V
  + Reverse stand off voltage: VR = 24V
  + Breakdown voltage: VBR(min) = 26.7V and VBR(max) = 29.5V
  + Maximum peak pulse current: IPP = 129A
  + Maximum clamping voltage (at IPP): VCL = 38.9V
  + Total capacitance: CT = 300 pF (see figure 4 of [RD41] )
* **Temperature characteristic**:
  + Operating ambient temperature: -65°C < TAMB < 150°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

**Pin to case injection (DO160F waveform set A, level 3)**:

* **Waveform 3/3: 600V/24A at 1.0MHz**
  + IPP capability / PPP vs time graph

5µs at 1.0MHz ±20% (§22.5.1.d and figure 22-4 of [RD8] )

* + Impedance equivalent Z source
  + Peak pulse current threat with VCL effect
* **Waveform 4/1: 300V/60A**
  + IPP capability / PPP vs time graph

t2 = 69µs ±20% (see figure 22-4 of [RD8] )

Worst case: 83µs

* + Impedance equivalent Z source
  + Peak pulse current threat with VCL effect

**Cable bundle injection (DO160F waveform set G or J, level 3)**:

**Single stroke**

* **Waveform 2/1: 300V/600A**
  + IPP capability / PPP vs time graph

t2 = 6.4µs ± 20% (see figure 22-3 of [RD19])

* + Impedance equivalent Z source
  + Peak pulse current threat with VCL effect
* **Waveform 3/3: 600V/120A at 1MHz and 10MHz**
  + IPP capability / PPP vs time graph

5µs at 1.0MHz ±20% (§22.5.1.d and figure 22-4 of [RD8] )

* + Impedance equivalent Z source
  + Peak pulse current threat with VCL effect

10MHz case is negligible because 1MHz case is working.

**Multi stroke**

* **Waveform 2/1: 300V/300A then 150V/150A**
  + Peak impulse current threat with VCL effect
  + Multi stroke ratio

Pulse duration: t2 = 6.4µs ± 20% (see figure 22-3 of [RD19])

Pulse interval: ∆t = 10ms

* + Peak pulse power threat average vs power dissipation
* **Waveform 3/3: 600V/120A then 300V/60A at 1MHz and 10MHz**
  + Peak impulse current threat with VCL effect
  + Multi stroke ratio

Pulse duration: t2 = 5µs for 1MHz ± 20% (see figure 22-3 of [RD19])

Pulse interval: ∆t = 10ms

* + Peak pulse power threat average vs power dissipation

**Multi-burst**

* **Waveform 3/3: 360V/6A at 1MHz and 10MHz**
  + Peak impulse current threat with VCL effect
  + Multi stroke ratio

Pulse duration: t2 = 5µs for 1MHz ± 20% (see figure 22-3 of [RD19])

Pulse interval: ∆t = 50µs

* + Peak pulse power threat average for 1 burst
  + Peak pulse power threat average for multiple burst

#### CAN interface capacitances

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1140 | | CAN interface capacitances | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0074 partial | Verification : | Analysis and Test |
| Definition:  CAN interface capacitances (without CAN controller and CAN transceiver) shall comply with:   * Common mode capacitance for CAN-H: CCMH ≤ 300 pF * Common mode capacitance for CAN-L: CCML ≤ 300 pF * Differential capacitances: CDiff ≤ 170 pF   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes:  For Common mode capacitance for CAN-H see GRECT-038 of [RD2]  For Common mode capacitance for CAN-L see GRECT-038 of [RD2]  For Differential capacitances see GRECT-040 of [RD2] | | | | |

Implementation

It is necessary to add additional diodes like shown on the following figure:



Figure 4‑30: CAN diodes

Diodes for CAN protection is **ES3J** from **Fairchild** (see [RD42] ). It will be named Diode\_can.

It has the following characteristic:

* **Diode characteristic**:
  + Power Dissipation: PD = 1.66W
  + Peak forward surge current, 8.3ms single half sine wave: IFSM = 100A
  + Maximum instantaneous forward voltage at 3A for unidirectional only: VF = 1.7V
  + Reverse stand off voltage: VR = 600V
  + Total capacitance: CT = 45 pF
* **Temperature characteristic**:
  + Operating ambient temperature: -50°C < TAMB < 150°C
  + Storage temperature: -50°C < TSTORAGE < 150°C

The total capacitance for CAN interface is represented on the following figure:



Figure 4‑31: Equivalent schema for CAN interface capacitances

Common mode capacitance for CANL:

CCML = = 131.26 pF

Common mode capacitance for CANH:

CCMH = = 131.26 pF

Differential capacitances:

CDiff = 10 pF

### CAN interface conclusion

The following figure shows the CAN interface for COM channel:



Figure 4‑32: CAN interface for COM channel

Legend:

|  |  |
| --- | --- |
| 1 | CAN controller see 4.5.1 |
| 2 | CAN transceiver see 4.5.2.1 |
| 3 | CAN interface ECM protection see 4.5.3.1 |
| 4 | CAN interface lightning protection see 4.5.3.2 |

The following figure shows the CAN interface for MON channel:



Figure 4‑33: CAN interface for MON channel

Legend:

|  |  |
| --- | --- |
| 1 | CAN controller see 4.5.1 |
| 2 | CAN transceiver see 4.5.2.2 |
| 3 | CAN interface ECM protection see 4.5.3.1 |
| 4 | CAN interface lightning protection see 4.5.3.2 |

## Safety requirements

BPTU have some safety requirements which shall be declined to board.

### BIT concept

The following requirements concern the BIT concept for FPGA.

The BRD (actual document) will just list those requirements without explanation. To have more information, please, refer to [IAD6] .

#### PBIT

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0750-S | | PBIT Execution Time | Version: | 1 |
|  | Covers: | BIT-BPTU-0010 | Verification : | Test |
| Definition:  The PBIT shall be performed after BPTU power up in less than 100ms.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0760-S | | Pin-Programming | Version: | 1 |
|  | Covers: | BIT-BPTU-0020 | Verification : | Test |
| Definition:  During PBIT, in case of pin-programming detected in the following states:  • (Pin-Prog Bit 2, Pin-Prog Bit 1) = (0, 0) OR  • (Pin-Prog Bit 2, Pin-Prog Bit 1) = (1, 1),  The FPGA module shall not emit on the CAN bus.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0770-S | | PBIT CAN Controller Failure | Version: | 1 |
|  | Covers: | BIT-BPTU-0050  BIT-BPTU-0060 | Verification : | Analysis |
| Definition:  During PBIT, the FPGA shall not emit on CAN bus if a failure is detected on the CAN Controller self-test.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0780-S | | PBIT data failure | Version: | 1 |
|  | Covers: | BIT-BPTU-0065 | Verification : | Analysis |
| Definition:  During PBIT, if data failure through CRC check is detected during the EEPROM read, the BPTU shall not emit on the CAN bus.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| BRD-BPTU-1300-S | | | Out Of Range Value | Version: | 1 |
|  | Covers: | BIT-BPTU-0067-D | | Verification : | Analysis |
| Definition:  An OOR frame shall be an Order frame (ID: 0x09184108, 0x09184109, 0x09184104 or 0x09184105) with brake order set to 0x80.  Rationale:  This requirement is justified at upper level. | | | | | |
| End\_Req | | | | | |
| Notes : The brake order field of the Order frame is “BPTU\_xxx\_YH\_BrakeOrderj” with:   * xxx = Pil or Copil * Y = L or R * j = 1 or 2 | | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0790-S | | Power on | Version: | 1 |
|  | Covers: | BIT-BPTU-0085-D | Verification : | Analysis |
| Definition:  During PBIT, the FPGA shall not emit on the CAN bus until reaching the power on threshold value defined in the EEPROM is not reached.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

#### CBIT

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0800-S | | CBIT 3.3V monitoring | Version: | 1 |
|  | Covers: | BIT-BPTU-0090  BIT-BPTU-0100 | Verification : | Analysis |
| Definition:  The 3.3 Vdc power supply shall be monitored during CBIT and the BPTU shall not emit if the measured value is under a defined threshold value stored in the EEPROM (low threshold) or above another defined threshold value stored in the EEPROM (high threshold). In such a case, the measure is declared as invalid.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0810-S | | CBIT ADC tests | Version: | 1 |
|  | Covers: | BIT-BPTU-0030  BIT-BPTU-0110  BIT-BPTU-0115 | Verification : | Analysis |
| Definition:  During CBIT, ADCs shall be tested through one or several mechanisms:   * timeout mechanisms (ADC1, ADC2 and ADC3) * configuration registers check (ADC2)   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0820-S | | CBIT ADC3 Failure | Version: | 1 |
|  | Covers: | BIT-BPTU-0040 | Verification : | Analysis |
| Definition:  During CBIT, each FPGA shall not emit on them CAN bus if an invalid measure or timeout is detected on ADC3 used for power supply monitoring.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0830-S | | CBIT measures monitoring | Version: | 1 |
|  | Covers: | BIT-BPTU-0120 | Verification : | Analysis |
| Definition:  The FPGA shall send an OOR if:   * Two successive measures are ignored due to time out mechanism, or * Three or more measures (regardless ranking) are ignored due to time out mechanism, or * Two successive measures are ignored due to OOR threshold mechanisms, or * Three or more measures (regardless ranking) are ignored due to OOR threshold mechanisms.   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0840-S | | CBIT FPGA reconfiguration | Version: | 1 |
|  | Covers: | BIT-BPTU-0130 | Verification : | Analysis |
| Definition:  The FPGA shall be reconfigured cyclically each 50ms.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0850-S | | CBIT data protection | Version: | 1 |
|  | Covers: | BIT-BPTU-0140 | Verification : | Analysis |
| Definition:  The following data shall be protected through protection data mechanisms (CRC32):   * Frame IDs * HW part number * HW serial number * PLD identification number * Calibration Data   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0860-S | | CBIT data failure | Version: | 1 |
|  | Covers: | BIT-BPTU-0150 | Verification : | Analysis |
| Definition:  During CBIT, if data failure through CRC check is detected during the EEPROM read, the BPTU shall not emit on the CAN bus.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

#### Power on/off strategy

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0870-S | | CBIT 28V monitoring | Version: | 1 |
|  | Covers: | BIT-BPTU-0070 | Verification : | Test |
| Definition:  During CBIT, the main power supply (28 VDC) shall be monitored to check the “power off” conditions.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0880-S | | Power off 1 | Version: | 1 |
|  | Covers: | BIT-BPTU-0080-D | Verification : | Test |
| Definition:  During CBIT, the FPGA shall stop when the 28 Vdc power supply reaches a low power off threshold value defined in the EEPROM.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0890-S | | Power off 2 | Version: | 1 |
|  | Covers: | BIT-BPTU-0083-D | Verification : | Test |
| Definition:  During CBIT, the FPGA shall stop when the 28 Vdc power supply reaches a high power off threshold value defined in the EEPROM.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

### Monitoring

Safety requirements of [IAD6] imposes that 3.3V (BRD-BPTU-0800 see 4.6.1.2) and 28V (BRD-BPTU-0870 see 4.6.1.3) are monitored.

#### ADC\_3

To control 3.3V and 28V, a single ADC with two channels is implemented:

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0920-D | | ADC\_3 characteristics | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  ADC characteristics shall be:   * Accuracy: 12 bits * Number of channel: 2 * DNL: < 1 LSB * Conversion time: < 2µs * Interface: Serial * Supply voltage: VCC(nom) = 3.3V   Rationale:  This requirement is justified by the inter-operability between components. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

The monitoring ADC is **AD7922** from **Analog Devices** (see [RD43] ). It will be named ADC\_3.

It has the following characteristic:

* **ADC characteristic**:
  + Accuracy: 12 bits
  + Number of channel: 2
  + DNL: ±0.9 LSB
  + Conversion time: 777ns
  + Interface: Serial
  + Low level output voltage: VOL(max) = 0.2V
  + High level output voltage: VOH(min) = 3.1V
  + Low level input voltage: VIL(max) = 0.66V
  + High level input voltage: VIH(min) = 2.31V
* **Power supply characteristic**:
  + Absolute maximum ratings: VCC(max) = 7V
  + Supply voltage: VCC(nom) = 3.3V
  + Stress default:
  + Supply current: ICC(max) = 4mA
  + Power supply: P = 13.2mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 85°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0930-D | | ADC\_3 inputs | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  Vin0 of ADC\_3 shall control 28V image.  Vin1 of ADC\_3 shall control 3.3V.  Rationale:  This requirement is for each FPGA have the information. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

#### 3.3V control

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0940-D | | 3.3V control | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  The 3.3V shall be divided by a factor of two before entering on ADC\_3.  Rationale:  This requirement is justified by the inter-operability between components. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

The following voltage divider, with two 100kΩ resistors, is used to divide by a factor of two the 3.3V for each channel:



Figure 4‑34: 3.3V voltage divider

## Power supply

Power supply will refer to [RD6] , [IAD2] and [RD4] .

The following figure represents the J1 connector with the power supply connection:

|  |  |  |
| --- | --- | --- |
| **J1** | | |
|  | | |
| R | 28V | EN2282 H/C network characteristics |
| 05 A max. under 28 Vdc |
| Constant power I = f(U) |
| T | 0V | 0.5 A max. |

Figure 4‑35: Power supply connection

* EN2282:

[RD6] norm describes the characteristics of aircraft power supply.

The figure below shows envelopes voltage transients on 28V DC systems.

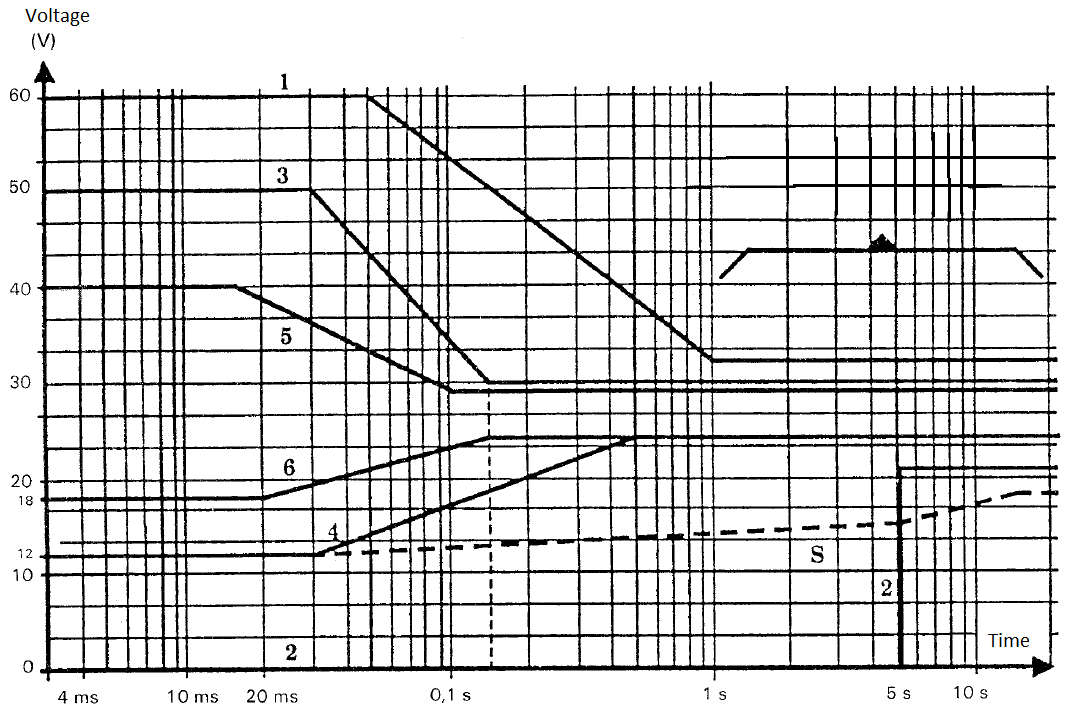


Figure 4‑36: Envelopes voltage transients on 28 VDC systems

### Power supply parameters

#### Board consumption

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0240-D | | Power supply consumption | Version: | 1 |
|  | Covers: | Derived | Verification : | Test |
| Definition:  Power consumption shall be less than IIN = 100mA at 28 VDC ± 100mV.  Rationale:  The consumption of the board is defined to choose the board components. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

On the following table, the efficiency is set at the worst-case:



Table 4‑6: BPTU board consumption

#### Power supply start

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0300 | | Power supply start | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0023 | Verification : | Test |
| Definition:  Power up shall be performed in less than 50ms.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: No transparency is implemented. | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0305 | | Power supply interruptions | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0145  MBD\_X4\_BPTU\_ETS\_0146 | Verification : | Test |
| Definition:  When subjected to DC 28V normal or abnormal power interruptions, the BPTU shall have the following behavior (no failure information, no wrong data, and no degradation).  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: Referred to [RD6] paragraph 6.3, table 3. | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0310 | | Power supply switch on | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0100 | Verification : | Test |
| Definition:  The power switch-on off the equipment will be an automatic power switch on:  The equipment is directly supplied by distribution busbar without control switch located on the cockpit.  When the busbar is supplied by the generation system (depending on the configuration) the equipment is supplied.  The current peak value during the equipment switch-on operation shall have the following characteristics: Maximum current peak value shall be less than 4 In (refer to MBD\_X4\_BPTU\_ETS\_0151) at all operating temperature range. In is the equipment rated current at the rated voltage (28VDC).  The power switch-on current I = f(t) shall be mandatory provided by the supplier according to equipment power consumption.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

#### Input parameters

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1200 | | Power supply in normal operation | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0137  MBD\_X4\_BPTU\_ETS\_0138  MBD\_X4\_BPTU\_ETS\_0139 | Verification : | Test |
| Definition:  When subjected to DC 28V normal operation, the BPTU shall have a nominal behavior (no warm start, no cold start, no failure information, no wrong data, no degradation) during transient and steady state of this input power supply (ripple voltage is limited to +/- 2V peak to peak).  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: Referred to [RD6] paragraph 6.3. | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1210 | | Power supply in abnormal operation | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0140  MBD\_X4\_BPTU\_ETS\_0141 | Verification : | Test |
| Definition:  When subjected to DC 28V abnormal operation, the BPTU shall have a nominal behavior (no warm start, no cold start, no failure information, no wrong data, no degradation) during steady state of this input power supply (overvoltage and under voltage shall be take into account).  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: Referred to [RD6] paragraph 6.3. | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1220 | | Power supply in emergency operation | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0142  MBD\_X4\_BPTU\_ETS\_0143  MBD\_X4\_BPTU\_ETS\_0144 | Verification : | Test |
| Definition:  When subjected to DC 28V emergency operation, the BPTU shall have a nominal behavior (no warm start, no cold start, no failure information, no wrong data, no degradation) during transient and steady state of this input power supply.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: Referred to [RD6] paragraph 6.3. | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0320-D | | Power supply performance | Version: | 1 |
|  | Covers: | Derived | Verification : | Test |
| Definition:  Power supply module shall be compatible to an input voltage between 12V to 60V permanent with tolerance ±1% with a DC 28V nominal.  Rationale:  Referred to [RD6] . | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

VIN represents the supply voltage

|  |  |  |
| --- | --- | --- |
| Name | Description | Value |
| VIN(min) | Minimal input voltage at which BPTU shall operate normally | 12V |
| VIN(max) | Maximum input voltage at which BPTU shall operate normally | 60V |
| VIN(nom) | Nominal input voltage. | 28V |
| POUT | Output power. | ~1W |

Table 4‑7: Power supply parameters

### Power supply architecture

The architecture chosen is **flyback** because POUT ~ 1W.

#### Flyback

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0130 | | Power supply return | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0164 | Verification : | Analysis |
| Definition:  BPTU shall be designed with power supply return insulated from case ground and available on a pin of the connector nearby the power supply line.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0135 | | Power supply ground | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0087 partial  MBD\_X4\_BPTU\_ETS\_0148 partial | Verification : | Analysis |
| Definition:  Primary winding and secondary winding shall be isolated.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0138-D | | GND\_SYS | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  All functions on secondary winding shall referred to GND\_SYS ground.  Rationale:  This requirement is justified by the inter-operability between components. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

Between 28V input (J1 connector) and GND\_SYS (case ground), and between 0V input (J1 connector) and GND\_SYS, a capacitor with the following characteristic is implemented:

* Capacitance: 470pF
* Absolute maximum ratings: V(max) = 2 kV
* Architecture:

Hereafter an equivalent schema for flyback architecture:

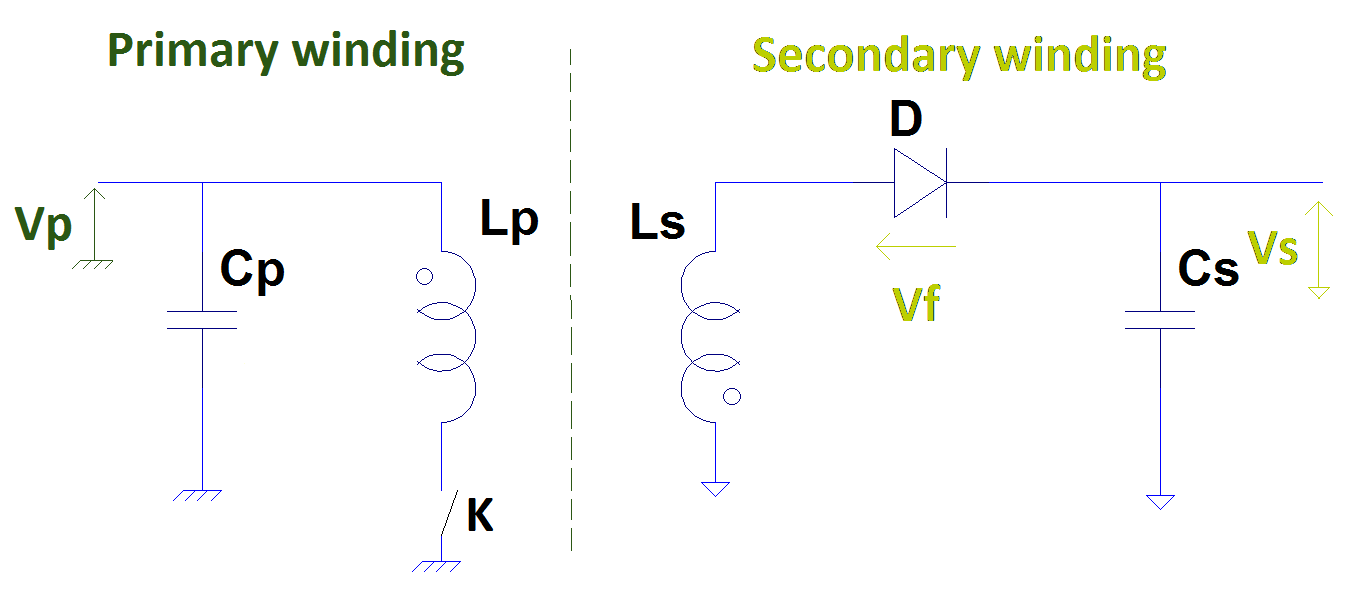


Figure 4‑37: Flyback equivalent schema

* Flyback working:

Flyback have two different phases of working:

First phase: K switch is closed. Voltage across D diode is negative so D is blocked. Power is stocked into Lp inductance. It is necessary to calculate Cs to the secondary winding has enough power. Phase duration is named TON. Hereafter an equivalent schema for flyback architecture during the first phase:

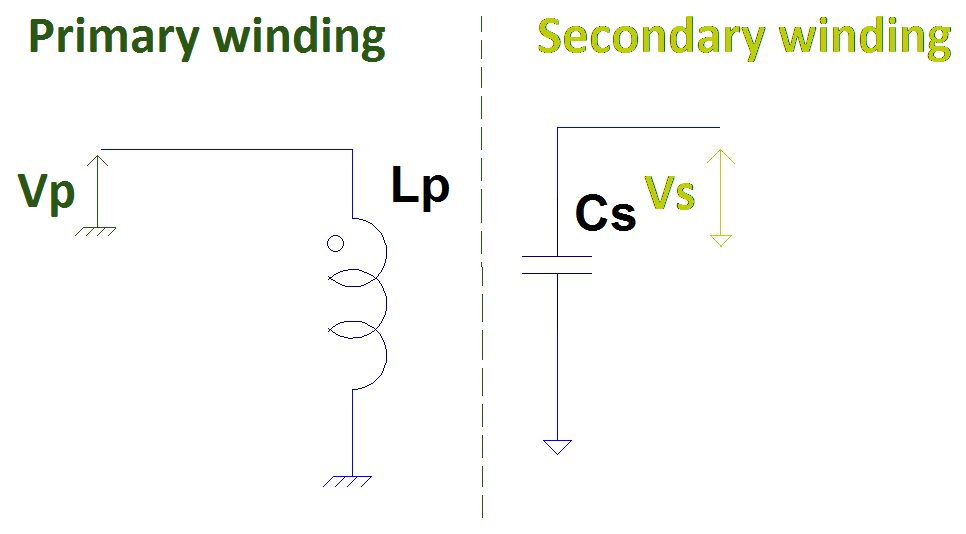


Figure 4‑38: First phase flyback equivalent schema

Second phase: K switch is opened. Lp power is transferred to Ls. During this phase, Cs power is rising up. Phase duration is named TOFF. TOFF corresponds to the duration of D conduction. Hereafter an equivalent schema for flyback architecture during the second phase:

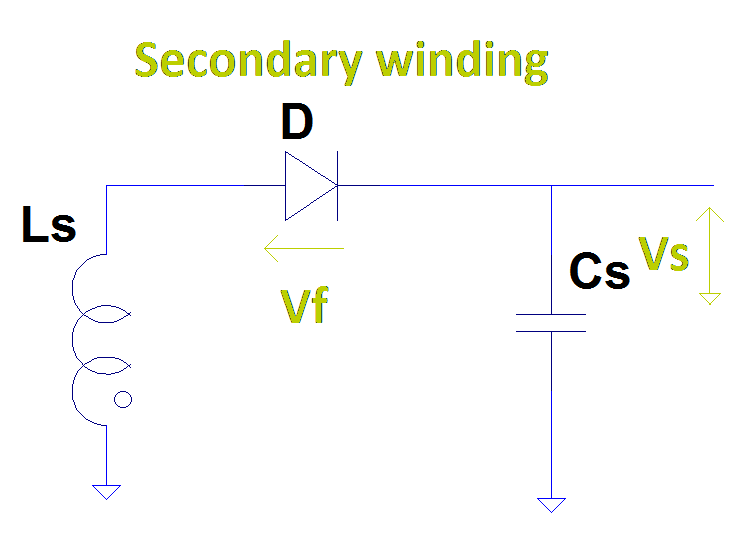


Figure 4‑39: Second phase flyback equivalent schema

* Operating mode:

There is three operating mode: continuous, critical and batch.

TSW represents the time between two switch (cycles).

IP represent the current supplied on LP.

IS represent the current supplied on LS.

Continuous mode:

|  |  |
| --- | --- |
|  | TSW is fixed.  No down time: TOFF is cut.  IP(min) = IS(min) ≠ 0. |

Figure 4‑40: Flyback continuous mode graph

Critical mode:

|  |  |
| --- | --- |
|  | TSW = TON + TOFF is not fixed.  No down time.  IP(min) = IS(min) = 0. |

Figure 4‑41: Flyback critical mode graph

Batch mode:

|  |  |
| --- | --- |
|  | TSW is fixed.  Down time: TON + TOFF < TSW.  IP(min) = IS(min) = 0. |

Figure 4‑42: Flyback batch mode graph

Choice:

The functional mode chosen is **batch mode** because TSW is fixed, duty cycle (see next paragraph) could be higher than 0.5, the size of the transformer is optimized, IP(max) is common.

#### Duty cycle

Duty cycle D represents the duty between the TON and TSW: D = .

The input range is wide: 12V to 60V. That represents a dynamic of = 5. D must be higher than 0.5.

VR = with VR is the brought back voltage to primary winding.

D(max) shall be choice for VR = VIN(nom):

**D(max) = 0.7.**

#### MOSFET transistor

K switch is represented by a transistor. It is necessary to define it VDSS voltage (Drain-to-Source Breakdown Voltage).

∆VLF represents the overvoltage due to the transformer leak coil. ∆VLF shall be lower than 32V.

VDSS > (VIN(max) + VR + ∆VLF) where 1.6 is the factor to respect the 60% load factor voltage.

VDSS > (60+ 28 + 32)

**VDSS > 192 V.**

### Power supply component for COM channel

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0330-D | | Power supply COM | Version: | 1 |
|  | Covers: | Derived | Verification : | Test |
| Definition:  Power supply for COM channel shall delivered 5V, 3.3V and 1.5V with tolerance ±5%.  Rationale:  This requirement is justified by the supply voltage of the component used on COM channel. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

|  |  |  |  |
| --- | --- | --- | --- |
| **Specifications** | | | |
| **Description** | **Name** | **Value** | **Unit** |
| **Input** | | | |
| Minimal input voltage at which BPTU shall operate normally | VIN(min) | 12.00 | V |
| Maximum input voltage at which BPTU shall operate normally | VIN(max) | 60.00 | V |
| Nominal input voltage. | VIN(nom) | 28.00 | V |
| **Efficiency** | | | |
| Optimal efficiency | η | 80.00 | % |
| **Output** | | | |
| Output 1 characteristic | VOUT1 | 5.00 | V |
| IOUT1 | 95.00 | mA |
| POUT1 | 475.00 | mW |
| Output 2 characteristic | VOUT2 | 3.30 | V |
| IOUT2 | 71.39 | mA |
| POUT2 | 235.60 | mW |
| Output 3 characteristic | VOUT2 | 1.50 | V |
| IOUT2 | 256.27 | mA |
| POUT2 | 384.40 | mW |
| **Power** | | | |
| Power of COM channel | POUT | 1.10 | W |
| Power needed for COM channel (1) | PIN | 1.38 | W |
| **Frequency** | | | |
| Chopping frequency | FSW | 110.00 | kHz |

Table 4‑8: Specifications for power supply COM

|  |  |  |  |
| --- | --- | --- | --- |
| **Primary winding components** | | | |
| **Description** | **Name** | **Value** | **Unit** |
| **MOSFET Transistor: IRF7450 International rectifier** | | | |
| Drain-to-Source Breakdown Voltage | VDSS | 200 | V |
| Static Drain-to-Source On-Resistance @VGS = 10V | RDS(on) | 0.17 | Ω |
| **PWM controller: HV9113 Supertex inc** | | | |
| Maximum duty cycle | D(max) | 99 | % |
| **Interfaces** | | | |
| **Description** | **Name** | **Value** | **Unit** |
| **Transformer** | | | |
| Transformation ratio for output 1 (5V) | m1 | 0.19 | NA |
| Transformation ratio for output 2 (3.3V) | m2 | 0.13 | NA |
| Transformation ratio for output 3 (1.5V) | m3 | 0.06 | NA |
| Number of primary coil | NP | 48 | coils |
| Number of secondary coil for output 1 (5V) | NS1 | 9 | coils |
| Number of secondary coil for output 2 (3.3V) | NS2 | 6 | coils |
| Number of secondary coil for output 3 (1.5V) | NS3 | 3 | coils |
| Primary winding self of transformer | LP | 307 | µH |
| **Optocoupler: VO615A-2X019T Vishay** | | | |
| Reverse voltage | VR | 6 | V |
| Forward current | IF | 60 | mA |
| Forward surge current | IFSM | 1.5 | A |
| LED power dissipation | PdissI | 70 | mW |
| Collector emitter voltage | VCEO | 70 | V |
| Emitter collector voltage | VECO | 7 | V |
| Collector current | IC | 50 | mA |
| Collector peak current | ICM | 100 | mA |
| Output power dissipation | PdissO | 70 | mW |
| **Secondary winding components** | | | |
| **Description** | **Name** | **Value** | **Unit** |
| **Diode for VOUT1: PMEG4015EPK NXP** | | | |
| Reverse voltage | VRR1 | 40 | V |
| **Diode for VOUT2: PMEG4015EPK NXP** | | | |
| Reverse voltage | VRR2 | 40 | V |
| **Diode for VOUT3: PMEG2010AEB NXP** | | | |
| Reverse voltage | VRR3 | 20 | V |

Table 4‑9: Components parameters for power supply COM

#### Transistor COM

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0340-D | | Power supply transistor COM | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  Power supply transistor for COM channel shall have the following characteristics:   * VDSS > 192V. * A SOIC package or a Super SO8 package to have multi sources.   Rationale:  This requirement is justify by having multi-sources | | | | |
| End\_Req | | | | |
| Notes: see “MOSFET transistor” | | | | |

Implementation

The transistor for COM channel is **IRF7450** from **International rectifier** (see [RD12] ).

It has the following characteristic:

* **Transistor characteristic**:
  + Drain-to-Source Breakdown Voltage : VDSS = 200V
  + Static Drain-to-Source On-Resistance : RDS(on) = 0.17Ω at VGS = 10V
* **Power supply characteristic**:
  + Absolute maximum ratings: VGS(max) = 30V
  + Supply current: IGS(max) = 0.75mA
* **Temperature characteristic**:
  + Operating ambient temperature: -55°C < TAMB < 150°C
  + Storage temperature: -55°C < TSTORAGE < 150°C

Conduction losses:

#### PWM controller COM

The PWM controller for COM channel is **HV9113** from **Supertex** (see [RD14] ).

It has the following characteristic:

* **Input voltage VIN characteristic**:
  + Absolute maximum ratings: VIN(max) = 120V
  + Supply voltage: VIN(nom) = 60 V
  + Stress default:
  + Supply current: ICC(max) = 0.01mA
  + Power supply: P = 0.6mW
* **Logic voltage VDD characteristic**:
  + Absolute maximum ratings: VDD(max) = 15.5V
  + Supply voltage: VDD(nom) = 7 V
  + Stress default:
  + Supply current: ICC(max) = 0.01mA
  + Power supply: P = 0.6mW
* **Temperature characteristic**:
  + Operating ambient temperature: -55°C < TAMB < 150°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

This component has an internal current generator which provide a power supply rise time of 10ms maximum.

#### Transformer

The transformer has three outputs. The **transformation ratio** for each output is:

with “i” represents “1, 2 or 3”

= 0.19

= 0.13

= 0.06

It is necessary that every coils number is integer:

NP = 48 coils

NS1 = 9 coils

NS2 = 6 coils

NS3 = 3 coils

🡪 🡪 LP = 307µH

🡪 🡪 IP(max) = 243mA

🡪 🡪

🡪

(see [RD11] chapter 3)

#### Optocoupler COM

The optocoupler for COM channel is **VO615A-2X019T** from **Vishay** (see [RD22] ).

It has the following characteristic:

* **Optocoupler characteristic**:
  + Reverse voltage: VR = 6V
  + Forward current: IF = 60mA
  + Forward surge current: IFSM = 1.5A
  + LED power dissipation: PdissI = 70mW
  + Collector emitter voltage: VCEO = 70V
  + Emitter collector voltage: VECO = 7V
  + Collector current: IC = 50mA
  + Collector peak current: ICM = 100mA
  + Output power dissipation: PdissO = 70mW
* **Temperature characteristic**:
  + Operating ambient temperature: -55°C < TAMB < 110°C
  + Storage temperature: -55°C < TSTORAGE < 125°C

#### Diodes

Reverse voltage needed: VDi(max) = VOUTi + mi VIN(max) with i is 1, 2 or 3.

For 5V: VD1(max) = 5 + 0.19 60 = 16.4V 🡪 To respect the 60% load factor voltage, PMEG4015EPK from NXP is chosen: **VRR1 = 40V** (see [RD17] ).

For 3.3V: VD2(max) = 3.3 + 0.13 60 = 11.1V 🡪 To respect the 60% load factor voltage, PMEG4015EPK from NXP is chosen: **VRR2 = 40V** (see [RD17] ).

For 1.5V: VD3(max) = 1.5 + 0.06 60 = 5.1V 🡪 To respect the 60% load factor voltage, PMEG2015EA from NXP is chosen: **VRR3 = 20V** (see [RD18] ).

#### Vin\_Control\_COM

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0950-D | | VIN\_Control\_COM | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  The 28V monitoring shall be reduced between 0V and 3.3V.  Rationale:  This requirement is justified by the inter-operability between components. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

To have a representation of 28 VDC monitored between 0V and 3.3V, it is necessary to implemented on the secondary winding the following schematic:



Figure 4‑43: Vin\_Control\_COM

### Power supply component for MON channel

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0350-D | | Power supply MON | Version: | 1 |
|  | Covers: | Derived | Verification : | Test |
| Definition:  Power supply for MON channel shall delivered 5V, 3.3V and 1.2V with tolerance ±5%.  Rationale:  This requirement is justified by the supply voltage of the component used on MON channel. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

|  |  |  |  |
| --- | --- | --- | --- |
| **Specifications** | | | |
| **Description** | **Name** | **Value** | **Unit** |
| **Input** | | | |
| Minimal input voltage at which BPTU shall operate normally | VIN(min) | 12.00 | V |
| Maximum input voltage at which BPTU shall operate normally | VIN(max) | 60.00 | V |
| Nominal input voltage. | VIN(nom) | 28.00 | V |
| **Efficiency** | | | |
| Optimal efficiency | η | 80.00 | % |
| **Output** | | | |
| Output 1 characteristic | VOUT1 | 5.00 | V |
| IOUT1 | 98 | mA |
| POUT1 | 490 | mW |
| Output 2 characteristic | VOUT2 | 3.30 | V |
| IOUT2 | 81.03 | mA |
| POUT2 | 267.4 | mW |
| Output 3 characteristic | VOUT2 | 1.20 | V |
| IOUT2 | 100 | mA |
| POUT2 | 120 | mW |
| **Power** | | | |
| Power of MON channel | POUT | 877.40 | W |
| Power needed for MON channel (1) | PIN | 1096.75 | W |
| **Frequency** | | | |
| Chopping frequency | FSW | 90 | kHz |

Table 4‑10: Specifications for power supply MON

|  |  |  |  |
| --- | --- | --- | --- |
| **Primary winding components** | | | |
| **Description** | **Name** | **Value** | **Unit** |
| **MOSFET Transistor: SI4462DY Vishay** | | | |
| Drain-to-Source Breakdown Voltage | VDSS | 200 | V |
| Static Drain-to-Source On-Resistance @VGS = 10V | RDS(on) | 0.48 | Ω |
| **PWM controller: ISL8843A Intersil** | | | |
| Maximum duty cycle | D(max) | 96 | % |
| **Interfaces** | | | |
| **Description** | **Name** | **Value** | **Unit** |
| **Transformer** | | | |
| Transformation ratio for output 1 (5V) | m1 | 0.19 | NA |
| Transformation ratio for output 2 (3.3V) | m2 | 0.13 | NA |
| Number of primary coil | NP | 48 | coils |
| Number of secondary coil for output 1 (5V) | NS1 | 9 | coils |
| Number of secondary coil for output 2 (3.3V) | NS2 | 6 | coils |
| Primary winding self of transformer | LP | 392 | µH |
| **Optocoupler: FODM121B Fairchild** | | | |
| Reverse voltage | VR | 6 | V |
| Forward current | IF | 50 | mA |
| Forward surge current | IFSM | 1 | A |
| LED power dissipation | PdissI | 70 | mW |
| Collector emitter voltage | VCEO | 80 | V |
| Emitter collector voltage | VECO | 7 | V |
| Collector current | IC | 80 | mA |
| Output power dissipation | PdissO | 150 | mW |
| **Secondary winding components** | | | |
| **Description** | **Name** | **Value** | **Unit** |
| **Diode for VOUT1: PMEG4015EPK NXP** | | | |
| Reverse voltage | VRR1 | 40 | V |
| **Diode for VOUT2: PMEG2015EA NXP** | | | |
| Reverse voltage | VRR2 | 20 | V |
| **Voltage reference for VOUT3: ST1S12GR ST** | | | |
| Fixed output voltage | VVRout | 1.2 | V |
| Minimum input voltage | VVRin(min) | 2.5 | V |

Table 4‑11: Components parameters for power supply MON

#### Transistor MON

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0360-D | | Power supply transistor MON | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  Power supply transistor for MON channel shall have the following characteristics:   * VDSS > 192V. * A SOIC package or a Super SO8 package to have multi sources.   Rationale:  This requirement is justify by having multi-sources | | | | |
| End\_Req | | | | |
| Notes: see “MOSFET transistor” | | | | |

The transistor for MON channel is **SI4462DY** from **Vishay** (see [RD13] ).

It has the following characteristic:

* **Transistor characteristic**:
  + Drain-to-Source Breakdown Voltage : VDSS = 200V
  + Static Drain-to-Source On-Resistance : RDS(on) = 0.48Ω at VGS = 10V
* **Power supply characteristic**:
  + Absolute maximum ratings: VGS(max) = 20V
  + Supply voltage: VGS(nom) = V
* **Temperature characteristic**:
  + Operating ambient temperature: -55°C < TAMB < 150°C
  + Storage temperature: -55°C < TSTORAGE < 150°C

Conduction losses:

#### PWM controller MON

The PWM controller for MON channel is ISL8843A from Intersil (see [RD15] ).

It has the following characteristic:

* **Supply voltage VDD characteristic**:
  + Absolute maximum ratings: VDD(max) = 30V
* **Temperature characteristic**:
  + Operating ambient temperature: -55°C < TAMB < 150°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

The VDD is supply at the beginning by the board input through two parallel 10kΩ resistors and a 22µF capacitor:



Figure 4‑44: RC for MON power supply

This implementation increase the rise time:

VIN(nom) = 28V

VDDstart(max) = 9.0V

The rise time for power supply is:

#### Transformer

The transformer has two outputs. The **transformation ratio** for each output is:

with “i” represents “1 or 2”

= 0.19

= 0.13

It is necessary that every coils number is integer:

NP = 48 coils

NS1 = 9 coils

NS2 = 6 coils

🡪 🡪 LP = 392µH

🡪 🡪 IP(max) = 238mA

🡪 🡪

🡪

(see [RD11] chapter 4)

#### Optocoupler MON

The optocoupler for MON channel is **FODM121B** from **Fairchild** (see [RD23] ).

It has the following characteristic:

* **Optocoupler characteristic**:
  + Reverse voltage: VR = 6V
  + Forward current: IF = 50mA
  + Forward surge current: IFSM = 1A
  + LED power dissipation: PdissI = 70mW
  + Collector emitter voltage: VCEO = 80V
  + Emitter collector voltage: VECO = 7V
  + Collector current: IC = 80mA
  + Output power dissipation: PdissO = 150mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 110°C
  + Storage temperature: -40°C < TSTORAGE < 125°C

#### Diodes

Reverse voltage needed: VDi(max) = VOUTi + mi VIN(max) with i is 1, 2 or 3.

For 5V: VD1(max) = 5 + 0.19 60 = 16.4V 🡪 To respect the 60% load factor voltage, PMEG4015EPK from NXP is chosen: **VRR1 = 40V** (see [RD17] ).

For 3.3V: VD2(max) = 3.3 + 0.13 60 = 11.1V 🡪 To respect the 60% load factor voltage, PMEG2015EPK from NXP is chosen: **VRR2 = 20V** (see [RD18] ).

#### VOUT3: 1.2V

VOUT3 couldn’t be generating by the transformer to ensure a tolerance of 5%. A voltage reference is added.

The voltage reference for VOUT3 1.2V is **ST1S12GR** from **ST** (see [RD21] ).

It has the following characteristic:

* **Voltage reference characteristic**:
  + VFB = 0.6V
* **Power supply characteristic (VVR**in**)**:
  + Absolute maximum ratings: VVRin(max) = 6.5V
  + Supply voltage: VVRin (nom) = 3.3V
  + Stress default:
  + Supply current: IVRin(max) = 0.7mA
  + Power supply: P = 2.31mW
* **Temperature characteristic**:
  + Operating ambient temperature: -40°C < TAMB < 150°C
  + Storage temperature: -65°C < TSTORAGE < 150°C

The voltage reference chosen is adjustable, [RD21] give the following formula and figure:

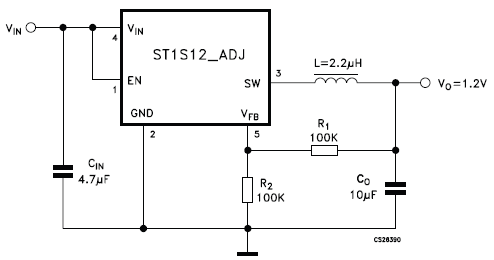


Figure 4‑45: Typical application for 1.2V voltage reference

To have VVRout = 1.2V, two 100kΩ resistors are placed on R1 and R2.

A filter is added on output with L = 10µH and C0 = 22µF.

#### Vin\_Control\_MON

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0960-D | | VIN\_Control\_MON | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  The 28V monitoring shall be reduced between 0V and 3.3V.  Rationale:  This requirement is justified by the inter-operability between components. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

To have a representation of 28 VDC monitored between 0V and 3.3V, it is necessary to implemented on the secondary winding the following schematic:



Figure 4‑46: Vin\_Control\_MON

### Power supply protection

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0170 | | Power supply voltage spikes | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0128 | Verification : | Analysis and Test |
| Definition:  The equipment shall not be disturbed due to voltage spikes appearing its power supply inputs.  See [RD5] issue F - §6.6  Test procedure: adaptation of DO160F/ED14F, section 17 Cat A  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0180 | | Power supply voltages conducted | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0129 | Verification : | Analysis and Test |
| Definition:  The equipment shall not be interfered by voltages conducted on power supply.  See [RD5] issue F - §6.7  Test procedure: adaptation of DO160F/ED14F, section 18 Cat Z (DC Equipment)  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0190 | | Power supply induced voltage | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0130 | Verification : | Analysis and Test |
| Definition:  The equipment shall not be interfered by induced voltages.  See [RD5] issue F - §6.8  Test procedure: adaptation of DO160F/ED14F, section 19, cat ZN  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

#### Power supply lightning protection

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0081 | | Power supply lightning protection | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0091 partial  MBD\_X4\_BPTU\_ETS\_0135 partial | Verification : | Analysis and Test |
| Definition:  Power supply input shall implement lightning protection.  See [RD5] - issue F - §7.1 DAL B level, limit L1 (metallic structure)  Test procedure: DO160F/ED14F, section 22  Pin injection tests: Waveform set A with BPTU: level 3  Functional tests (Pin to case injection and cable bundle injection): Waveform set G or J with level 3  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

The transorb for power supply lightning protection is **5KP58CA** from **Littelfuse** (see [RD9] ). It will be named Transorb\_power.



Figure 4‑47: Power supply lightning protection

It has the following characteristic:

* **Transorb characteristic**:
  + Peak pulse power dissipation by 10x1000µs test Waveform (see fig.1 of [RD9] ): PPPM = 5kW
  + Steady State Power Dissipation on infinite heat sink at TL = 75°C (see fig.5 of [RD9] ): PD = 8.0W
  + Peak forward surge current, 8.3ms single half sine wave unidirectional only: IFSM = 400A
  + Maximum instantaneous forward voltage at 100A for unidirectional only: VF = 3.5/5.0V
  + Reverse stand off voltage: VR = 58V
  + Breakdown voltage: VBR(min) = 64.4V and VBR(max) = 71.2V
  + Maximum peak pulse current: IPP = 54.5A
  + Maximum clamping voltage (at IPP): VCL = 93.6V
* **Temperature characteristic**:
  + Operating ambient temperature: -55°C < TAMB < 175°C
  + Storage temperature: -55°C < TSTORAGE < 175°C

It has to deals with:

* **Power supply characteristics**:

|  |  |  |
| --- | --- | --- |
| Name | Description | Value |
| VIN(min) | Minimal input voltage at which BPTU shall operate normally | 12V |
| VIN(max) | Maximum input voltage at which BPTU shall operate normally | 60V |
| VIN(nom) | Nominal input voltage. | 28V |
| POUT | Output power. | ~1W |

Table 4‑12: power supply characteristics

* **Capacitors maximal input voltage**: 100V (see 4.7.5.2)

**Pin to case injection (DO160F waveform set A, level 3)**:

* **Waveform 3/3: 600V/24A at 1.0MHz**
  + IPP capability / PPP vs time graph

5µs at 1.0MHz ±20% (§22.5.1.d and figure 22-4 of [RD8] )

* + Impedance equivalent Z source
  + Peak pulse current threat with VCL effect
* **Waveform 4/1: 300V/60A**
  + IPP capability / PPP vs time graph

t2 = 69µs ±20% (see figure 22-4 of [RD8] )

Worst case: 83µs

* + Impedance equivalent Z source
  + Peak pulse current threat with VCL effect

**Cable bundle injection (DO160F waveform set G or J, level 3)**:

**Single stroke**

* **Waveform 2/1: 300V/600A**
  + IPP capability / PPP vs time graph

t2 = 6.4µs ± 20% (see figure 22-3 of [RD19])

* + Impedance equivalent Z source
  + Peak pulse current threat with VCL effect
* **Waveform 3/3: 600V/120A at 1MHz and 10MHz**
  + IPP capability / PPP vs time graph

5µs at 1.0MHz ±20% (§22.5.1.d and figure 22-4 of [RD8] )

* + Impedance equivalent Z source
  + Peak pulse current threat with VCL effect

10MHz case is negligible because 1MHz case is working.

**Multi stroke**

* **Waveform 2/1: 300V/300A then 150V/150A**
  + Peak impulse current threat with VCL effect
  + Multi stroke ratio

Pulse duration: t2 = 6.4µs ± 20% (see figure 22-3 of [RD19])

Pulse interval: ∆t = 10ms

* + Peak pulse power threat average vs power dissipation
* **Waveform 3/3: 600V/120A then 300V/60A at 1MHz and 10MHz**
  + Peak impulse current threat with VCL effect
  + Multi stroke ratio

Pulse duration: t2 = 5µs for 1MHz ± 20% (see figure 22-3 of [RD19])

Pulse interval: ∆t = 10ms

* + Peak pulse power threat average vs power dissipation

**Multi-burst**

* **Waveform 3/3: 360V/6A at 1MHz and 10MHz**
  + Peak impulse current threat with VCL effect
  + Multi stroke ratio

Pulse duration: t2 = 5µs for 1MHz ± 20% (see figure 22-3 of [RD19])

Pulse interval: ∆t = 50µs

* + Peak pulse power threat average for 1 burst
  + Peak pulse power threat average for multiple burst

#### Power supply EMC protection

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0145 | | Power supply EMC protection | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0091 partial | Verification : | Analysis and Test |
| Definition:  Power supply input shall implement EMC protection.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0140 | | Power supply conducted emissions | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0124 partial | Verification : | Analysis and Test |
| Definition:  The equipment shall not produce unwanted conducted emissions on its wiring.  See [RD5] issue F - §6.3.1  Test procedure: adaptation of DO160F/ED14F, section 21 Cat P.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0150 | | Power supply radiated electromagnetic fields | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0125 partial | Verification : | Analysis and Test |
| Definition:  The equipment shall not produce radiated electromagnetic fields directly through box or due to spurious RF currents conducted on its wiring.  See [RD5] issue F - §6.3.2  Test procedure: adaptation of DO160F/ED14F, Chap 21 Cat P  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0290 | | Conducted emission | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0147 | Verification : | Analysis and Test |
| Definition:  The equipment conducted emission limits on power lines shall be lower than:   |  |  | | --- | --- | | Frequency bands | Limits | | 20Hz | 100 dB µA | | 1 KHz | 100 dB µA | | 10 KHz | 80 dB µA | | 150 KHz | 53 dB µA |   Additional info:  DO-160F section 21  The BWI (measurement bandwidth) will be as per table below:   |  |  | | --- | --- | | Frequency bands | BWI | | 20 Hz – 1 KHz | 10 Hz | | 1 KHz – 10 KHz | 100 Hz | | 10 KHz – 150 KHz | 1 KHz |   Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

A π filter is provided for EMC protection:

|  |  |
| --- | --- |
|  | * L1 = L2 = 330µH * C1 = C2 = 1µF * C1 and C2 maximal input voltage: 100V |

Figure 4‑48: Power supply EMC protection

The π filter reduces the input and the output disturbances.

#### Power supply damage

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0100 | | Power supply damage | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0087 partial | Verification : | Analysis |
| Definition:  Damage due to an internal power supply shall be limited to the internal power supply, the voltage of internal power supply shall not propagate outside the equipment.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0110 | | Power supply crossed polarity | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0088 | Verification : | Analysis and Test |
| Definition:  Equipment shall be protected against crossed polarity of power supply input.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0120 | | Voltage transients generation | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0092 | Verification : | Analysis |
| Definition:  The equipment shall not generate voltage transients on its inputs or outputs out of functional orders, and susceptible to modify other inputs or outputs.  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-0160 | | Power supply conducted spikes | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0126 | Verification : | Analysis and Test |
| Definition:  The equipment shall not produce unwanted conducted spikes on its power leads during on/off switching and in the course of normal operation.  See [RD5] issue F - §6.4 Limit 28 VDC : +/- 150 Vpeak  Rationale:  This requirement is justified at upper level. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

The protection against polarity reversal is done by the D2 diode. It is a **USL1M** from **Diotec** (see [RD10] ). It will be name Diode\_polarity.

It has the following characteristic:

* **Diode characteristic**:
  + Repetitive peak reverse voltage: VRRM = 1kV
  + Nominal current: IF = 1A
* **Temperature characteristic**:
  + Operating ambient temperature: -50°C < TAMB < 150°C
  + Storage temperature: -50°C < TSTORAGE < 150°C

Permanent constraint: 32V at 125mA.

### Decoupling capacitors

Requirement

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| BRD-BPTU-1000-D | | Decoupling capacitors | Version: | 1 |
|  | Covers: | Derived | Verification : | Analysis |
| Definition:  Each integrated circuit (mentioned U on the schematic) shall have decoupling capacitors according to their datasheet.  Rationale:  This requirement is justify by the use of each components. | | | | |
| End\_Req | | | | |
| Notes: | | | | |

Implementation

The document [IAD5] indicates that all decoupling capacitors must be placed as closed as possible of each component.

#### Hall-effect sensors decoupling capacitors

A decoupling capacitor of 100nF is placed as closed as possible of the Hall-effect\_sensor\_1.

A decoupling capacitor of 100nF is placed as closed as possible of the Hall-effect\_sensor\_2.

The following figure shows the schematic of decoupling capacitor for hall-effect sensors:



Figure 4‑49: Decoupling capacitors for hall-effect sensors

#### Instrumentation\_amplifier\_1 decoupling capacitors

The datasheet of the Instrumentation\_amplifier\_1 [RD28] shows a typical application circuit:

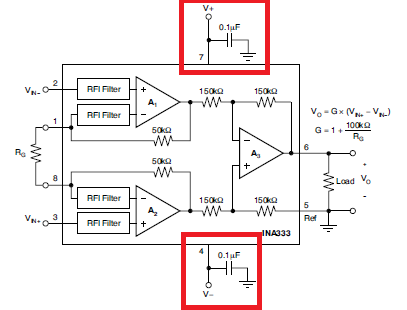


Figure 4‑50: Decoupling capacitors for Instrumentation\_amplifier\_1

Two decoupling capacitors of 100nF are placed as closed as possible of the Instrumentation\_amplifier\_1.

#### Instrumentation\_amplifier\_2 decoupling capacitors

The datasheet of the Instrumentation\_amplifier\_2 [RD27] shows a typical application circuit:

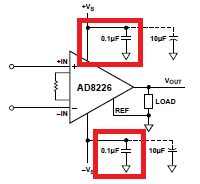


Figure 4‑51: Decoupling capacitors for Instrumentation\_amplifier\_2

Two decoupling capacitors of 100nF are placed as closed as possible of the Instrumentation\_amplifier\_2.

#### ADC\_1 decoupling capacitors

The datasheet of the ADC\_1 [RD29] shows a typical application circuit:

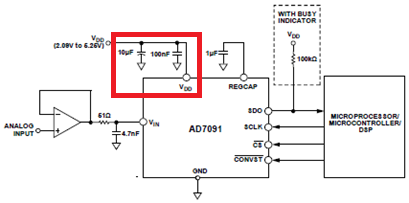


Figure 4‑52: Decoupling capacitors for ADC\_1

Two decoupling capacitors of 10µF and 100nF are placed as closed as possible of the ADC\_1.

#### ADC\_2 decoupling capacitors

The datasheet of the ADC\_2 [RD30] shows a typical application circuit:

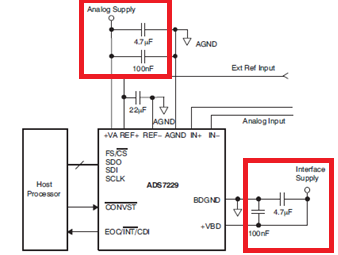


Figure 4‑53: Decoupling capacitors for ADC\_2

Two decoupling capacitors of 4.7µF and 100nF are placed as closed as possible of the net Va of ADC\_2.

Two decoupling capacitors of 4.7µF and 100nF are placed as closed as possible of the net VBD of ADC\_2.

#### FPGA decoupling capacitors

A decoupling capacitor, 10nF or 10µF, is placed on each power supply of FPGA\_COM.

A decoupling capacitor, 10nF or 100nF, is placed on each power supply of FPGA\_MON.

#### Oscillators decoupling capacitors

A decoupling capacitor of 100nF is placed as closed as possible of the Oscillator\_COM.

A decoupling capacitor of 100nF is placed as closed as possible of the Oscillator\_MON.

The following figure shows the schematic of decoupling capacitor for oscillators:



Figure 4‑54: Decoupling capacitors for Oscillators

#### EEPROM decoupling capacitors

Two decoupling capacitor of 100nF are placed as closed as possible of the EEPROM\_COM.

Two decoupling capacitor of 100nF are placed as closed as possible of the EEPROM\_MON.

The following figure shows the schematic of decoupling capacitor for EEPROM:



Figure 4‑55: Decoupling capacitors for EEPROM

#### CAN\_transceiver\_COM decoupling capacitors

Two decoupling capacitor of 100nF are placed as closed as possible of the VDD (net 3) of the CAN\_transceiver\_COM.

Two decoupling capacitor of 100nF are placed as closed as possible of the VIO (net 8) of the CAN\_transceiver\_COM.



Figure 4‑56: Decoupling capacitors for CAN\_transceiver\_COM

#### CAN\_transceiver\_MON decoupling capacitors

Two decoupling capacitor of 100nF are placed as closed as possible of the VDD (net 3) of the CAN\_transceiver\_MON.

Two decoupling capacitor of 100nF are placed as closed as possible of the VIO (net 8) of the CAN\_transceiver\_MON.



Figure 4‑57: Decoupling capacitors for CAN\_transceiver\_MON

#### ADC\_3 decoupling capacitors

A decoupling capacitor of 100nF and a decoupling capacitor of 10µF are placed as closed as possible of the ADC\_3.



Figure 4‑58: Decoupling capacitors for ADC\_3

## Environmental requirements

BPTU have some environmental requirements which shall be declined to board.

### Temperature

#### Board components temperature

Requirements

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| BRD-BPTU-0900 | | | Operating ambient temperature | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0107  MBD\_X4\_BPTU\_ETS\_0109  MBD\_X4\_BPTU\_ETS\_0110 | | Verification : | Analysis and Test |
| Definition:  All board components shall have an operating ambient temperature (TAMB) verifying:  -40°C ≤ TAMB ≤ 85°C  Rationale:  This requirement is justified at upper level. | | | | | |
| End\_Req | | | | | |
| Notes:TAMB ≥ 75°C is temporary state | | | | | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| BRD-BPTU-0910 | | | Storage temperature | Version: | 1 |
|  | Covers: | MBD\_X4\_BPTU\_ETS\_0106  MBD\_X4\_BPTU\_ETS\_0108 | | Verification : | Analysis and Test |
| Definition:  All board components shall have a storage temperature (TSTORAGE) verifying:  -55°C ≤ TSTORAGE ≤ 85°C  Rationale:  This requirement is justified at upper level. | | | | | |
| End\_Req | | | | | |
| Notes: | | | | | |

Implementation

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Component** | **TAMB (°C)** | | **TSTORAGE (°C)** | |
| **Min** | **Max** | **Min** | **Max** |
| **Acquisition channel (see 4.2.3)** | | | | |
| Hall-effect\_sensor\_1 ([RD25] ) | -40 | 150 | -65 | 170 |
| Hall-effect\_sensor\_2 ([RD26] ) | -40 | 100 | -55 | 165 |
| Instrumentation\_amplifier\_1 ([RD28] ) | -40 | 150 | -65 | 150 |
| Instrumentation\_amplifier\_2 ([RD27] ) | -40 | 125 | -65 | 150 |
| ADC\_1 ([RD29] ) | -40 | 125 | -65 | 150 |
| ADC\_2 ([RD30] ) | -40 | 85 | -65 | 150 |
| **Processing (see 4.4)** | | | | |
| FPGA\_COM ([RD31] ) | -40 | 85 | -65 | 150 |
| FPGA\_MON ([RD32] ) | -40 | 100 | -65 | 150 |
| Oscillator\_COM ([RD35] ) | -40 | 85 | -40 | 125 |
| Oscillator\_MON ([RD36] ) | -40 | 85 | -55 | 100 |
| EEPROM\_COM ([RD33] ) | -40 | 125 | -65 | 150 |
| EEPROM\_MON ([RD34] ) | -40 | 125 | -65 | 150 |
| **CAN interface (see 4.5)** | | | | |
| CAN\_transceiver\_COM ([RD39] ) | -40 | 125 | -65 | 150 |
| CAN\_transceiver\_MON ([RD40] ) | -40 | 125 | -55 | 155 |
| Transorb\_can ([RD41] ) | -65 | 150 | -65 | 150 |
| ES3J ([RD42] ) | -50 | 150 | -50 | 150 |
| **Monitoring (see 4.6.2)** | | | | |
| ADC\_3 ([RD43] ) | -40 | 85 | -65 | 150 |
| **Power supply (see 4.7)** | | | | |
| Transistor\_COM ([RD12] ) | -55 | 150 | -55 | 150 |
| Transistor\_MON ([RD13] ) | -55 | 150 | -55 | 150 |
| Controller\_COM ([RD14] ) | -55 | 125 | -65 | 150 |
| Controller\_MON ([RD15] ) | -40 | 105 | -65 | 150 |
| Optocoupler\_COM ([RD22] ) | -55 | 110 | -55 | 125 |
| Optocoupler\_MON ([RD23] ) | -40 | 110 | -40 | 125 |
| Ref\_Des\_COM ([RD19] ) | -40 | 125 | -65 | 150 |
| Ref\_Des\_MON ([RD20] ) | -40 | 105 | -65 | 150 |
| Ref\_1.2\_MON ([RD21] ) | -40 | 150 | -65 | 150 |
| D\_transorb ([RD9] ) | -55 | 175 | -55 | 175 |
| USL1M ([RD10] ) | -50 | 150 | -50 | 150 |
| BAS521 | -65 | 150 | -65 | 150 |
| PMEG2015EA | -65 | 125 | -65 | 150 |
| MBR0520LT3G | -65 | 125 | -65 | 150 |
| PMEG4015EPK | -55 | 150 | -65 | 150 |

Table 4‑13: Components temperatures

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Component technology** | **TAMB (°C)** | | **TSTORAGE (°C)** | |
| **Min** | **Max** | **Min** | **Max** |
| **Capacitors** | | | | |
| X5R technology | -55 | 85 | -55 | 85 |
| X7R technology | -55 | 125 | -55 | 125 |
| X6S technology | -55 | 105 | -55 | 105 |
| X6T technology | -55 | 105 | -55 | 105 |
| NPO technology | -55 | 125 | -55 | 125 |

Table 4‑14: Capacitors temperature

#### BPTU thermal considerations

* Scope

The aim is to assess the thermal risks of the BPTU, in the extreme high temperatures.

For this we use an approximation of the BPTU enclosure and board thermal modeling.

* Thermal modeling approximation

The BPTU enclosure is approximated to a rectangular case which is made of aluminum 6061.

The approximate dimensions are given in the following scheme.



Figure 4‑59: BPTU enclosure approximation

The total inner wall surface is about **0,0572** m2

The BPTU wall is **3**mm width.

The aluminum thermal conductivity is λ=**167** W.m/ m2 °C

* BPTU power consumption and inner wall temperature

For a 28 VDC nominal power input the maximum current is 0,5 A (conservative assumption) so it means a 14W power dissipation.



Figure 4‑60: BPTU estimation of the inside temperature

The thermal resistance of the BPTU wall is :

The temperature variation between the outside and the inside wall is given by:

Δt = Temperature increase

Rth = thermal resistance

Φ = heat flow (Power)

The Δt is negligible so we consider that the inner temperature is the same as the outside temperature, the considered temperature is 85°C it’s the maximum temperature at which the BPTU may be subjected.

* BPTU inner ambient temperature

The dissipation of the 14W is made by conduction along the aluminum screws and by convection through the air inside the BPTU.



The thermal resistance for the convection aspect is given by:

We assume **hair** = 5 W/m²K

**S** is the board surface ~0.00826 m2

The thermal resistance for the screws conduction is given by:



As there are 11 screws the total thermal résistance is 1.13/11 = 0.1 K/W

A few part of the 14W dissipation power is made by convection, 14 \* 0,1/24 = 0.058W

Meaning an increase of the ambient temperature inside the BPTU of 1,4 °C

* BPTU electronic board

The board could be modeled, regarding the thermal aspects, as the following scheme:



Figure 4‑61: Electronic board modeling

Rthjc I = Thermal resistance between junction and case of component I

Rthca I = Thermal resistance between case and ambient (inside the BPTU) of component I

Rthcp I = Thermal resistance between case and Printed circuit board of component I

Rthaw = Thermal resistance between ambient inside BPTU and the inner wall of the BPTU

Some thermal resistances are not easy to determine so in a conservative way we simplify the model as following:



The temperature *Tinside* (ambient inside the BPTU) as calculate before is 1,4 + 85 = 86,4 °C

* Junction temperature

To assess the thermal risk we take into consideration the component with the highest power dissipation. See Table 4‑6: BPTU board consumption.

The components with the highest power dissipation are listed in the following table.

|  |  |  |  |
| --- | --- | --- | --- |
| Supplier | Component Reference | Package | Consumption  (mW) |
| Actel | A3P1000 | FGG144 | 406 |
| Actel | M2GL050 | VFG400 | 140 |

From the *Tinside* temperature we have to verify that the Junction temperature of the components never exceed 125°C (absolute maximum rating), which is the case as demonstrated in the table below.

|  |  |  |  |
| --- | --- | --- | --- |
| Component Reference | Rth JA | p  Consumption  (mW) | **TJ** = Tinside + Rth JA \* P |
| A3P1000 | Junction to ambient  26,9°C/W | 406 | 86,4 + 0.406\*26.9 = **97.3°C** |
| M2GL050 | Junction to ambient  18,36°C/W | 140 | 86,4 + 0.140\*18.36 = **89°C** |

These hypotheses are confirmed in the document [IAD10] .

# Deleted requirements

This paragraph reports all the deleted requirements:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ~~BRD-BPTU-0080~~ | | ~~Power supply lightning and ECM protection~~ | ~~Version:~~ | DELETED |
|  | ~~Covers:~~ |  | ~~Verification :~~ | ~~Analysis~~ |
| ~~Definition:~~  ~~The equipment shall implement lightning and devices to comply with the electromagnetic environment requirements.~~  ~~Rationale:~~  ~~The BPTU input shall perform filtering.~~ | | | | |
| ~~End\_Req~~ | | | | |
| ~~Notes:~~ | | | | |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ~~BRD-BPTU-0090~~ | | ~~Power supply lightning indirect effects~~ | ~~Version:~~ | DELETED |
|  | ~~Covers:~~ |  | ~~Verification :~~ | ~~Analysis and Test~~ |
| ~~Definition:~~  ~~The equipment must show neither any arcing nor any damages when exposed to lightning indirect effects.~~  ~~See [RD5] - issue F - §7.1 DAL B level, limit L1 (metallic structure)~~  ~~Test procedure: DO160F/ED14F, section 22~~  ~~Pin injection tests: Waveform set A with BPTU: level 3~~  ~~Functional tests (BCI and GI): Waveform set G or J with BPTU: level 3~~  ~~Rationale:~~  ~~The BPTU input shall perform filtering.~~ | | | | |
| ~~End\_Req~~ | | | | |
| ~~Notes:~~ | | | | |

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| --- | --- | --- | --- | --- |
| ~~BRD-BPTU-0200~~ | | ~~CAN lightning and EMC protection~~ | ~~Version:~~ | DELETED |
|  | ~~Covers:~~ |  | ~~Verification :~~ | ~~Analysis~~ |
| ~~Definition:~~  ~~The equipment shall implement lightning and EMC protection devices to comply with the electromagnetic environment requirements.~~  ~~Rationale:~~  ~~This requirement is justified at upper level.~~ | | | | |
| ~~End\_Req~~ | | | | |
| ~~Notes:~~ | | | | |

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| --- | --- | --- | --- | --- |
| ~~BRD-BPTU-0230~~ | | ~~CAN lightning indirect effects~~ | ~~Version:~~ | DELETED |
|  | ~~Covers:~~ |  | ~~Verification :~~ | ~~Analysis and Test~~ |
| ~~Definition:~~  ~~The equipment must show neither any arcing nor any damages when exposed to lightning indirect effects.~~  ~~See~~~~[RD5] issue F - §7.1 DAL B level, limit L1 (metallic structure)~~  ~~Test procedure: DO160F/ED14F, section 22~~  ~~Pin injection tests~~  ~~Waveform set A~~  ~~BPTU: level 3~~  ~~Functional tests (BCI and GI)~~  ~~Waveform set G or J~~  ~~BPTU: level 3~~  ~~Rationale:~~  ~~This requirement is justified at upper level.~~ | | | | |
| ~~End\_Req~~ | | | | |
| ~~Notes:~~ | | | | |

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| --- | --- | --- | --- | --- |
| ~~BRD-BPTU-0250~~ | | ~~Electrical bonding and grounding~~ | ~~Version:~~ | DELETED |
|  | ~~Covers:~~ |  | ~~Verification :~~ | ~~Analysis~~ |
| ~~Definition:~~  ~~Interfaced with the helicopter structure, the BPTU shall be compliant to [RD7] , item number 00.~~  ~~Rationale:~~  ~~This requirement is justified at upper level.~~ | | | | |
| ~~End\_Req~~ | | | | |
| ~~Notes:~~ | | | | |

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| --- | --- | --- | --- | --- |
| ~~BRD-BPTU-0490-D~~ | | ~~FPGA reset~~ | ~~Version:~~ | DELETED |
|  | ~~Covers:~~ |  | ~~Verification :~~ | ~~Analysis and Test~~ |
| ~~Definition:~~  ~~The board shall implement a reset function in order to ensure the correct driving of the two FPGA components.~~  ~~Rationale:~~  ~~This requirement is for protect data sending by FPGA.~~ | | | | |
| ~~End\_Req~~ | | | | |
| ~~Notes:~~ | | | | |

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| --- | --- | --- | --- | --- |
| ~~BRD-BPTU-0500-D~~ | | ~~Oscillator~~ | ~~Version:~~ | DELETED |
|  | ~~Covers:~~ |  | ~~Verification :~~ | ~~Test~~ |
| ~~Definition:~~  ~~COM and MON oscillators shall be different with 16MHz ± 800Hz (50ppm) of frequency.~~  ~~Rationale:~~  ~~This requirement is to provide clock to FPGA.~~ | | | | |
| ~~End\_Req~~ | | | | |
| ~~Notes:~~ | | | | |

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| --- | --- | --- | --- | --- |
| ~~BRD-BPTU-0740~~ | | ~~CAN transceiver~~ | ~~Version:~~ | DELETED |
|  | ~~Covers:~~ |  | ~~Verification :~~ | ~~Analysis and Test~~ |
| ~~Definition:~~  ~~CAN transceiver shall comply with the specification [RD2] .~~  ~~Rationale:~~  ~~This requirement is justified at upper level.~~ | | | | |
| ~~End\_Req~~ | | | | |
| ~~Notes:~~ | | | | |

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| --- | --- | --- | --- | --- |
| ~~BRD-BPTU-0660-D~~ | | ~~V~~~~3.3V~~ ~~acquisition~~ | ~~Version:~~ | DELETED |
|  | ~~Covers:~~ |  | ~~Verification :~~ | ~~Analysis~~ |
| ~~Definition:~~  ~~The power supply of acquisition channel V~~~~3.3V~~ ~~shall be acquired to correct the data value with the following formula:~~  ~~Where:~~   * ~~X represents the acquisition data~~ * ~~Y represents the acquisition data treated~~   ~~Rationale:~~  ~~This requirement is justified by the necessity to correct acquisition data.~~ | | | | |
| ~~End\_Req~~ | | | | |
| ~~Notes:~~ | | | | |

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| --- | --- | --- | --- | --- |
| ~~BRD-BPTU-1040-D~~ | | ~~Schmitt trigger on FPGA\_MON reset~~ | ~~Version:~~ | DELETED |
|  | ~~Covers:~~ |  | ~~Verification :~~ | ~~Analysis and Test~~ |
| ~~Definition:~~  ~~FPGA\_MON shall implement a Schmitt trigger function on reset input pad.~~  ~~Rationale:~~  ~~This requirement is written in order to ensure the good functionality of the component.~~ | | | | |
| ~~End\_Req~~ | | | | |
| ~~Notes:~~ | | | | |

# Traceability matrix

Board traceability matrixes are on [IAD9] .