MIPS Processor

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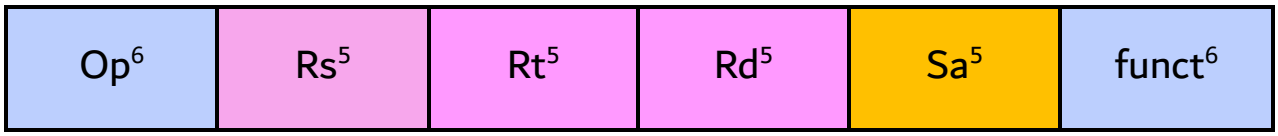
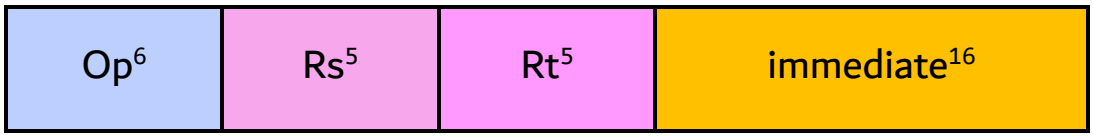
Instruction Set Architecture:

R-Type



I-Type

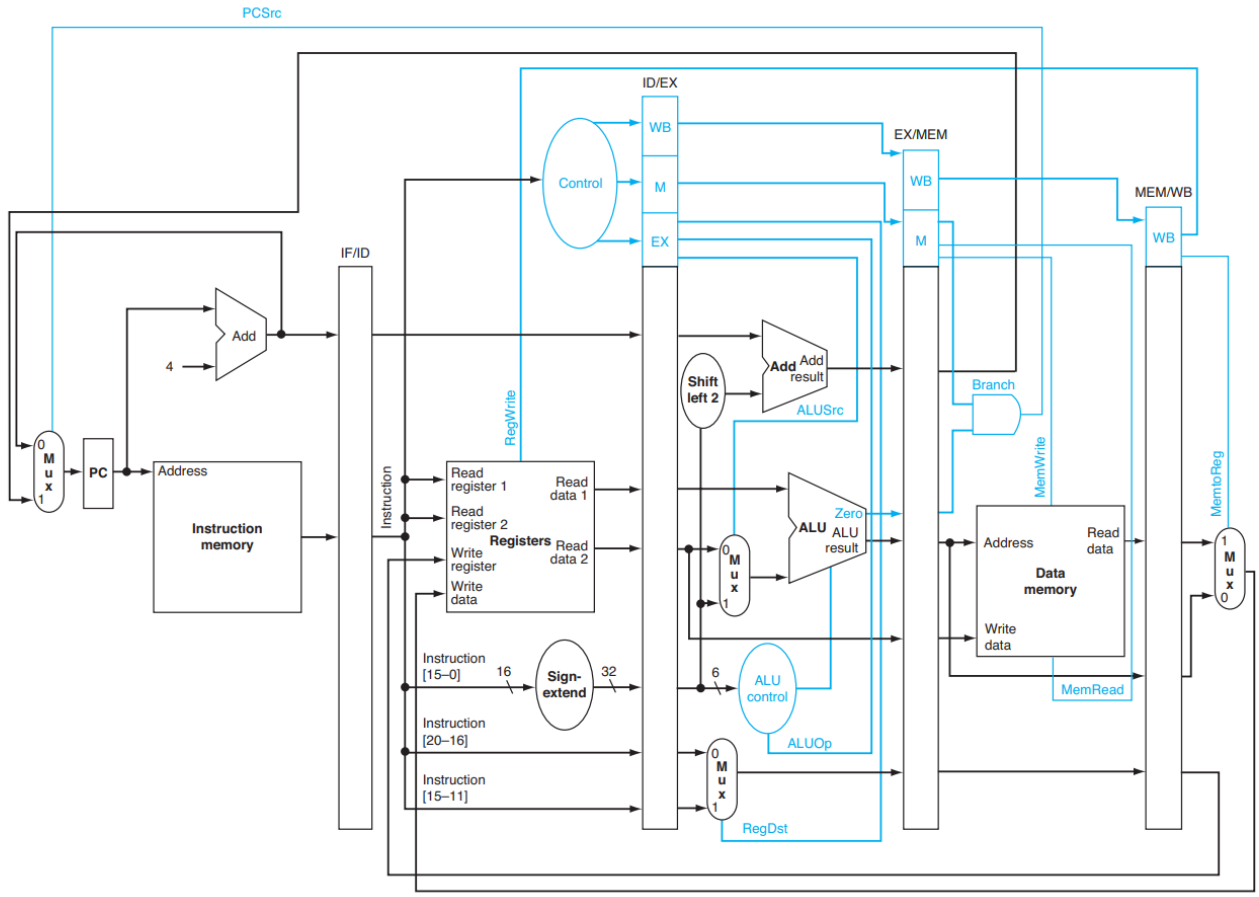


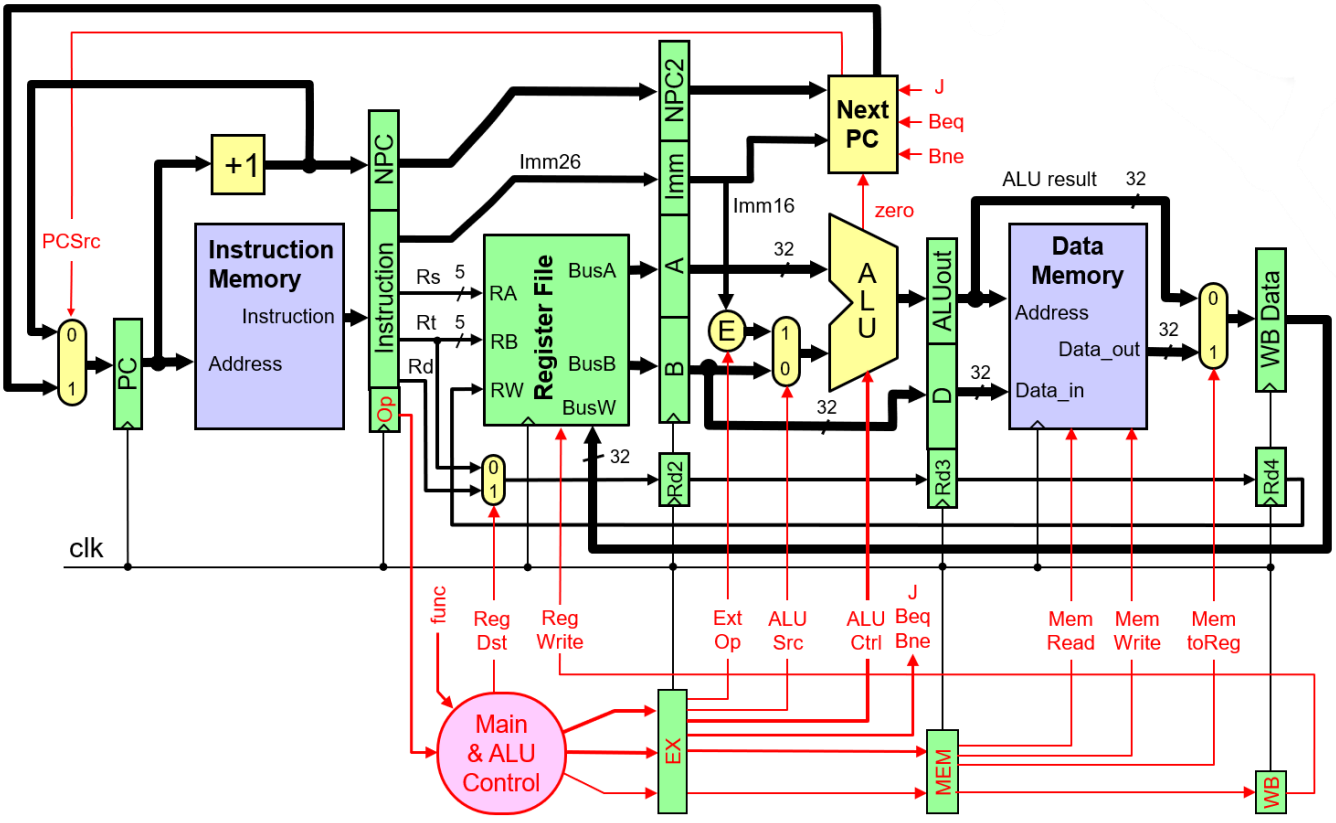
J-Type

MIPS Subset

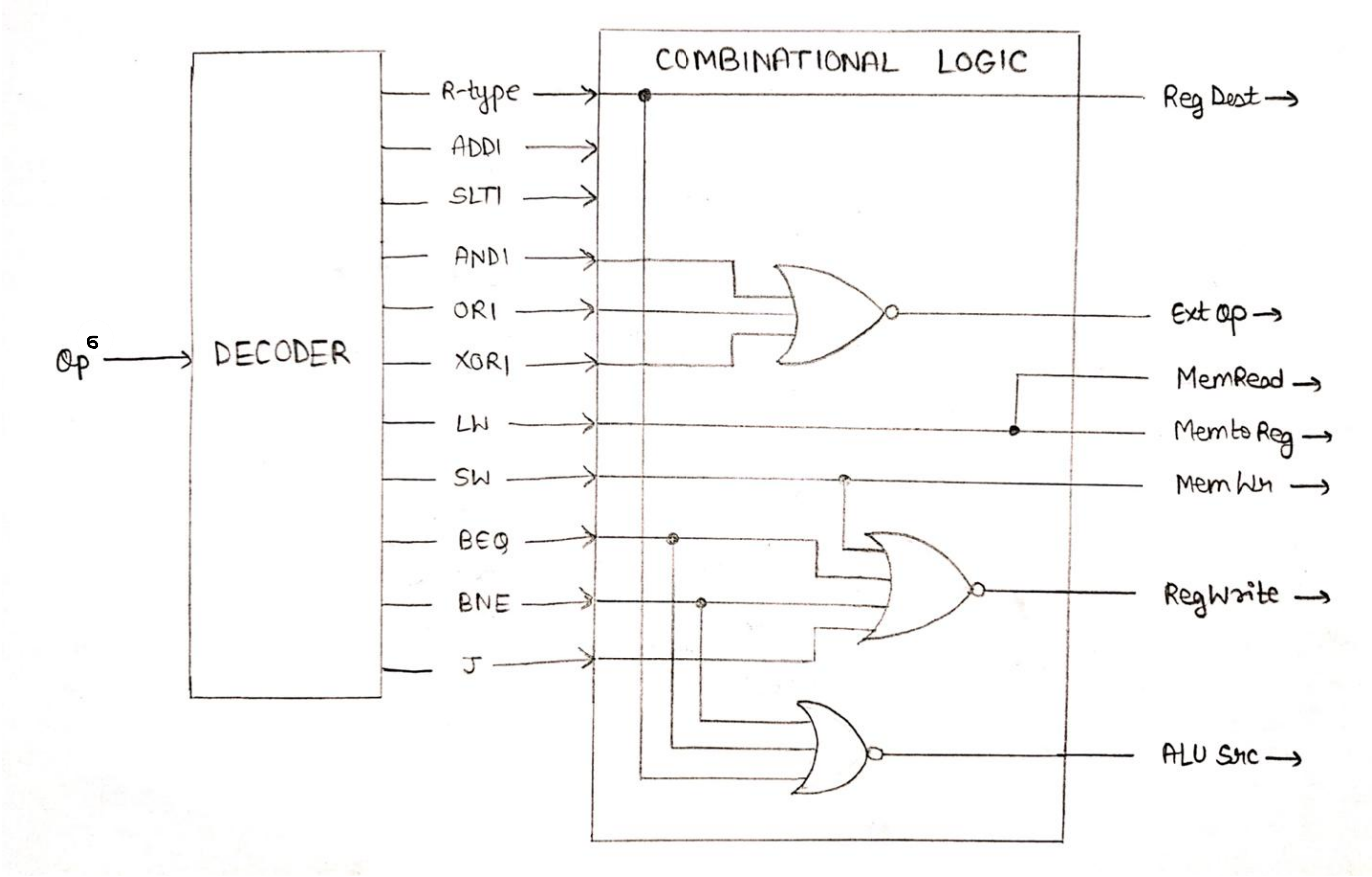
Instruction		Meaning	Format					
add	rd, rs, rt	addition	$op^6 = 0$	rs^5	rt^5	rd^5	sa = 0	f = 0x20
sub	rd, rs, rt	subtraction	$op^6 = 0$	rs^5	rt^5	rd^5	sa = 0	f = 0x22
and	rd, rs, rt	bitwise and	$op^6 = 0$	rs^5	rt^5	rd^5	sa = 0	f = 0x24
or	rd, rs, rt	bitwise or	$op^6 = 0$	rs^5	rt^5	rd^5	sa = 0	f = 0x25
xor	rd, rs, rt	exclusive or	$op^6 = 0$	rs^5	rt^5	rd^5	sa = 0	f = 0x26
slt	rd, rs, rt	set on less than	$op^6 = 0$	rs^5	rt^5	rd^5	sa = 0	f = 0x2a
addi	rt, rs, imm^{16}	add immediate	$op^6 = 0x08$	rs^5	rt^5	imm^{16}		
slti	rt, rs, imm^{16}	slt immediate	$op^6 = 0x0a$	rs^5	rt^5	imm^{16}		
andi	rt, rs, imm^{16}	and immediate	$op^6 = 0x0c$	rs^5	rt^5	imm^{16}		
ori	rt, rs, imm^{16}	or immediate	$op^6 = 0x0d$	rs^5	rt^5	imm^{16}		
xori	rt, imm^{16}	xor immediate	$op^6 = 0x0e$	rs^5	rt^5	imm^{16}		
lw	rt, imm^{16}(rs)	load word	$op^6 = 0x23$	rs^5	rt^5	imm^{16}		
sw	rt, imm^{16}(rs)	store word	$op^6 = 0x2b$	rs^5	rt^5	imm^{16}		
beq	rs, rt, $offset^{16}$	branch if equal	$op^6 = 0x04$	rs^5	rt^5	$offset^{16}$		
bne	rs, rt, $offset^{16}$	branch not equal	$op^6 = 0x05$	rs^5	rt^5	$offset^{16}$		
j	$address^{26}$	jump	$op^6 = 0x02$	$address^{26}$				

Block Diagrams





Main Control Logic



ALU Control Logic

ALU function	4-bit Coding
AND	0001
OR	0010
XOR	0011
ADD	0100
SUB	0101
SLT	0110

Opcode	ALUOp	Operation	funct	ALU function	ALU control
R-type	000	AND	100100	and	0001
		OR	100101	or	0010
		XOR	100110	xor	0011
		add	100000	add	0100
		subtract	100010	subtract	0101
		set-on-less-than	101010	set-on-less-than	0110
ADDI	100	ADD Immediate	-	add	0100
SLTI	101	set-on-less-than immediate	-	set-on-less-than	0110
ANDI	001	AND immediate	-	and	0001
ORI	010	OR immediate	-	or	0010
XORI	011	XOR immediate	-	xor	0011
LW	100	load word	-	add	0100
SW	100	store word	-	add	0100
BEQ	101	branch equal	-	subtract	0101
BNE	101	branch not equal	-	subtract	0101