# Rapid and Accurate PPA Prediction for the Template-Based Processor Design Method.


## Abstract

This paper proposes a rapid and accurate method for predicting Performance, Power, and Area (PPA) in template-based processor design workflows, which traditionally rely on time-consuming synthesis and simulation. Two prediction models are introduced: a **Multivariate Linear Regression Model (ML-PM)** and a **Multivariate Nonlinear Regression Model (MNL-PM)** based on **Amdahl's Law**. These models estimate PPA outcomes using only a limited number of RTL parameter samples, drastically accelerating the design space exploration process. Experiments using the Rocket Chip template show high prediction accuracy—**98.60% (performance), 99.19% (power), and 98.68% (area)**—demonstrating the method's effectiveness for early-stage chip design in AIoT and agile development environments.


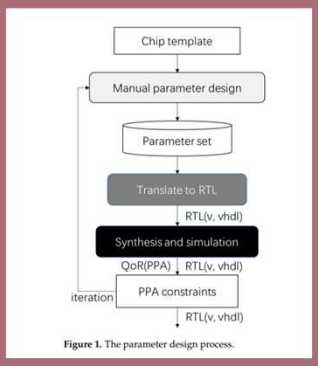


**Figure 1.** The parameter design process.

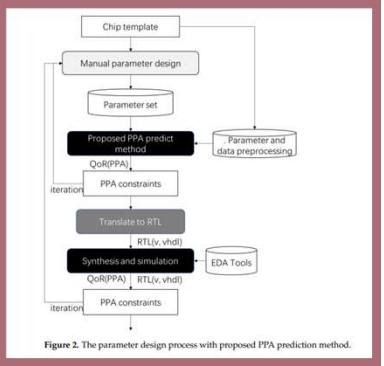


**Figure 2.** The parameter design process with proposed PPA prediction method.

## Introduction

To accelerate PPA estimation in template-based processor designs, the authors proposed a two-stage approach:

**1.Parameter and Data Preprocessing**:

They first identified 27 key design parameters from the Rocket Chip generator, covering modules such as Core, ICache, DCache, and BTB. A **base parameter set** was selected, and then each parameter was individually varied to measure its isolated effect on performance, power, and area. This preprocessing required only **42 RTL synthesis samples**, significantly reducing the data requirement.

**2.Prediction Model Construction**:

Two models were developed to estimate PPA from new parameter sets:

1. **ML-PM (Multivariate Linear Prediction Model)**:
   Assumes each parameter has an additive, independent effect. It computes PPA by summing the influence of changed parameters based on previously measured deltas.
2. **MNL-PM (Multivariate Nonlinear Prediction Model)**:
   Uses a nonlinear approach inspired by **Amdahl's Law**, modeling interactions between parameters and their impact on the overall system. This model offers improved accuracy, especially when multiple parameters change simultaneously.

**Table 2.** The portion of parameters set with value range.

| Parameter | Module | Value Range |
|---|---|---|
| mulEarlyOut | Core | **true**, false |
| divEarlyOut | Core | **true**, false |
| divSqrt | Core | **true**, false |
| nSets | Icache | 16, **32**, 64 |
| nWays | Icache | 2, **4**, 8 |
| nTLBSuperpages | Icache | 2, **4**, 8 |
| nSets | Dcache | 16, **32**, 64 |
| nWays | Dcache | 2, **4**, 8 |
| nTLBSets | Dcache | 1, **2**, 4 |
| nEntries | BTB | 256, **512**, 1024 |
| updatesOutOfOrder | BTB | true, **false** |
| historyLength | BTB | 1, **2**, 4 |
| counterLength | BTB | 2, **4**, 8 |
| ... | ... | ... |

The bold values are the defaults.

## Results

### Results Obtained by Authors:

The authors evaluated their PPA prediction method using the **Rocket Chip generator** with a 28nm technology node. They used **42 synthesized samples** from the preprocessing step as the training base and tested the prediction models on two types of parameter variations:

**1.General Parameter Changes**:

1. Created **260 random samples** with 2 to 27 parameters changed.
2. Compared predicted PPA values (from ML-PM and MNL-PM) with actual synthesis and simulation results.
3. Found that the **MNL-PM model outperformed ML-PM**, especially in accuracy and stability.
4. Achieved average prediction accuracies of:
   - **1.Performance**: 98.60% (MNL-PM) vs. 98.42% (ML-PM)
   - **2.Power**: 99.19% (MNL-PM) vs. 99.15% (ML-PM)
   - **3.Area**: 98.68% (MNL-PM) vs. 98.53% (ML-PM)

**2.Module-Specific Changes**:

1. Focused on changing parameters **within the same module** (Core, ICache, DCache, or BTB), which mimics real-world design iterations.
2. Generated **92 additional samples**.
3. Observed that **MNL-PM remained consistently accurate**, while ML-PM showed some irregularities in prediction due to parameter dependencies.

**Key Observations**:

- Prediction accuracy was higher when **fewer parameters were changed**.
- **Power predictions** were consistently the most accurate and stable across both models.
- The method proved effective even with a **small training set**, demonstrating strong generalization.

### Results obtained by us:

The initial phase of the project involved an extensive literature survey, with key references listed in the reference section. After gaining a solid understanding of the Rocket Chip Generator, we successfully extracted performance and area parameters.

For power estimation, early attempts using Genus were unsuccessful. However, in the final month, we obtained access to Synopsys tools and were able to derive a reasonable number of power measurements.

We then trained a **Random Forest (RF)** regression model to predict performance, power, and area. While the prediction accuracy was slightly lower than the models proposed in the reference paper, the difference was minimal, indicating that our model was effective and aligned closely with published approaches.

## References and github Links


1) Rapid and Accurate PPA Prediction for the Template-Based Processor Design Method..
2) Fast and Accurate PPA Modeling with Transfer Learning.
3) MasterRTL: A Pre-Synthesis PPA Estimation Framework for Any RTL Design.
4) NoCeption: A Fast PPA Prediction Framework for Network-on-Chips Using Graph Neural Network
4) https://github.com/keshavv79/RE_Sem6