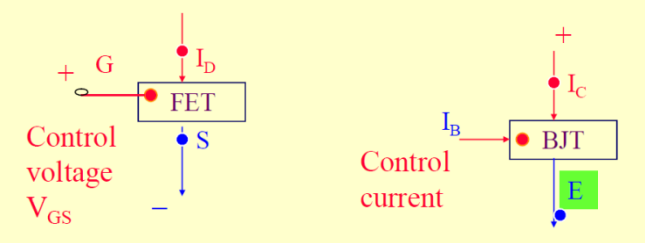
Junction Field effect transistor: Basic structure, types, working of n channel JFET, output and transfer characteristics.

Reference: Donald A Neamen, "Semiconductor Physics and Devices", Tata McGraw Hill, 4th Edition and Mr. Google

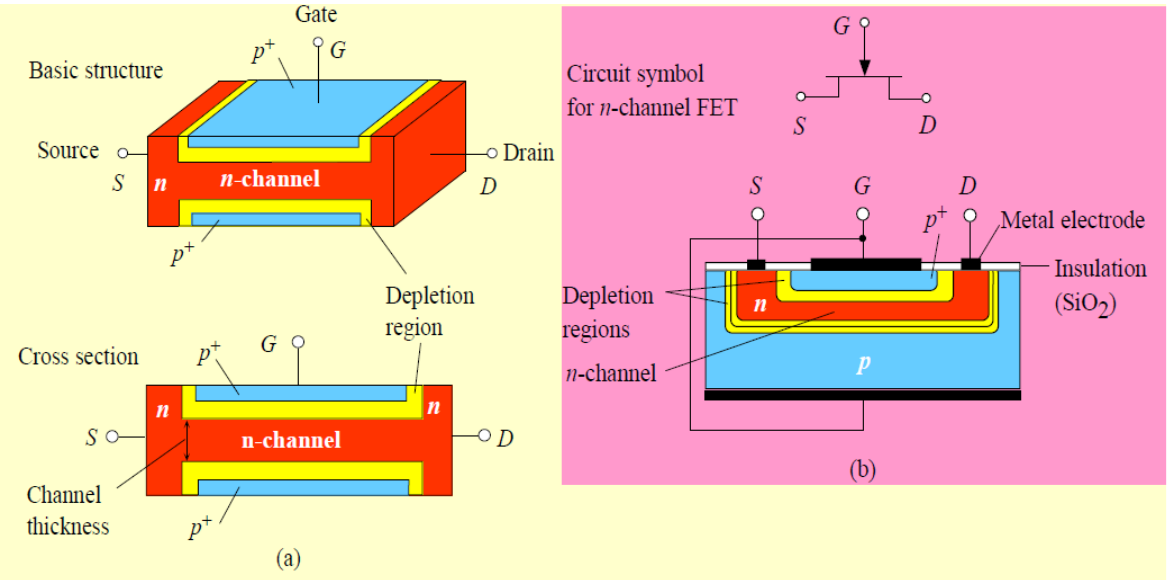
JFET Theory

BJT Vs JFET



- The conventional bipolar transistor has two type of current carriers of both polarities (majority and minority) and FET has only one type of current carriers, p or n (holes or electrons)
- The BJT is current controlled and FET is voltage controlled current between two other terminals
- JFET is a high-input resistance device, while the BJT is comparatively low.
- JFET junction is reverse-biased, the gate current is practically zero, and a very high impedance at input whereas the base current of the BJT is always some value greater than zero, for example, in µAs

Field effect transistor is a unipolar-transistor, which acts as a voltage-controlled current device and is a device in which the current is controlled and transported by carriers of one polarity (majority) only and an electric field near the one terminal controls the current between other two.



(a)The basic structure of the junction field effect transistor (JFET) with an *n*-channel. The two p^+ regions are electrically connected and form the gate. (b) A simplified sketch of the cross section of a more practical *n*-channel JFET.

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9.1 JFET CONCEPTS

9.1.1 Basic *pn* JFET Operation

The first type of field-effect transistor is the *pn* junction field-effect transistor, or *pn* JFET. A simplified cross section of a symmetrical device is shown in Fig. 9.2. The *n*-region between the two *p*-regions is known as the channel and, in this *n*-channel device, majority carrier electrons flow between the source and drain terminals. The source is the terminal from which carriers enter the channel from the external circuit, the drain is the terminal where carriers leave, or are drained from, the device, and the gate is the control terminal. Two gate terminals shown in Fig. 9.2 are tied together to form a single gate connection. Since majority carrier electrons are primarily involved in the conduction in this *n*-channel transistor, the JFET is a majority-carrier device or an unipolar device.

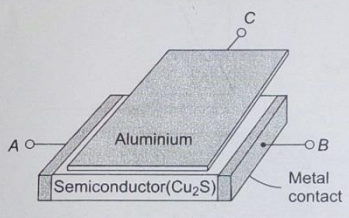

Fig. 9.1 *Idealization of the Lilienfeld transistor (From Pierret [10])*

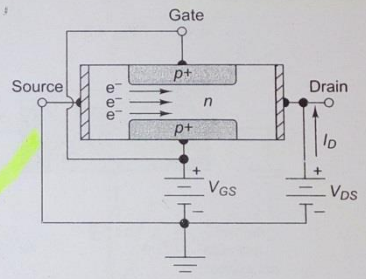

Fig. 9.2 *Cross section of a symmetrical n-channel pn junction FET*

A complementary *p*-channel JFET can also be fabricated in which the *p*- and *n*-regions are reversed from those of the *n*-channel device. Holes will flow in the *p*-type channel between source and drain and the source terminal will now be the source of the holes. The current direction and voltage polarities in the *p*-channel JFET are the reverse of those in the *n*-channel device. The *p*-channel JFET is generally a lower frequency device than the *n*-channel JFET due to the lower hole mobility.

Figure 9.3(a) shows an *n*-channel *pn* JFET with zero volts applied to the gate. If the source is at ground potential, and if a small positive drain voltage is applied, a drain current I_D is produced between the source and drain terminals. The *n* channel is essentially a resistance so the I_D versus V_{DS} characteristic, for small V_{DS} values, is approximately linear, as shown in the figure.

When we apply a voltage to the gate of a *pn* JFET with respect to the source and drain, we alter the channel conductance. If a negative voltage is applied to the gate of the *n*-channel *pn* JFET shown in Fig. 9.3, the gate-to-channel *pn* junction becomes reverse biased. The space charge region now widens so the channel region becomes narrower and the resistance of the *n* channel increases. The slope of the I_D versus V_{DS} curve, for small V_{DS}, decreases. These effects are shown in Fig. 9.3(b). If a larger negative gate voltage is applied, the condition shown in Fig. 9.3(c) can be achieved. The reverse-biased gate-to-channel space charge region has completely filled the channel region. This condition is known as *pinchoff*. The drain current at pinchoff is essentially zero, since the depletion region isolates the source and drain terminals. Figure 9.3(c) shows the I_D versus V_{DS} curve for this case, as well as the other two cases.

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The current in the channel is controlled by the gate voltage. The control of the current in one part of the device by a voltage in another part of the device is the basic transistor action. This device is a normally on or *depletion mode* device, which means that a voltage must be applied to the gate terminal to turn the device off.

Now consider the situation in which the gate voltage is held at zero volts, $V_{GS} = 0$, and the drain voltage changes. Figure 9.4(a) is a replica of Fig. 9.3(a) for zero gate voltage and a small drain voltage. As the drain voltage increases (positive), the gate-to-channel *pn* junction becomes reverse biased near the drain terminal so that the space charge region extends further into the channel. The channel is essentially a resistor, and the effective channel resistance increases as the space charge region widens; therefore, the slope of the I_D versus V_{DS} characteristic decreases as shown in Fig. 9.4(b). The effective channel resistance now varies along the channel length and, since the channel current must be constant, the voltage drop through the channel becomes dependent on position.

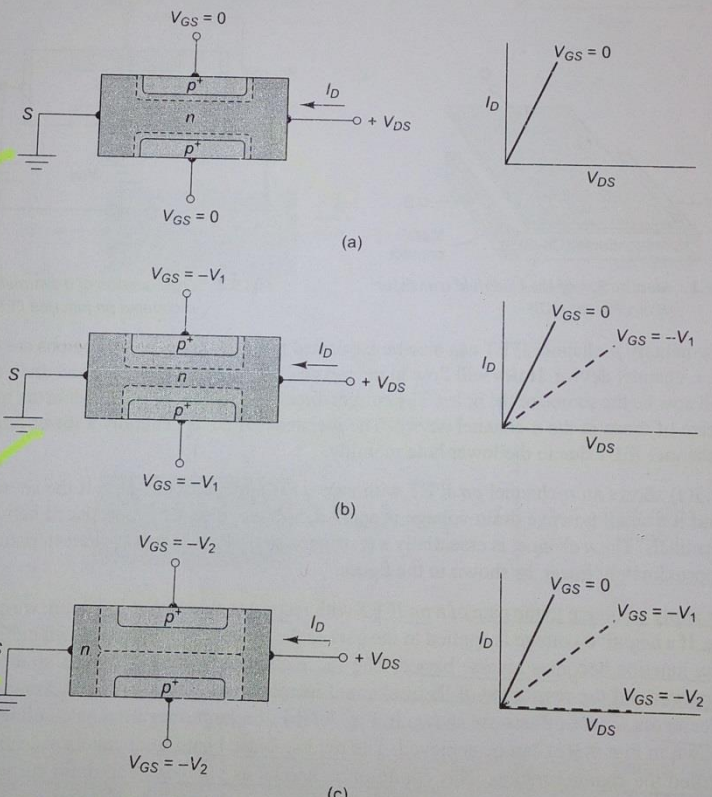

Fig. 9.3 *Gate-to-channel space charge regions and I–V characteristics for small V_{DS} values and for (a) zero gate voltage, (b) small reverse-biased gate voltage, and (c) a gate voltage to achieve pinchoff*

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If the drain voltage increases further, the condition shown in Fig. 9.4(c) can result. The channel has been pinched off at the drain terminal. Any further increase in drain voltage will not cause an increase in drain current. The *I–V* characteristic for this condition is also shown in this figure. The drain voltage at pinchoff is referred to as V_{DS}(sat). For $V_{DS} > V_{DS}$(sat), the transistor is said to be in the saturation region and the drain current, for this ideal case, is independent of V_{DS}. At first glance, we might expect the drain current to go to zero when the channel becomes pinched off at the drain terminal, but we will show why this does not happen.

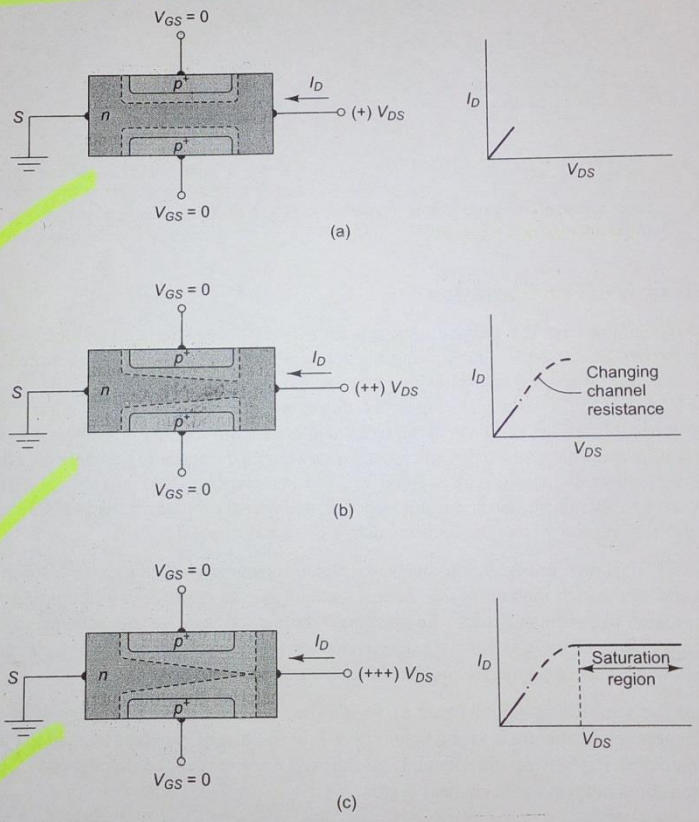

Fig. 9.4 *Gate-to-channel space charge regions and I–V characteristics for zero gate voltage and for (a) a small drain voltage, (b) a larger drain voltage, and (c) a drain voltage to achieve pinchoff at the drain terminal*

Figure 9.5 shows an expanded view of the pinchoff region in the channel. The *n*-channel and drain terminal are now separated by a space charge region which has a length ΔL. The electrons move through the *n*-channel from the source and are injected into the space charge region where, subjected to the *E*-field force, they are swept through into the drain contact area. If we assume that $\Delta L << L$, then the electric field in the *n*-channel

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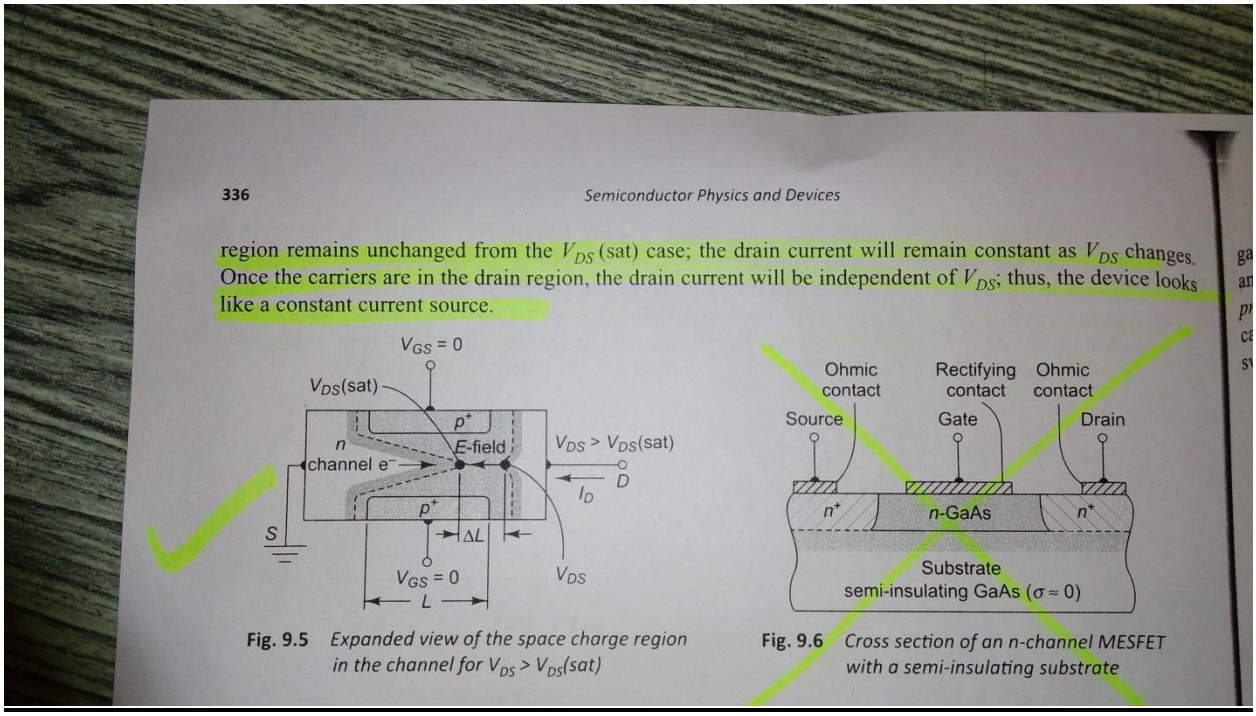

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region remains unchanged from the V_{DS} (sat) case; the drain current will remain constant as V_{DS} changes. Once the carriers are in the drain region, the drain current will be independent of V_{DS}; thus, the device looks like a constant current source.

Fig. 9.5 *Expanded view of the space charge region in the channel for $V_{DS} > V_{DS}$(sat)*

Fig. 9.6 *Cross section of an n-channel MESFET with a semi-insulating substrate*

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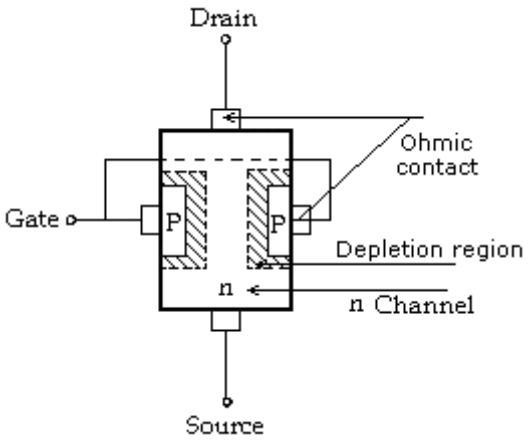
Construction & Characteristics of n-channel JFET:-



The basic construction of n – channel FET is as shown in figure. The major part of JEET is the channel between embedded P type of material. The top of the n- channel is connected to an ohmic contact called as 'Drain' (D) & Lower end of Channel is called as 'Source' (S). The two p types of materials are connected together & to the 'Gate 'terminal (G).

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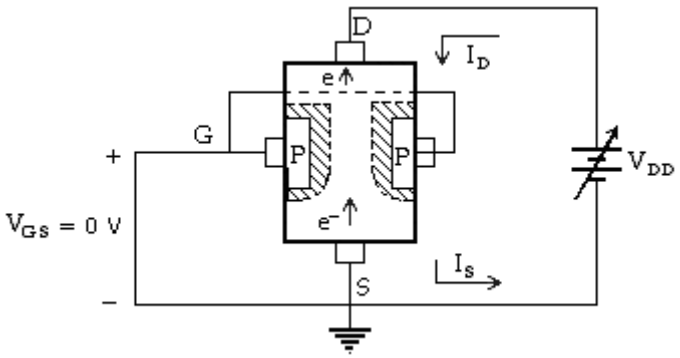
Working and Characteristic:-

1. **V_{GS} = 0$_V$, V_{DS} - Some +ve Value:-**



As shown in the figure the gate is directly connected to source to achieve $^{V}_{GS}$ = 0v, this is similar to no bias condition. The instant the voltage V_{DD} (=V_{DS}) is applied, the e^- will be drawn to the drain terminal, causing I_D & I_S to flow (i.e. I_D = I_S). Under this condition the flow of charge is limited solely by resistance of the n channel between drain & source.

It is important to note that the depletion region wider at the top of both p type of material. Since the upper terminal is more R.B. than the lower terminal (source - S).

As voltage V_{DS} is increased from 0 to few volts, the current will increase as determined by ohm's law. If still V_{DS} is increased & approaches a level referred as Vp, the depletion region will widen, causing a noticeable reduction in channel width. The reduced path of conduction causes the resistance to increase. The more the horizontal curve, the higher resistance.

If V_{DS} is increase to a level where it appears that the two depletion region would touch each other, the condition referred as 'pinch – off' will result. The level of V_{DS} that establish this condition is called as 'pinch off voltage' (V_P). At V_P, I_D should be zero, but practically a small channel still exists & very high density current still flows through the channel.

As V_{DS} is increased beyond V_P the saturation current will flow through the channel (I_{DSS}).

I_{DSS} – Drain to source saturation current from source to Gate.

2. **V_{GS} < 0V:-**

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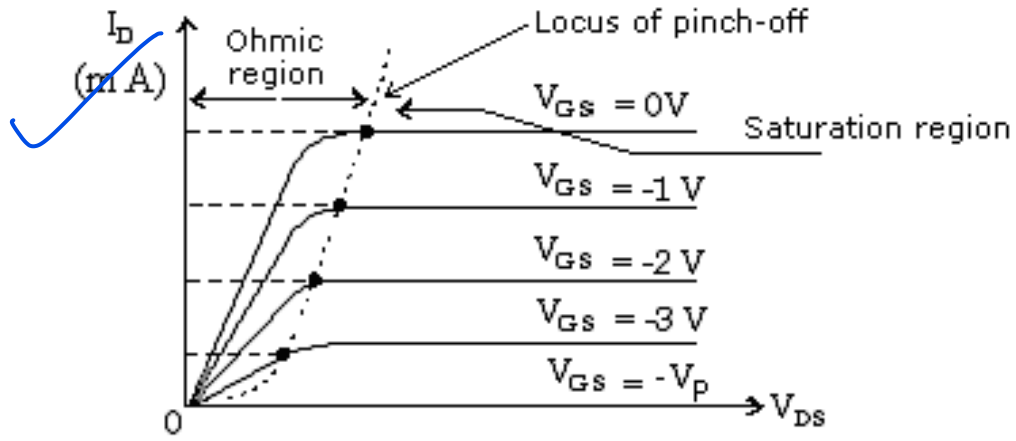
If a –ve bias is applied between gate and source, the effect of the applied –ve bias V_{GS} is to establish depletion region similar to those obtained with V_{GS} = 0V but at lower level of V_{DS}.

As V_{GS} will become more & more –ve biased, the depletion layer pinch off occur at the less & less value of V_{DS}. Eventually, when $V_{GS} = -V_P$, will be sufficiently –ve to establish a saturation level, i.e. essentially 0 mA & for all practical purpose the device has been 'turned OFF.'



The region to the right of the pinch – off locus is typically employed in linear amplifiers (Amplifier with min. distortion at applied signal) is commonly referred as the constant current, saturation or linear amplification region.

Voltage controlled region. :-The region left of pinch – off locus is called as ohmic or voltage controlled region. In this region the JEET can actually be employed as a variable register whose resistance is controlled by V_{GS}. As V_{GS} becomes more & more –ve, the slope of the curve becomes more & more horizontal, corresponding with an increasing resistance level.

$$rd = \frac{ro}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

where,

ro – the resistance with V_{GS} = 0V

rd – the resistance at particular value of V_{GS}.

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Transfer characteristic:-

The relation between I_D & $V_{GS,}$ is given by Shockley's equation.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

The squared term of equation will result in a non – linear relationship between I_D & V_{GS}.