Important numericals COA unit -4

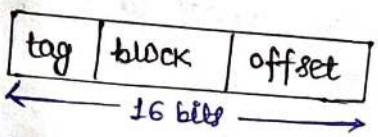
Computer Organization and Architecture (APJ Abdul Kalam Technological University)

Important Numericals of Computer Organization & Architecture.

Q. A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.

(i) How many bits are there in the tag, index, block, and word fields of the address format.

Soln:- Here, main memory size = 64K x16
i.e main memory has 2^{16} words
∴ physical address = 16 bits



Now, no. of blocks in cache = $\frac{\text{cache size}}{\text{block size}} = \frac{2^{10}}{4} = 2^8 = 256$

∴ 8 bits for block (index)

as block size = 4 words $= 2^2$ words

∴ 2 bits for offset

Now, tag bits = 16-8-2 = 6 bits.

word bits = 2

(ii) How many bits are there in each word of cache, and how they are divided into functions? Include a valid bit.

Soln:- Here, memory unit is 64K x16 = 2^{16} x16

Therefore, 16 bits for address (MAR) and 16 bits for data (MBR)

so, each word of cache will contain = data + tag + valid bit
= 16 + 6 + 1
= 23 bits.

(iii) How many blocks can the cache accomodate?

Soln:- Here, cache size = 210
block size = 4

∴ no. of blocks can cache accomodate = $\frac{2^{10}}{2^2}$ = 256 blocks.

(2)

Q. A two way set associative cache memory uses blocks of 4 words. The cache can accomodate a total of 2048 words from memory. The main memory size is 128 K x 32.

(i) Formulate all pertinent information required to construct the cache memory.

Soln:- Here, main memory size = 128 K x 32

$= 2^{12} \times 2^5$

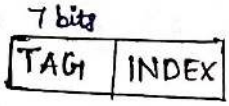
$= 2^{17}$

Cache size = 2048 words

Now, Set size of cache can accomodate = $\frac{2048}{2}$ = 1024 words of Cache

Block size = 4 words.

Now,

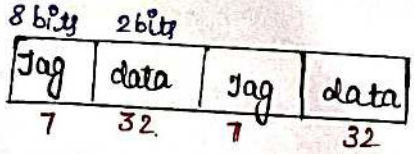


(ii) What is the size of cache memory?

Soln:- Size of cache memory = $1024 \times 2^{(7+32)}$

$= 1024 \times (78)$

Ans.



Q. Consider a cache that uses a direct mapping scheme. The size of main memory is 4K bytes and word size of cache is 2 bytes. The size of cache memory is 128 bytes. Find the following -

(i) The size of main memory address (assume each byte of main memory has an address).

Soln:- Here, size of main memory = 4K bytes

size of cache memory = 128 bytes

word size of Cache = 2 bytes

∴ Size of main memory address $\Rightarrow$ 4 K bytes = $2^{(12)}$ = 12

Ans

(ii) Address of cache block.

Soln:- Here, size of cache memory = 128 bytes

block size = word size of cache = 2 bytes

∴ no. of lines = $\frac{128}{2} = 64$

so, address of cache block is given 0 to 63. Ans

(iii) How many memory location addresses will be translated to cache address / block / location?

Soln:- Here, size of main memory = 4K bytes = 4096 bytes

no. of blocks = 4096

no. of blocks in cache = 64

each block of cache = 2 bytes

∴ no. of memory location address that will be translated to cache address = $\frac{4096}{64 \times 2} = 32$ Ans

(iv) How can it be determined if the content of the specified main memory address in cache?

Soln:- We can determine content of specified main memory address in cache using this -

$$i \bmod 2^k$$

where $i \Rightarrow$ particular memory address

$k \Rightarrow$ the number.

④

Q. A computer uses RAM chips of 1024 capacity.

(i) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 * 8 ?

Soln:- Here, available size of RAM chips = 1024 x 1

Required memory capacity = 1024 bytes

= 1024 x 8

∴ Number of chips required = $\frac{1024 \times 8}{1024}$

= 8 chips.

Ans

(ii) How many chips are needed to provide a memory capacity of 16 KB ? Explain in words how the chips are to be connected to the address bus.

Soln:-

To provide a memory capacity of 16 K bytes, chips required are = 16 x 8

= 128 chips.

no. of address line for 16K = 14 [$16K = 2^{14}$]

so, 14 lines are required to specify chip address.

Ans

Q. A ROM chip of 1024 * 8 has four select inputs and operates from 5 Volt power supply. How many pins are needed for the IC package ? Draw a block diagram and label all input and output terminals in the ROM.

Soln:- Here, size of ROM chip = 1024 * 8

number of input = 10 pins [$2^{10} = 1024$]

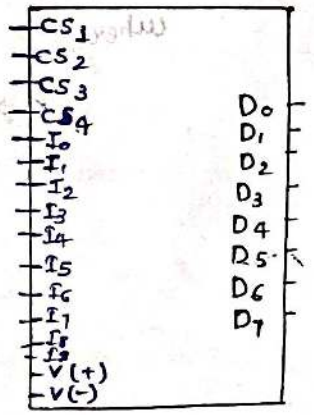
number of output = 8 pins

number of chip select = 4 pins

power = 2 pins

∴ total lines required = 24

Ans



Q. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one-word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.

(i) How many bits are there in the operation code, the register code part and the address part.

soln:-

No. of bits in address part = $2^8 \times 2^{10} = 2^{(18)} = 18$ bits AND

No. of bits in register part = 64 register = $2^6 = 6$ bits. AND

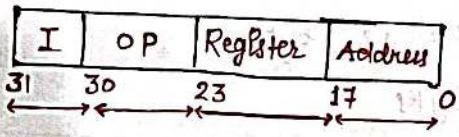
No. of bits in operation code = (Total - Indirect - address-register)

= (32 - 1 - 18 - 6) bits

= 7 bits AND

(ii) Draw the instruction word format and indicate the number of bits in each part.

soln:-



(iii) How many bits are there in the data and address inputs of the memory?

soln:-

Number of bits in address inputs = 18 }
Number of bits in data part = 32 } AND

Q. A moving arm disc storage device has the following specifications:

Number of tracks per recording surface = 200
Disk rotation speed = 2400 revolution/minute
Track storage capacity = 62500 bits.
estimate the average latency and data transfer of this device.

Soln:- Here, disk rotation speed = 2400 rpm

as we know that average latency = $\frac{1}{2}$ x rotation time

2400 rotation in 1 minute so time for 1 rotation = $\frac{1}{2} \times \frac{6}{2400}$ s = 12.5 ms AND

Track storage capacity = 62500 bits.

∴ data transfer rate = $62500 \times \frac{2400}{8}$

= 2.5×10^6 bps AND

Q. An eight way set associative cache is used in computers in which the real memory size is 232 bytes. The line size is 16 bytes, and there are 210 lines per set. Calculate the cache size and tag length.

⑥

Soln:- Here, main memory size = 232 bytes

line size = block size = 16 bytes = 2^7 bits

lines per set = 2^{10}

Since, 8 way set associative, so cache have 8 set.

No. of set = 8

Now, total no. of lines = no. of sets x no. of lines / set

$= 8 \times 2^{10}$

$= 2^3 \times 2^{10}$

$= 2^{13}$

Now, cache size = no. of sets x no. of lines/set x size of line

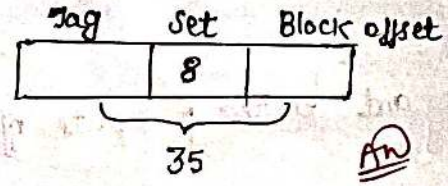
$= 8 \times 2^{13} \times 2^7$

$= 2^3 \times 2^{13} \times 2^7$

$= 2^{23}$ bits

$= 2^3 \times 2^{10} \times 2^{10}$ bytes

= 8 MBytes Ans



Ans

Block offset = $\log_2$ (line size) = $\log_2 (= 2^7) = 7$ bits

no. of set = 8

physical address = 35

∴ Tag size = PA − (Block offset + no. of set)

= 35 − (7 + 8)

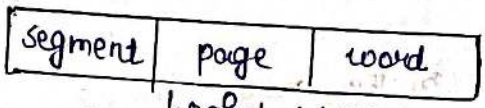
= 35 − 15

= 20 bits

Ans

Q. The logical address space in a computer system consist of 128 segments. Each segments can have up to 32 pages of 4K words each. Physical memory consist of 4K blocks of 4K words each. Formulate the logical and physical address formats.

Soln:- The logical address is denoted as-



logical Address

Here, number of segments = 128 = 2^{7}

∴ segment field contains 7 bits

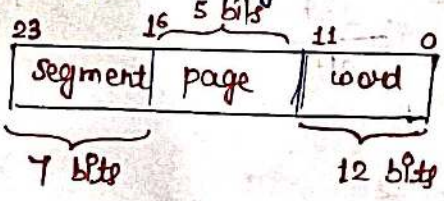
Now, no. of pages in each segment = 32 = 2^{5}

∴ page field contains 5 bits

again, no of words in each page = 4K = 2^{12}

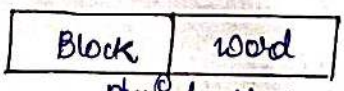
∴ word field contains 12 bits

Now, total no. of bits in logical address = 12+5+7 = 24 bits



AN

The physical address is denoted as-



Physical address.

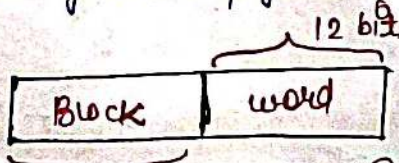
Here, no. of block field = 4K = 2^{12}

∴ block field contains 12 bits

again, no. of words in each block = 4K = 2^{12}

∴ word field contains 12 bits

Now, total no of bits in physical address = 12+12 = 24 bits.



(8) Q. An address space is specified by 24 bits and the corresponding memory space by 16 bits.

(i) How many words are there in the address space?

Soln:- Here, Number of words in address space = 2^{24}
as address space has each address of 24 bits.

(ii) How many words are there in the address space?

Soln:- No. of words in memory space = 2^{16}
as memory space has each address of 16 bits.

(iii) If a pages consist of 2K words, how many pages and blocks are there in the system.

Soln:- Here, page size = 2K words
∴ block size = page size = 2K words

∴ Number of pages = $\frac{\text{no. of words in address space}}{\text{no. of words in each page}}$

$= \frac{2^{24}}{2^{11}}$

$= 2^{13}$

$= 2^{10} \cdot 2^3$

$= 8K \quad [\because 2^{10} = K]$

Ans

again, Number of blocks = $\frac{\text{no. of words in memory space}}{\text{no. of words in each block}}$

$= \frac{2^{16}}{2K}$

$= \frac{2^{16}}{2^{11}}$

$= 2^5$

$= 32$

Ans