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Title: FPGA ENABLED SOLAR MPPT SYSTEM FOR SPACE APPLICATIONS

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DECLARATION

I Ketan Singh certify that the work embodied in this report is my own bonafide work and carried out by me under the supervision of Dr. Prashant Surana from May 2025 to June 2025 in the Department of Hydro and Renewable Energy at Indian Institute of Technology Roorkee, Roorkee, Uttarakhand, India. The matter embodied in this report has not been submitted for the completion of any other internship. I declare that I have faithfully acknowledged and given credits to the research workers wherever their works have been cited in my work in this report. I further declare that I have not willfully copied any other's work, paragraphs, text, data, results, etc., reported in journals, books, magazines, reports dissertations, theses, etc., or available at websites and have not included them in this report and have not cited as my own work.

Date

Roorkee

Ketan Singh

CERTIFICATE

This is to certify that the work contained in the report entitled "**FPGA ENABLED SOLAR MPPT SYSTEM FOR SPACE APPLICATIONS.**" submitted by Ketan Singh in fulfillment of the summer internship at SPARK 2025 at INDIAN INSTITUTE OF TECHNOLOGY ROORKEE, Roorkee, Uttarakhand, India has been carried out under my supervision and that this work has not been submitted elsewhere.

Dr. Prashant Surana
(Assistant Professor)

Department Of Hydro and Renewable Energy
Indian Institute of Technology Roorkee

ACKNOWLEDGEMENT

I would like to express my sincere gratitude to all those who have made this project possible and meaningful. I am grateful to my mentor, **Dr. Prashant Surana**, who has been a constant source of guidance and support throughout this project. I have learned a great deal from his expertise and experience, and his feedback and encouragement have been instrumental in my growth during this endeavor. I am also thankful to **The Department of Hydro and Renewable Energy**, and **SPARK IIT ROORKEE**, for providing me with an opportunity to undergo summer internship at **Indian Institute of Technology IIT Roorkee**. Lastly, I would like to express my heartfelt gratitude to my family and friends for their constant support and encouragement throughout this journey. This project, titled **"FPGA Enabled Solar MPPT System for Space Applications,"** has been a valuable learning experience for me. Thank you all for contributing to my growth and development during this endeavor.

ABSTRACT

This project focuses on the development of a real-time, FPGA-based Maximum Power Point Tracking (MPPT) system optimized for space-grade photovoltaic (PV) applications. The system architecture integrates a BOOST converter for voltage step-up and regulation, modeled and simulated using MATLAB Simulink. The MPPT algorithm based on perturb and observe (P&O) logic has been validated in simulation and is currently being implemented in hardware on the Microchip PolarFire SoC Discovery Kit. This implementation uses the on-chip FPGA fabric to achieve fast and reliable control, which is important for use in space environments where conditions are harsh and unpredictable.

Real-time acquisition of PV voltage and current is achieved via the MIKROE-3394 ADC Click Board, featuring the ADS1115 16-bit ADC, interfaced using a custom designed I2C controller in Verilog. The input to the system is provided by a programmable solar PV simulator (Chroma 62050H-600S), enabling controlled emulation of varying solar irradiance and temperature conditions. The acquired data is processed onboard, and the optimized duty cycle for the BOOST converter is updated to ensure operation at the maximum power point. The system demonstrates a robust, low-latency digital control strategy suited for spaceborne power systems where traditional microcontroller-based solutions may fall short.

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Abbreviations

- MPPT: Maximum Power Point Tracking
- MPP: Maximum Power Point
- PV: Photo Voltic
- P&O: Perturb & Observe
- INC: Incremental Conductance
- SoC: System on Chip
- DSP: Digital Signal Processor
- ASIC: Application Specific Integrated Circuit
- I2C: Inter-integrated Circuits
- SCL: Serial Clock
- SDA: Serial Data
- UART: Universal Asynchronous Receiver-Transmitter
- FPGA: Field Programable Gate Array
- ADC: Analog to Digital Converter
- RISC-V: Reduced Instruction Set Computing - V
- PWM: Pulse Width Modulation

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Chapter 1

Introduction

1.1 Motivation

With the growing demand for efficient and sustainable energy solutions in space missions, solar photovoltaic (PV) systems have become a primary power source for satellites, space stations, and exploratory spacecraft. However, the output power from PV panels is highly sensitive to variations in solar irradiance and temperature conditions that can change rapidly in extraterrestrial environments. To ensure maximum energy extraction under such conditions, a fast and reliable Maximum Power Point Tracking (MPPT) system is essential.

1.2 Literature Review

The increasing reliance on PV systems in space missions has driven significant research in the areas of MPPT control, power electronics, and reliable embedded system design. MPPT algorithms are essential for ensuring maximum energy extraction from PV panels under varying environmental conditions. Among the various MPPT techniques, the Perturb and Observe (P&O) and Incremental Conductance (INC) methods are widely used due to their simplicity and ease of implementation [1][2]. Several studies have analyzed their dynamic performance, convergence speed, and stability under rapid irradiance fluctuations common in space environments.

Traditionally, MPPT has been implemented using microcontrollers or DSPs. However, these platforms face limitations in speed, parallelism, and radiation tolerance, which are critical in space environments. Recent studies have shown that FPGAs offer significant advantages, including faster response, deterministic control, and better reliability under harsh conditions.

In the domain of power converters, the BOOST converter is a preferred topology for stepping up the voltage from PV sources, especially when operating under low-light conditions. Several simulation-based studies have focused on BOOST converters to maintain output voltage regulation with adjusting the duty cycle through MPPT control logic.

1.3 Research Gap

While numerous MPPT systems have been developed using microcontrollers and DSPs, these platforms often struggle with the processing speed, timing determinism, and radiation resilience required in space environments. Most existing implementations focus on terrestrial solar applications, with limited emphasis on FPGA-based MPPT systems optimized for space missions [3][4].

Additionally, there is a lack of comprehensive, low-latency hardware implementations that combine MPPT logic, power converter control, and high-resolution sensing for space-grade PV systems. This project aims to fill this gap by developing a complete FPGA-based MPPT system suitable for space applications, using the PolarFire SoC platform and real-time ADC interfacing [1][4].

Chapter 2

Problem Statement

2.1 Objective

The objective of this project is to design and implement a real-time, FPGA-based MPPT system working on P&O algorithm and using a BOOST converter for space grade solar applications, integrating high-resolution voltage and current sensing with control logic on the Microchip PolarFire SoC Discovery Kit FPGA Board for efficient and reliable power extraction under varying environmental conditions.

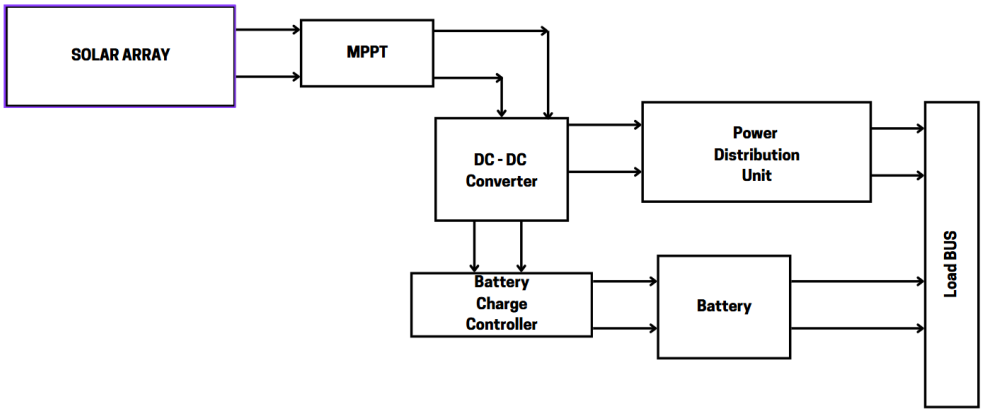

Fig.1 Flow Chart of Typical MPPT System

2.2 Study of existing solutions

2.2.1 Micro-Controllers and FPGA Based Systems

Conventional MPPT systems are commonly implemented using microcontrollers (e.g., STM32, Arduino) or DSPs (e.g., TI C2000 series), which execute algorithms like P&O, INC, and Constant Voltage methods. These platforms are favored for their ease of programming and cost-effectiveness but face limitations in handling high-speed, real-time control, especially in rapidly changing environments like space. But the microcontrollers still rely on sequential execution, which is less deterministic than hardware logic.

In satellite systems, radiation-hardened microcontrollers and ASICs are commonly used for power tracking and regulation. These systems employ MPPT logic within dedicated Power Conditioning Units and often follow architectures such as Peak Power Tracking or Direct Energy Transfer [1][3][5]. While effective, these systems are typically custom built and lack flexibility for algorithm upgrades or reconfiguration once deployed

FPGAs are being explored in a number of studies for MPPT due to their parallel processing capabilities and precise timing control. However, most implementations are focused on grid-connected or terrestrial PV systems. Few utilize radiation-tolerant FPGA platforms like the Microchip PolarFire SoC, which combine low power consumption with on-chip reliability features suitable for space environments.

More recently, radiation-tolerant FPGAs (e.g., Microchip RTG4, Xilinx Virtex-5QV) are being explored for space applications due to their deterministic timing, reconfigurability, and parallel processing capabilities. These

platforms support real-time integration of MPPT algorithms, sensor data acquisition, and control of DC-DC converters within a single chip, reducing latency and improving reliability.

2.3 Summary of Work

This project aimed to develop an operating hardware setup of FPGA based MPPT system tailored for space applications. The initial phase involved simulating a closed-loop BOOST converter and implementing the P&O MPPT algorithm using MATLAB Simulink to validate the control logic.

For hardware development, the Microchip PolarFire SoC Discovery Kit was selected due to its suitability for real-time control and space relevant features. The ADS1115-based MIKROE-3394 ADC Click Board was chosen for voltage and current sensing from a solar PV simulator (Chroma 62050H-600S). A custom Verilog-based I2C master was partially developed to interface with the ADC, and efforts were made to implement UART communication for data display.

As of now, PWM signal generation from the FPGA board has been successfully achieved, indicating readiness for controlling a DC-DC BOOST converter. Although full hardware integration is ongoing, the simulation results and initial FPGA implementation lay a strong foundation for a complete real-time MPPT system suitable for space applications.

Chapter 3

Overview of Core Technologies

3.1 Boost Converters

A **Boost Converter** is a type of DC-DC converter that steps up the input voltage to a higher output voltage while reducing the current, conserving power. It operates using a high-speed switching device (typically a MOSFET or IGBT), an inductor, a diode, and an output capacitor. During the switch-on phase, energy is stored in the inductor, and during the switch-off phase, the energy is transferred to the load through the diode, resulting in a higher output voltage. The output voltage is regulated by adjusting the duty cycle of the switch, making the Boost Converter suitable for applications like photovoltaic systems where the input voltage can fluctuate. In closed-loop configurations, feedback control ensures that the output remains stable despite variations in input or load conditions.

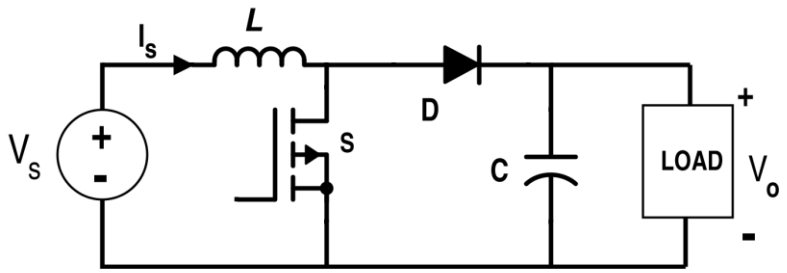

Fig.2 Boost Converter Circuit

3.2 Maximum Power Point Tracking

Maximum Power Point Tracking (MPPT) is a control technique used in PV systems to continuously extract the maximum possible power from a solar panel under varying environmental conditions. The power output of a PV panel depends on both the irradiance and temperature, and it exhibits a non-linear current-voltage (I-V) characteristic with a unique point known as the Maximum Power Point (MPP) [5]. MPPT algorithms, such as P&O or INC, dynamically adjust the operating voltage or current of the converter interfacing the PV panel to ensure operation at this optimal point. In this project, MPPT is applied to control a Boost Converter, optimizing energy transfer from the PV source to the load, and enabling higher efficiency even under changing input conditions.

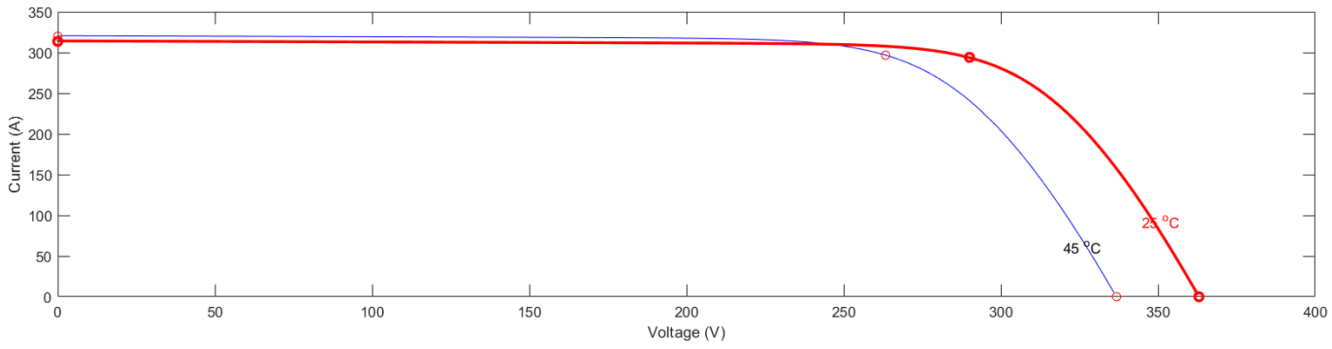

Fig.3 I-V Characteristics of a Solar Cell

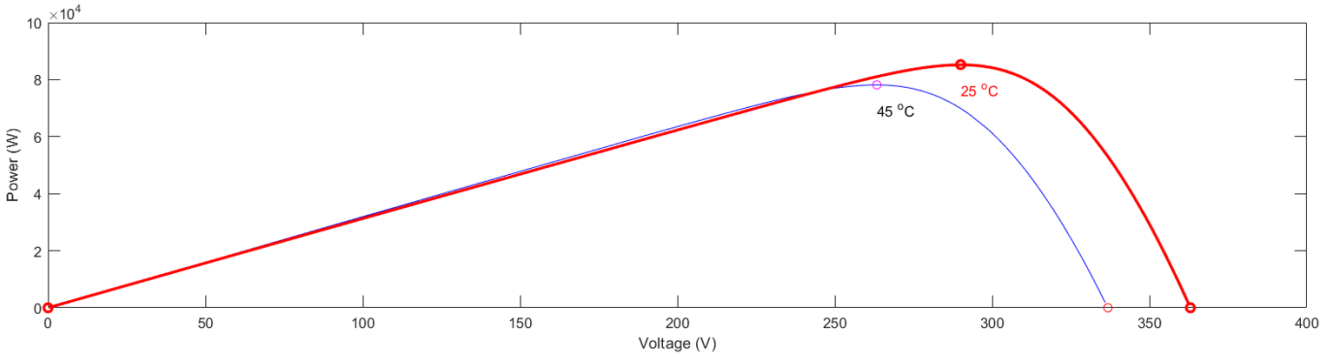

Fig.4 P-V Characteristics of a Solar Cell

3.2.1 Perturb and Observe Algorithm

Perturb and Observe is one of the most widely used MPPT algorithms due to its simplicity and ease of implementation. The algorithm operates by periodically perturbing (i.e., slightly increasing or decreasing) the operating voltage of the PV system and observing the resulting change in output power. If the power increases following the perturbation, the algorithm continues in the same direction; otherwise, it reverses the direction of perturbation. This iterative process allows the system to converge toward the Maximum Power Point (MPP). Although P&O is efficient under slowly varying conditions, it may exhibit steady-state oscillations around the MPP and can momentarily track away from it under rapidly changing irradiance [3][4]. Despite these limitations, its low computational complexity makes it suitable for real-time hardware implementation, such as on an FPGA.

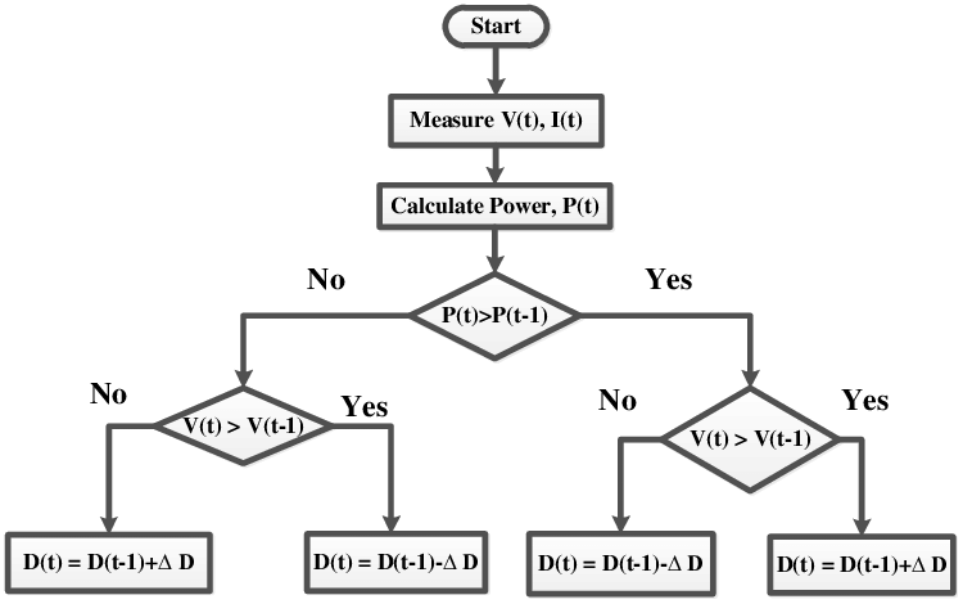

Fig.5 P&O Algorithm Flow Chart

3.2.2 Incremental Conductance

Incremental Conductance is a more accurate MPPT algorithm that overcomes some limitations of the P&O method, particularly under rapidly changing irradiance. It is based on the principle that the derivative of power with respect to voltage (dP/dV) is zero at the MPP. By comparing the incremental conductance (ΔI/ΔV) to the instantaneous conductance (I/V), the algorithm determines whether the operating point is to the left or right of the

MPP and adjusts the voltage accordingly. When ΔI/ΔV = –I/V, the system is at MPP. This method provides faster and more stable convergence with fewer oscillations around the MPP, making it suitable for environments with dynamic solar conditions [1]. However, INC is slightly more complex computationally compared to P&O and may require higher resolution sensing and control.

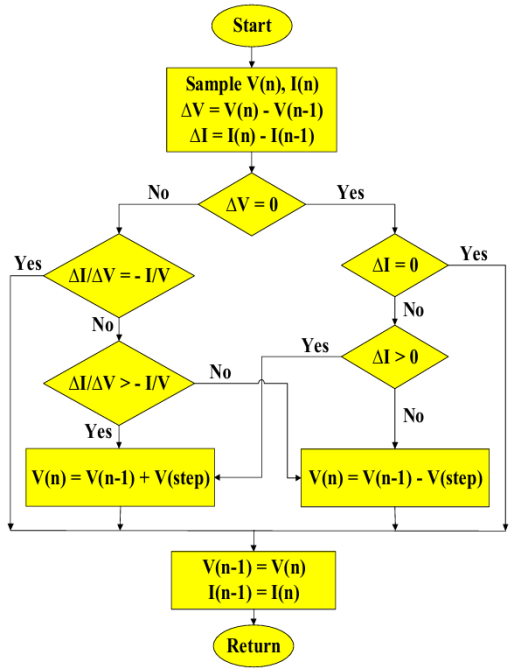

Fig.6 INC Algorithm Flow Chart [1]

3.3 Inter-Integrated Circuit Protocol

Inter-Integrated Circuit (I2C) is a synchronous, multi-master, multi-slave, two-wire communication protocol commonly used for short-distance communication between microcontrollers and peripheral devices. It uses two lines: SCL (clock) and SDA (data), both of which are open-drain and require pull-up resistors. I2C enables efficient and low-pin-count communication with devices like ADCs, sensors, and memory modules. Each device on the I2C bus is assigned a unique 7-bit or 10-bit address, and communication is initiated by the master through a start condition followed by the address and read/write bit [7][8]. In this project, the I2C protocol is implemented on FPGA fabric to interface with the ADS1115-based MIKROE-3394 ADC, enabling real-time data acquisition for MPPT control.

Key features of the protocol include:

- Two-wire communication: SDA (data) and SCL (clock)
- Supports multiple slaves with unique addresses on a single bus
- Synchronous data transfer controlled by the master device
- Open-drain architecture with external pull-up resistors
- Suitable for low-speed, low-complexity peripheral communication
- Used to interface the ADS1115 ADC with the PolarFire SoC FPGA

3.3.1 Working of I2C protocol

- The I²C communication begins with the START condition, which is generated by the controller (formerly called "master"). This is defined by a high-to-low transition on the SDA (data) line while the SCL (clock) line remains high. This unique condition signals to all connected devices on the bus that a communication sequence is starting. Once the START condition is detected, all devices on the bus become alert and begin monitoring the data to see if they are being addressed [8].

- Immediately following the START condition, the controller sends a 7-bit address (or 10-bit in some cases) to identify the target device it wants to communicate with. This address is followed by a 1-bit Read/Write (R/W) flag, where '0' indicates a write operation and '1' indicates a read operation. The entire 8-bit address frame is sent MSB (most significant bit) first.

- After the address + R/W bit is sent, the controller releases the SDA line and generates the ninth clock pulse on SCL. During this time, the addressed target device (formerly "slave") must pull the SDA line low to acknowledge (ACK) that it has received the address and is ready to proceed. If no device acknowledges, the SDA line stays high (NACK), and the controller may terminate or restart the transaction [9].

- If the address is acknowledged, data transfer begins. The controller (or target, depending on the direction) sends 8-bit data words, MSB first. After each byte, the receiver sends an ACK (logic 0) or NACK (logic 1) bit during the ninth clock cycle, just like with address acknowledgment. This sequence can continue for any number of bytes, depending on the operation (e.g., multi-byte write/read).

- If the controller wishes to switch from writing to reading (or vice versa) without releasing the bus, it issues a Repeated START condition—identical in form to the initial START, but used mid-transfer. When the communication is complete, the controller issues a STOP condition, defined by a low-to-high transition on SDA while SCL is high [10][11]. This signals that the bus is now free and available for the next communication.

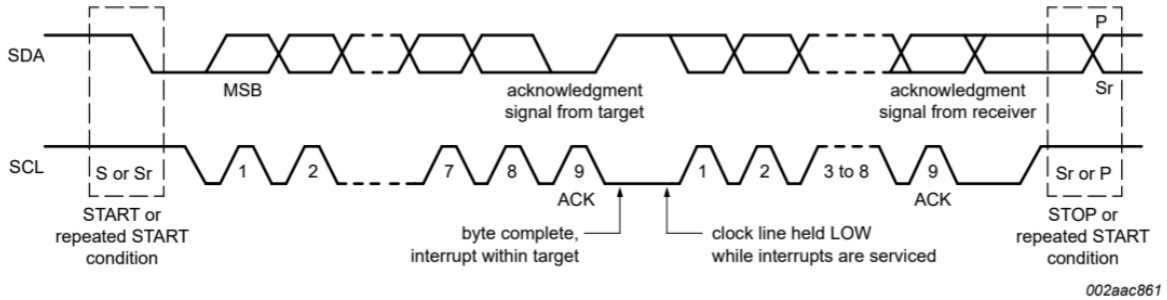

Fig.7 Representation of I2C Communication [11]

3.4 PolarFire SoC Discovery Kit

The PolarFire SoC Discovery Kit is a compact development platform featuring Microchip's PolarFire SoC FPGA, which combines a low-power FPGA fabric with a hardened RISC-V processor subsystem. It is particularly suitable for real-time control and space-grade applications due to its deterministic timing, radiation tolerance, and

support for hardware-level implementation of algorithms. In this project, the kit is used to implement MPPT control logic, generate PWM signals for the Boost converter, and interface with sensors via I2C [9][10].

The key features of the kit include:

- Low-power, radiation-tolerant FPGA fabric ideal for space applications
- 160 MHz and 2 MHz on-board clock sources for high-speed logic and precise timing
- Support for hardware-based I2C, UART, and PWM implementations
- mikroBUS expansion socket for interfacing with external ADC modules
- Compatible with Libero SoC Design Suite for Verilog-based FPGA development
- Integrated USB-UART for serial communication and debugging

3.5 Mikroe – 3394 ADC

The MIKROE-3394 ADC 8 Click Board is a precision analog-to-digital conversion module based on the Texas Instruments ADS1115 16-bit ADC. It interfaces with digital systems via the I2C protocol and is designed for accurate measurement of low-level analog signals. The board provides programmable gain, high-resolution conversion, and flexible input configurations, making it ideal for sensing applications in embedded control systems. In this project, it is used to measure voltage and current signals from a solar PV simulator, with digital output fed to the FPGA for real-time processing and MPPT control. The mikroBUS form factor allows seamless connection to the PolarFire SoC Discovery Kit.

The key features of the module include:

- ADS1115 16-bit ADC with programmable gain and 860 SPS sampling rate
- I2C communication for easy interfacing with FPGA logic
- mikroBUS form factor, compatible with PolarFire SoC Discovery Kit
- On-board pull-up resistors and I2C address selection for ease of use
- Wide input voltage range support, suitable for current and voltage sensors

Chapter 4

Proposed Method

4.1 Simulation of Closed Loop Control Boost Converter

4.1.1 Objective

The primary objective of simulating a closed-loop control algorithm for a BOOST converter in MATLAB Simulink is to achieve stable and accurate output voltage regulation using real-time feedback. The simulation models essential components such as inductors, capacitors, and switching devices, enabling precise tuning of control parameters. This virtual environment allows for testing and validation of control strategies like duty cycle modulation before hardware implementation, ensuring optimized performance and reduced design errors in the actual system.

4.1.2 Assumption and Dependencies

The assumptions to be taken for the application are:

- The simulation environment, MATLAB Simulink, is properly configured with all required toolboxes and libraries for boost converter and real-time simulation.
- The simulation assumes ideal conditions without considering external disturbances such as temperature variations or hardware imperfections.

The dependencies to be taken for the application are:

- The control algorithm relies the values of Inductor and Capacitors which were determined by the following formulas:
  - $D = 1 - \frac{V_{in}}{V_{out}}$
  - $L = \frac{V_{in}D}{f_s \Delta I_l}$
  - $C = \frac{I_{out}D}{f_s \Delta V_{out}}$
  - $I_{in} = \frac{I_{out}}{1-D}$
- The Values of Inductor Current Ripple (ΔI_l) was assumed as 30%, the value of Capacitor Voltage ripple (ΔV_c / ΔV_{out}) was assumed as 3%.
- The Input voltage for the Boost converter was assumed to be 200 V and the Desired output between 300-600 V

- The project depends on external resources like datasheets, and libraries for implementing the closed-loop control algorithm.

4.1.3 Advantages offered by the System

The major advantages provided by the system are:

- **Customizability:** The simulation environment allows us to design and test control algorithms tailored specifically to the requirements of the Boost Converter, such as application in space.
- **Scalability:** The MATLAB Simulink platform can handle simulations of varying complexity, from simple models to complete MPPT systems, ensuring reliable performance regardless of system size or configuration.

4.2 Simulation of P&O MPPT Algorithm

4.2.1 Objective

The main objective of simulating the Perturb and Observe (P&O) MPPT algorithm in MATLAB Simulink is to achieve stable and accurate tracking of the maximum power point for photovoltaic systems using real-time feedback. The simulation includes key components such as PV array, allowing precise tuning of control parameters within a Boost converter setup. This virtual environment enables thorough testing and validation of the MPPT strategy particularly the duty cycle modulation before deploying it to hardware. As a result, it helps in optimizing system performance and minimizing potential design errors during implementation..

4.2.2 Assumption and Dependencies

The assumptions to be taken for the application are:

- The PV module in Simulink accurately represent the real system behavior under varying irradiance and temperature conditions.
- The P&O algorithm converges to the correct maximum power point under standard test conditions.
- The Solar array was Assumed to have 10 Series connected modules per string with 40 strings.
- The Voltage at MPP was assumed to be 290V with a current of 294A, making the power at MPP to be 85kW

The dependencies to be taken for the application are:

- The performance of the algorithm is influenced by the chosen sampling time, simulation step size, and solver configuration in Simulink.

4.3 Programing the FPGA board

4.3.1 Objective

The main objective of programming the Microchip PolarFire SoC FPGA board is to implement and test the MPPT control algorithm in real-time for a Boost converter-based solar energy system. The goal is to translate the P&O logic into Verilog and integrate it with PWM generation, ADC interfacing, and UART communication. This hardware-level implementation allows precise control of the converter and real-time acquisition of voltage and current data from the PV simulator. By using the FPGA's deterministic timing and parallel processing capabilities, the system ensures high-speed operation and responsiveness required in space-grade energy applications.

4.3.2 Assumptions and Dependencies

The assumptions to be taken for the application are:

- The PolarFire SoC Discovery Kit is properly configured with the necessary IP cores and clock settings, and all essential I/O connections (PWM, I2C, UART) are correctly mapped and functioning.

- The simulated MPPT algorithm behaves similarly when implemented in hardware logic, allowing seamless translation from MATLAB Simulink to Verilog-based design.

The Dependencies to be taken for the application are:

- Successful operation depends on the correct functioning of the ADC module (MIKROE-3394) and its I2C communication with the FPGA for real-time voltage and current feedback.

- The development process relies on the Libero SoC Design Suite for synthesizing and programming the FPGA, as well as compatibility with the board's supported clock frequencies and IP cores.

Chapter 5

Results and Discussion

5.1 Closed Loop Boost Converter Simulation

5.1.1 Simulation Model

The closed-loop control algorithm was successfully simulated in MATLAB Simulink, demonstrating stable boost converter operation. The algorithm efficiently regulated voltage based on real-time feedback, with minimal overshoot and steady-state error. The results showed improved dynamic response and smooth transition between different duty cycles, confirming the robustness of the control strategy.

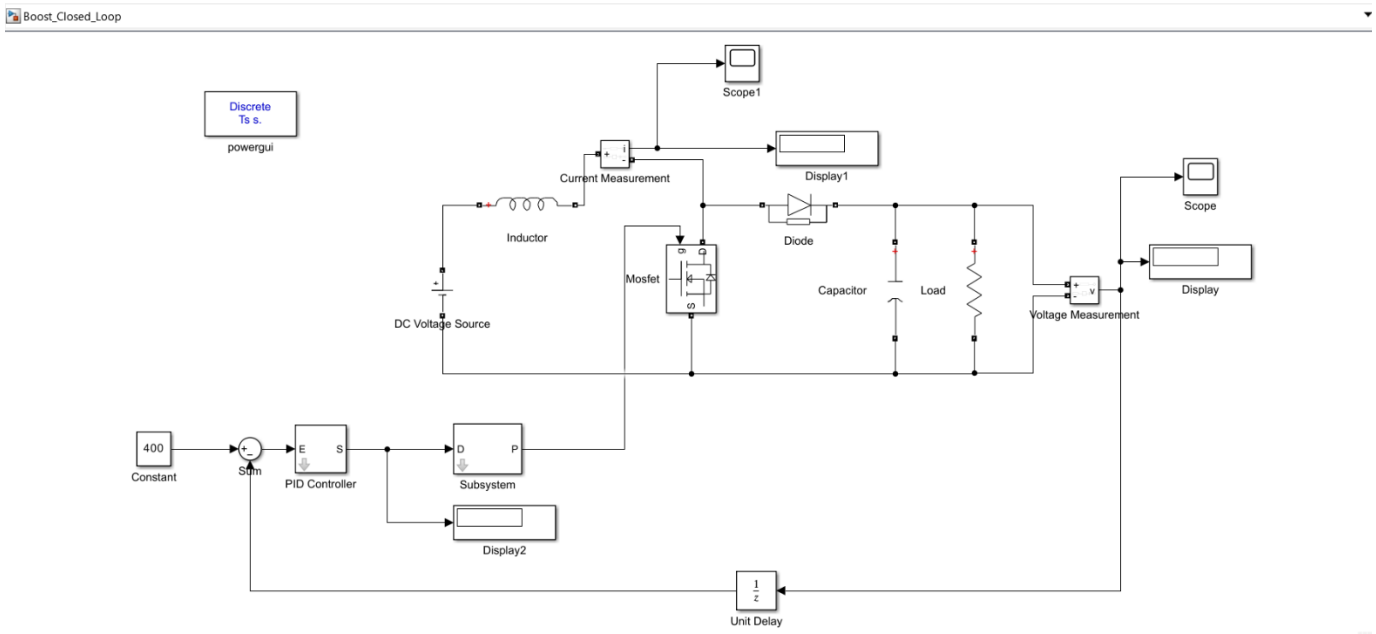

Fig.8 MATLAB Simulink Model for Closed Loop Boost Converter

The model consists of a boost converter circuit, a PID controller mask and a PWM generator mask. The input to the PID controller is the error signal obtained from the difference of the actual voltage output and the desired voltage. Controller generates the Duty cycle which is then fed to the PWM generator and then given to the MOSFET's gate port.

The Boost converter was developed considerinf

5.1.2 Simulation Subsystems

- **PID Controller mask:**
  The PID (Proportional-Integral-Derivative) controller processes the voltage error (difference between desired and actual voltage) to generate a duty cycle signal. This ensures precise and stable speed control by dynamically adjusting the control signal based on the magnitude and trend of the error.

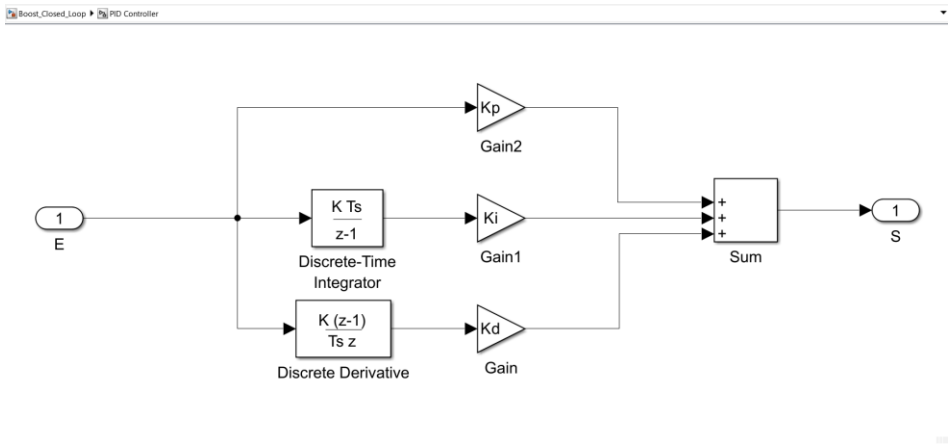

Fig.9 PID Controller Mask

- **PWM Generator Mask**:
  The PWM generator Mask Consists of a Carrier signal generated through the relational operator block, then to generate the PWM signal the carrier wave and the duty cycle from the PID controller are compared through the Relational Operator.

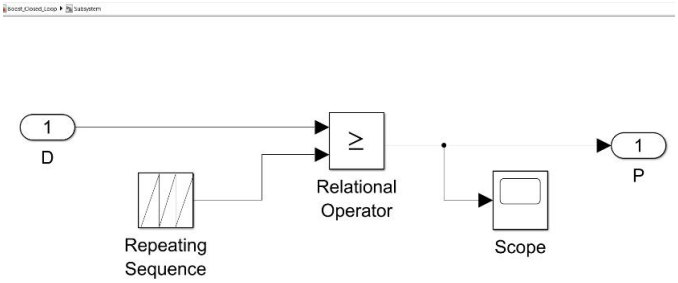

Fig.10 PWM Generator Mask

5.1.3 Simulation Result

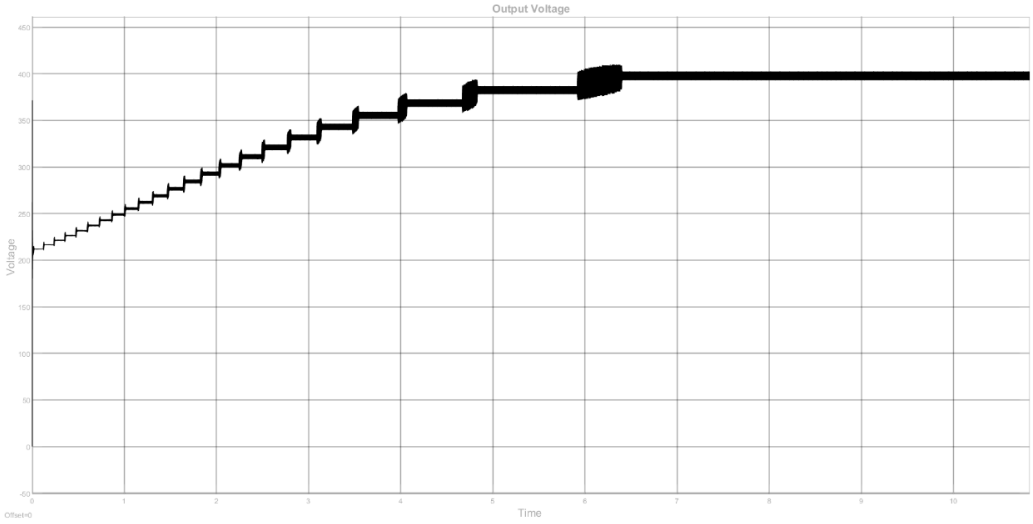

Fig.11 Output of Boost Converter with Reference of 400 V

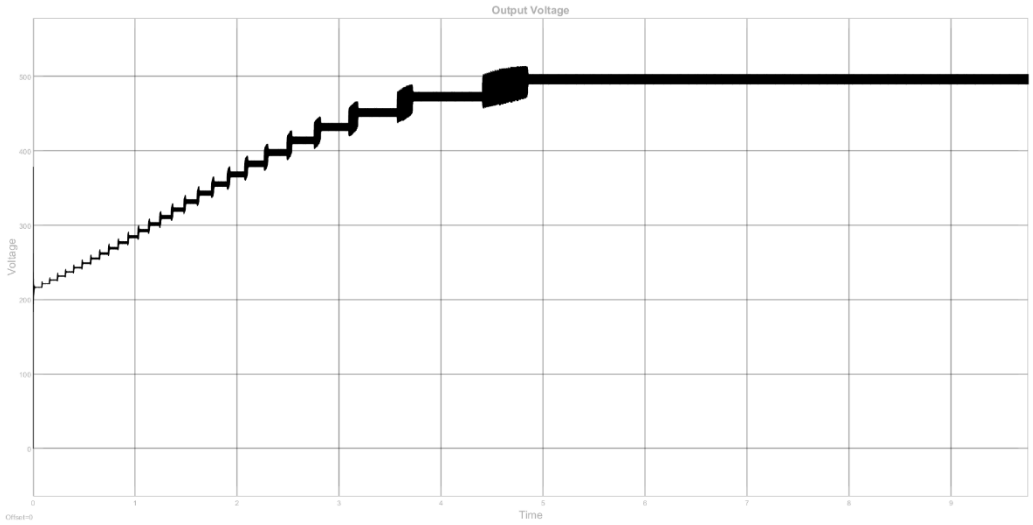

Fig.12 Output of Boost Converter with Reference of 500 V

5.2 MPPT Algorithm Simulation

5.2.1 Simulation Model

The P&O algorithm for obtaining MPP was successfully simulated in MATLAB Simulink, demonstrating stable boost converter operation. The algorithm efficiently regulated voltage based on duty cycle received through P&O algorithm, with minimal overshoot and steady-state error. The results showed stable operation of the PV array at the MPP, confirming the robustness of the control strategy.

The Model Consists of a boost converter the input to which is obtained from the Solar Array block. Standard environmental conditions (Irradiance = 1000 W/m^2 and Room temperature of 25^o Celsius) were considered for the simulation of PV array, the MOSFET is operated by the gate pulse as revived from the MPPT controller.A counter logic is also used to run the MPPT controller after a delay of 10ms, so that the values of voltage and current gets stable instead of changing continuously which can cause undesired results.

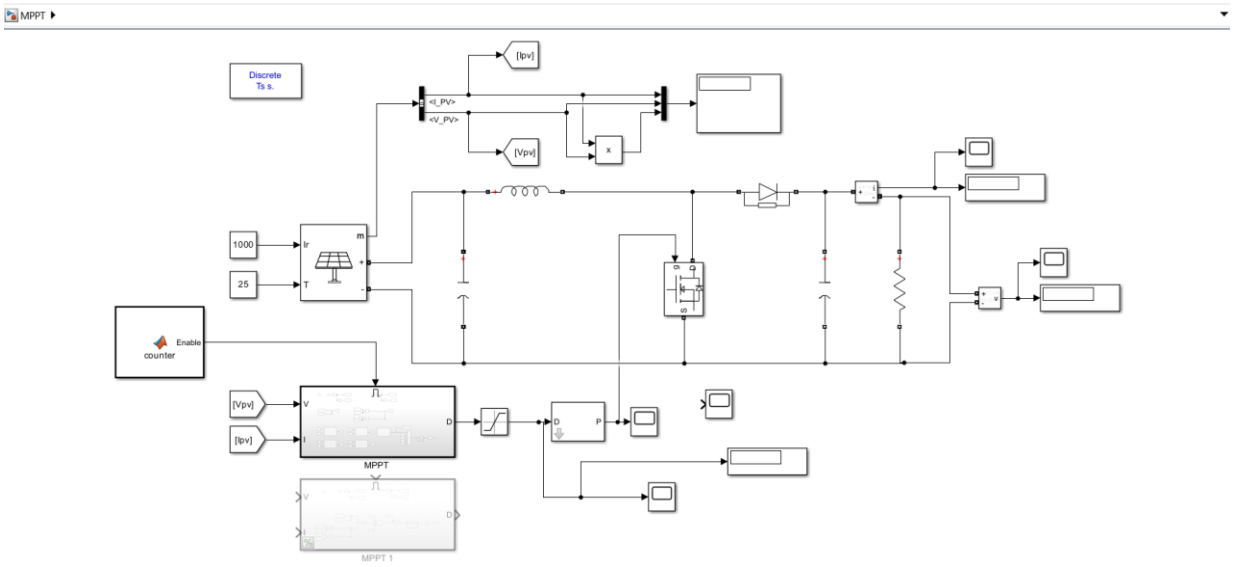

Fig.13 MATLAB Simulink Model of MPPT Controller

5.2.2 Simulation Subsystems

- **MPPT Controllers**

  The MPPT controllers are designed to perform P&O algorithm to maintain the MPP of the attached PV array, both of the MPPT subsystems perform P&O but in different ways. Input to both is voltage and current of the PV array, these values of voltage and current are passed through zero order hold and memory block to obtain Present and Past values of Voltages and Power which is then further used for determining the duty cycle for the Boost converter to maintain the MPP.

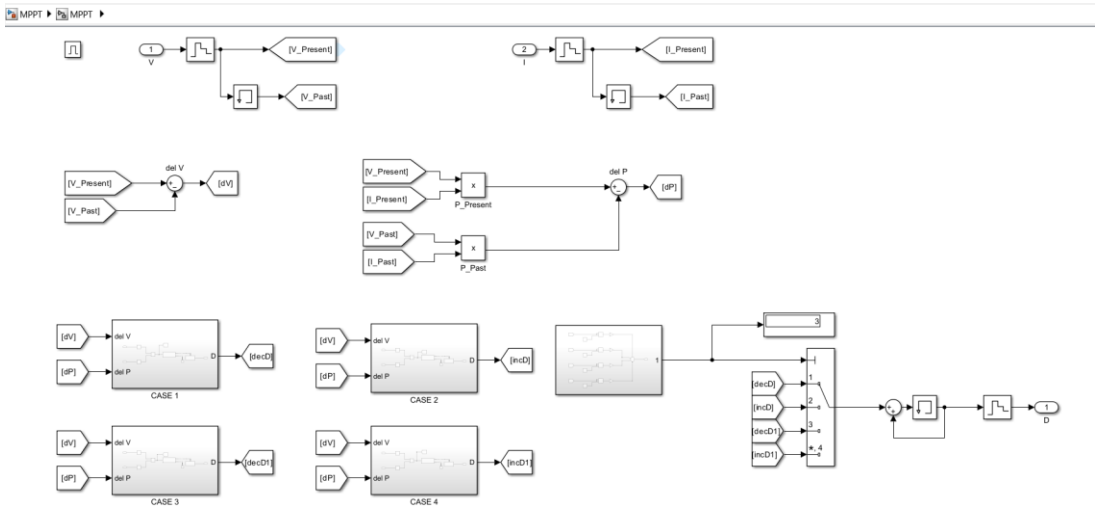

Fig.14 MPPT Controller Subsystem

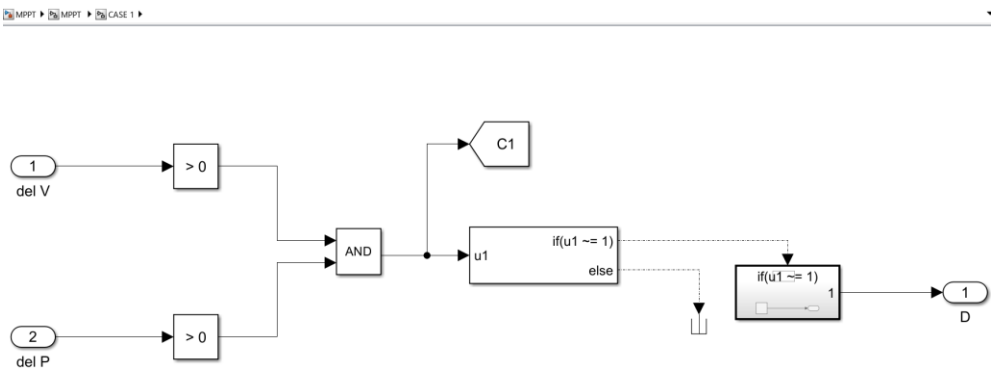

Fig.15 P&O Algorithm Case for Positive ΔV, ΔP

- **Counter Block**

  The MPPT controller need not to be operated continuously, if done so the values of voltage and power won't get a stable value for determining the next stage, to avoid it a counter is used to operate the MPPT controller at a small fixed delay such that the controller provides correct values of Duty Cycle.

MATLAB Function

```
function Enable  = counter
    persistent n
    if isempty(n)
        n = 0;
    end

    n = n + 1;
    if n >= 1000

        Enable = 1;
        n = 0;
    else

        Enable = 0;
    end
end
```

Fig.16 Counter Block Code

5.2.3 Simulation Result

- **Duty Cycle**

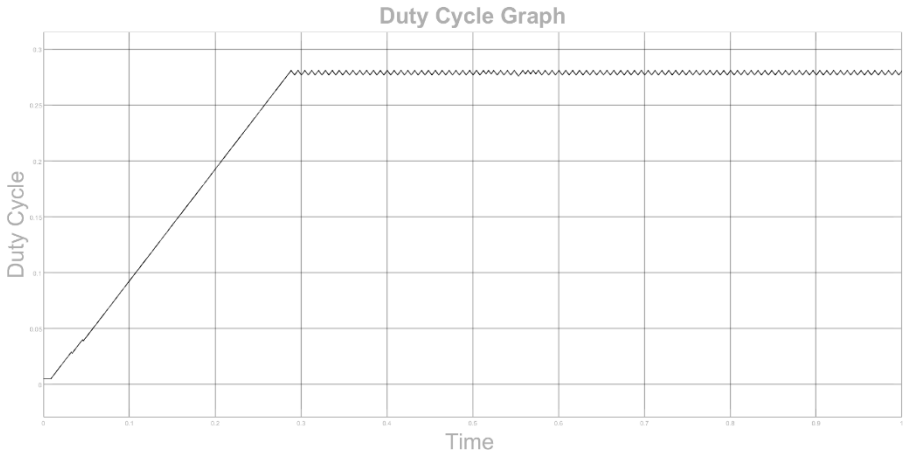

Fig.17 Duty Cycle Value as Controlled by MPPT Controller

- **Boost Converter Output**

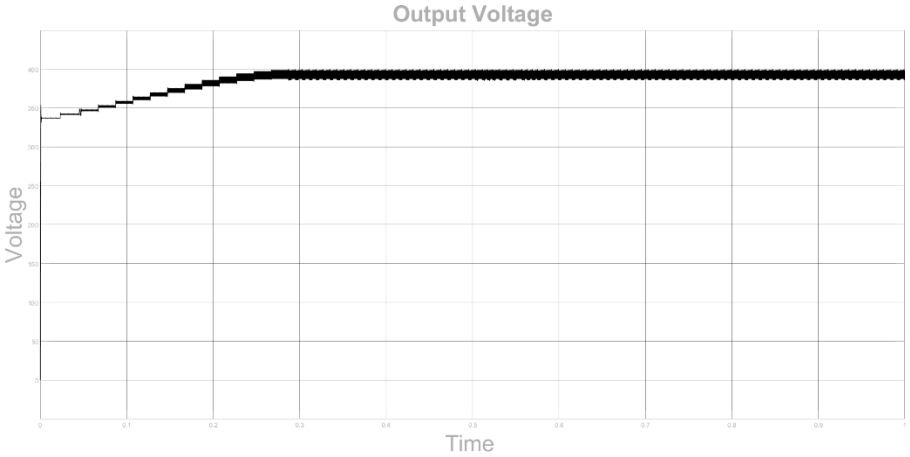

Fig.18 Output Voltage of MPPT Controlled Boost Converter

- **PV Parameters**

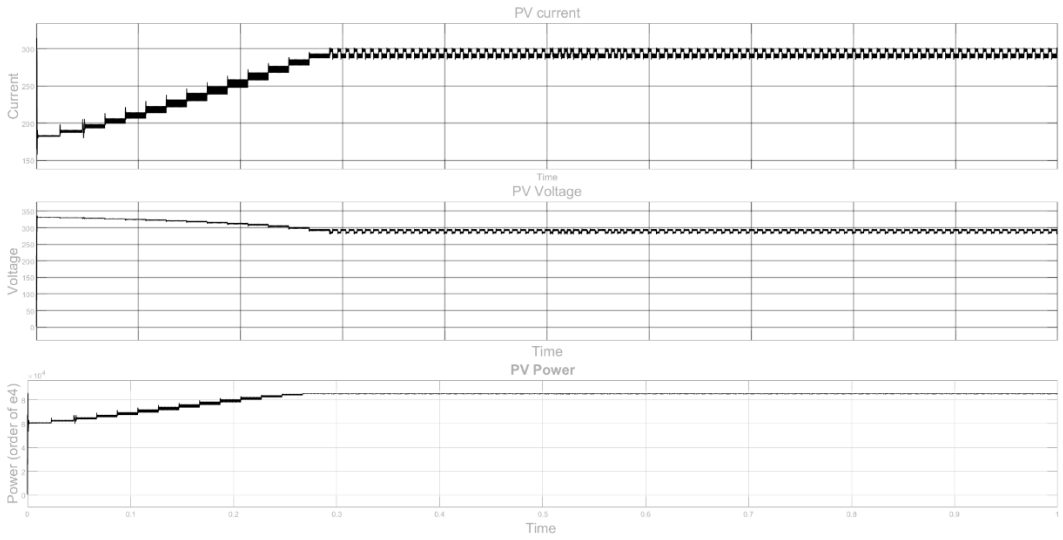

Fig.19 Voltage, Current and Power of The Solar Array at MPP

5.3 Hardware Implementation

5.3.1 FPGA Board Integration

Integration of the system involves interfacing the PolarFire SoC FPGA board with the Libero SoC Design Suite to implement real-time control of the PV system. The FPGA receives voltage and current measurements from the PV array via an external ADC (ADS1115), which are used as inputs for the MPPT control logic. Based on these inputs, the FPGA executes the P&O algorithm and generates a corresponding PWM signal to control the switching of a Boost converter MOSFET. All sensing, decision-making, and control operations are handled entirely within the FPGA fabric, enabling high-speed, deterministic operation suitable for dynamic solar environments.

- **Generating PWM:**

  For the integration process, a simple PWM was initially generated. The FPGA generated a PWM signal. This step was crucial to verify the basic functionality of the system before moving on to the MPPT algorithm testing.

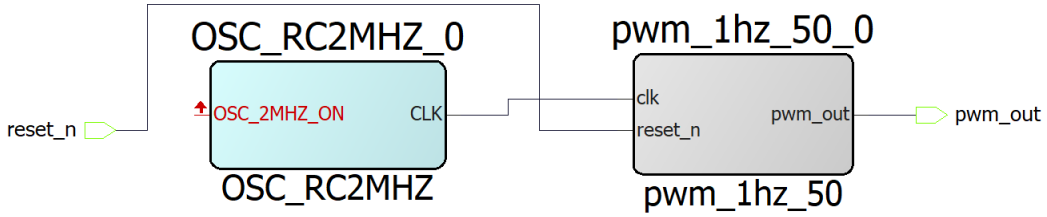

Fig.20 Libero SoC Design for PWM Generation

- **Controller Setup:**

  The Verilog-based design is developed and compiled using the Libero SoC Design Suite, which synthesizes the code into a hardware-level configuration. This synthesized design is then translated into a bitstream file that represents the internal logic and routing of the FPGA. Using Libero's built-in programmer and the on-board JTAG interface, the bitstream is uploaded to the PolarFire SoC FPGA, which then directly executes the hardware-implemented logic (such as MPPT control, PWM generation, and I²C communication) in real time, without the need for a processor or operating system.

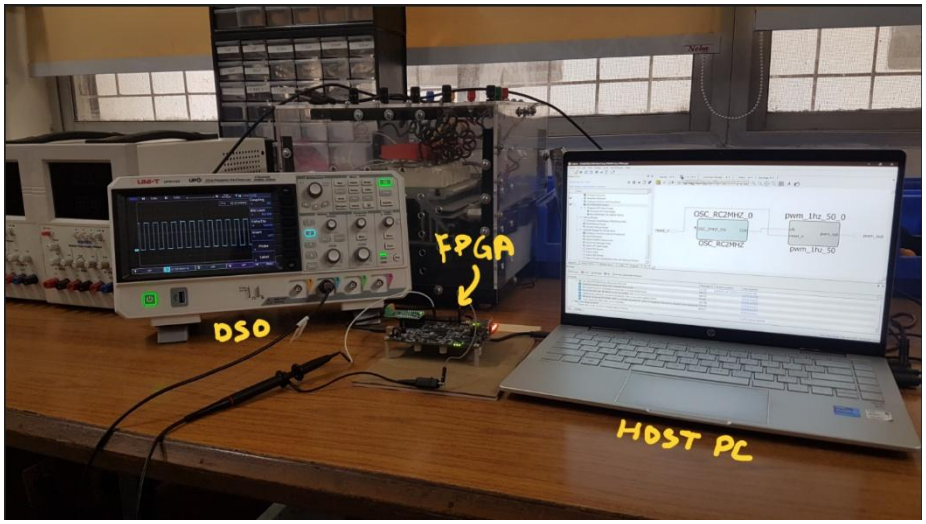

Fig.21 Polar Fire SoC Discovery Kit for PWM Generation

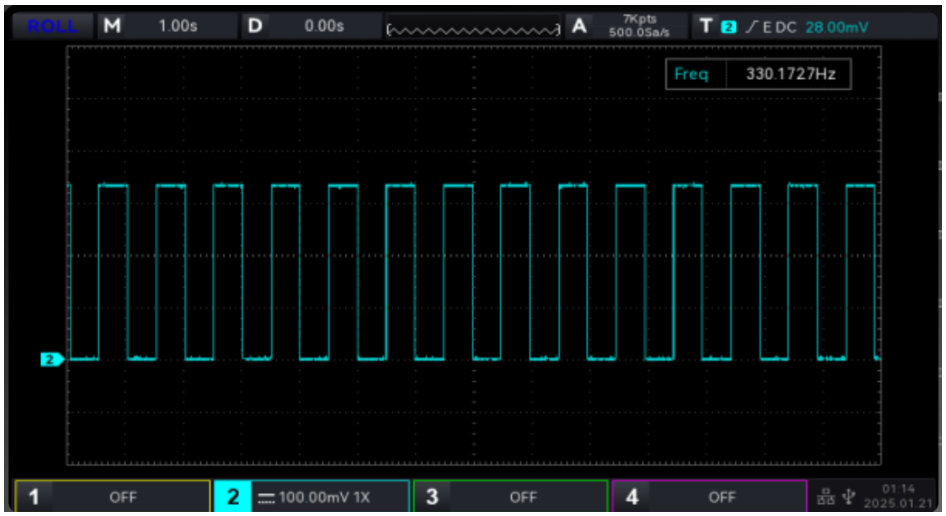

Fig.22 Output of PWM Signal on a DSO

5.3.2 Sensor Calibration

For Measuring the Values of PV voltage and current voltage and current sensor boards were calibrated using a Programable DC voltage Supply. Following are the results that were obtained.

- **Voltage Sensor:**
  - Max Input = 800 V
  - Off-Set Voltage = 1.286 V
  - Gain = 772
  - Gain = $\frac{V_{in}}{V_{out}-Offset}$

- **Current Sensor**
  - Max Input = 20 A
  - Off-Set Voltage = 1.653 V
  - Sensitivity = 0.05 V per Ampere

5.3.3 ADC Interfacing

The values obtained from the voltage and current sensor are physical values (analog signals) the FPGA boards are digital devices, so the analog values need to be converted into digital signals before feeding into the FPGA board. Hence an ADC is required.

For interfacing the ADC (ADS1115) we need to know the device address so that the controller can locate it on the I2C bus. For ADS115 there are several addresses available depending on the connection of the address pin [8].

ADDRESS PIN CONNECTION	SLAVE/ADC ADDRESS
GND	1001000
VDD	1001001
SCL	1001010
SDA	1001011

Table 1

We have our Address pin connected to the GND therefore the 7-bit address is 1001000. Along with the address we have to send an 8th bit telling the ADC about the Read (1) or Write (0) operation.

To interface the ADC, we need to first tell the ADC on which channel we will be giving the input of PV voltage and current, for doing so we first send the configuration register address (00000001) to the ADC then we send the 16-bit configuration word which sets various settings of the ADC [8].

After every byte the ADC gives an Acknowledgement bit (ACK) which acts as a conformation from the salve that the transmitted data is received.

During our interfacing process we were able to send the slave address and receive the ACK bit, but we faced issues after sending the configuration register address as we didn't receive any acknowledgement bit, which caused the connection to fail.

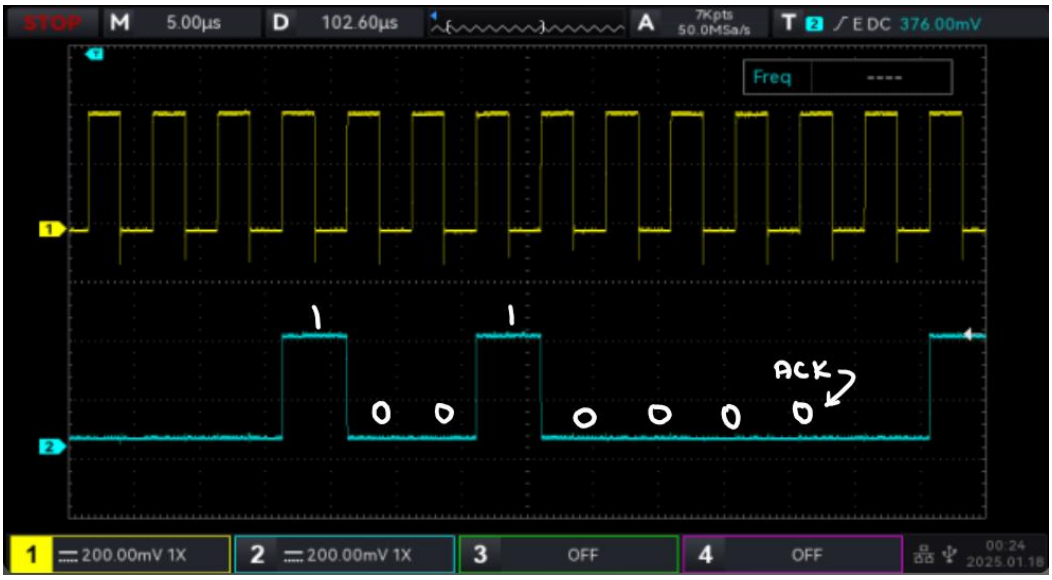

Fig.23 SCL and SDA Lines Observed on DSO During Writing the Slave Address

Chapter 6

Conclusion and Future Work

In this project, the FPGA-based solar MPPT system was developed with a focus on real-time control and data acquisition using the Microchip PolarFire SoC Discovery Kit. The Perturb and Observe MPPT algorithm was successfully simulated in MATLAB Simulink, and the FPGA was programmed to implement key components such as PWM generation and a custom I2C communication protocol to interface with the ADS1115 ADC. We successfully established communication with the ADC up to the stage of sending the slave address and receiving an acknowledgment. However, the system was unable to receive an ACK after transmitting the configuration register address, indicating an issue in the subsequent stages of the I2C write sequence.

Future development of this project would involve completing the I2C protocol to enable full communication with the ADS1115 ADC, including successful reading from the configuration and conversion registers. With reliable data acquisition in place, the next step would be to implement real-time processing of voltage and current values for dynamic MPPT control within the FPGA. Additional enhancements could include integrating UART communication for real-time monitoring, completing the control of the Boost converter using PWM, and validating the system under various simulated PV conditions. The project also opens possibilities for implementing more advanced MPPT algorithms and further optimizing the design for use in radiation-tolerant, space-grade solar energy systems.

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