INDEX

EXP.NO: 01	DESIGN AND SIMULATION OF CMOS GATES
DATE:	

AIM: To perform the functional verification of the CMOS gates through schematic entry.

FACILITIES REQUIRED AND PROCEDURE

a) Facilities required to do the experiment

S.No.	SOFTWARE REQUIREMENTS QUANTITY	
1	S-Edit, W-Edit, T-Edit using Tanner Tool.	1

b) Procedure for doing the experiment

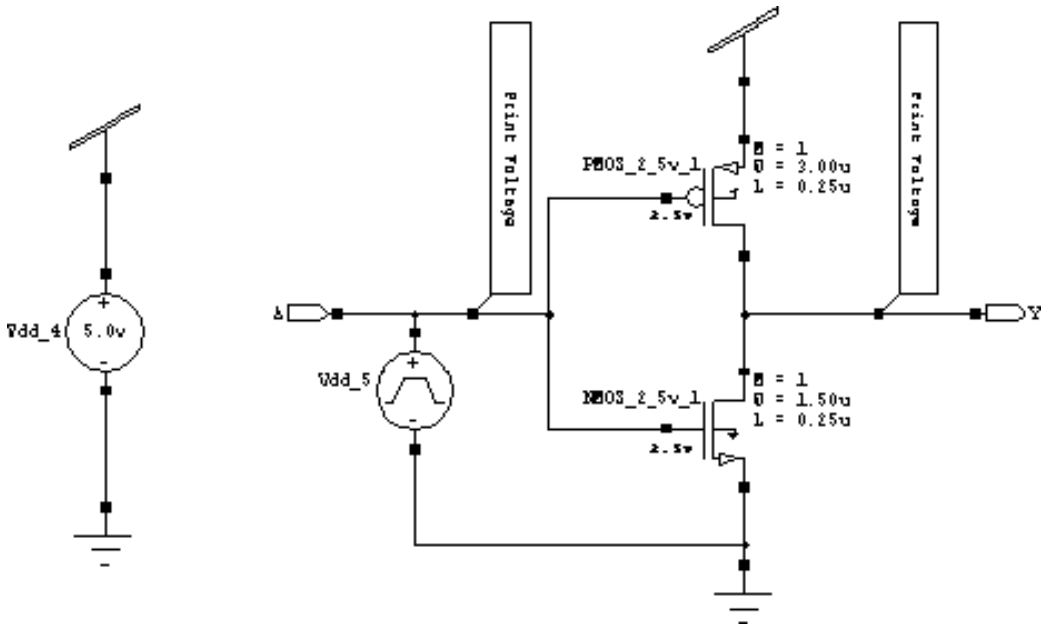
S.NO	DETAILS OF THE STEP
1	Draw the schematic of CMOS Gates using S-edit
2	Perform Transient Analysis of the CMOS Inverter
3	Obtain the output waveform from W-edit
4	Obtain the spice code using T-edit

c) THEORY: (CMOS NOT)

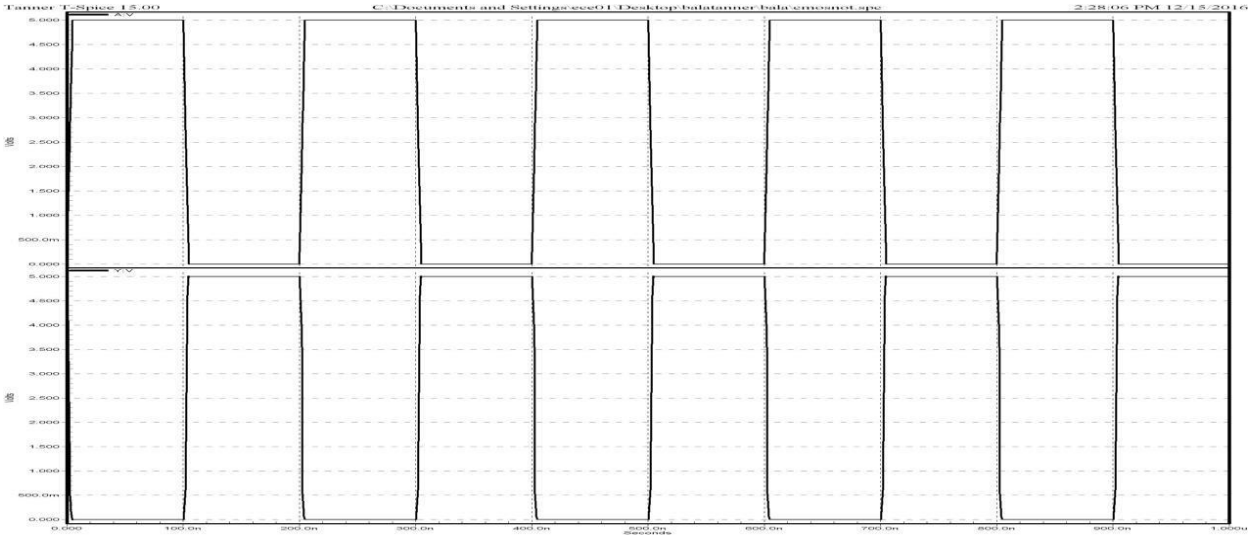
- Inverter consists of nMOS and pMOS transistors in series connected between VDD and GND.
- The gate of the two transistors are shorted and connected to the input. When the input to the inverter A =0, nMOS transistor is OFF and pMOS transistor is ON. The output is pull- up to VDD.When the input A=1, nMOS transistor is ON and pMOS transistor is OFF. The Output is Pull-down to GND.

CMOS NOT

SCHEMATIC DIAGRAM:



OUTPUT WAVEFORM:



NETLIST:

********* Simulation Settings - General Section *********

.lib "C:\Documents and Settings\ece01\My Documents\Tanner EDA\Tanner Tools v15.0\Process\Generic_250nm\Generic_250nm_Tech\Generic_250nm.lib" TT

*-------- Devices With SPICE.ORDER == 0.0 --------

***** Top Level *****

MNMOS_2_5v_1 Y A Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $
$x=4293
+$y=3300 $w=414 $h=600

MPMOS_2_5v_1 Y A Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
+$x=4293 $y=4500 $w=414 $h=600

*-------- Devices With SPICE.ORDER > 0.0 --------

VVdd_4 Vdd Gnd DC 5 $ $x=1200 $y=3800 $w=400 $h=600

VVdd_5 A Gnd PULSE(0 5 0 5n 5n 95n 200n) $ $x=2800 $y=3500 $w=400 $h=600

.PRINT TRAN V(A) $ $x=3250 $y=4650 $w=300 $h=1500 $r=270

.PRINT TRAN V(Y) $ $x=5350 $y=4650 $w=300 $h=1500 $r=270

********* Simulation Settings - Analysis Section *********

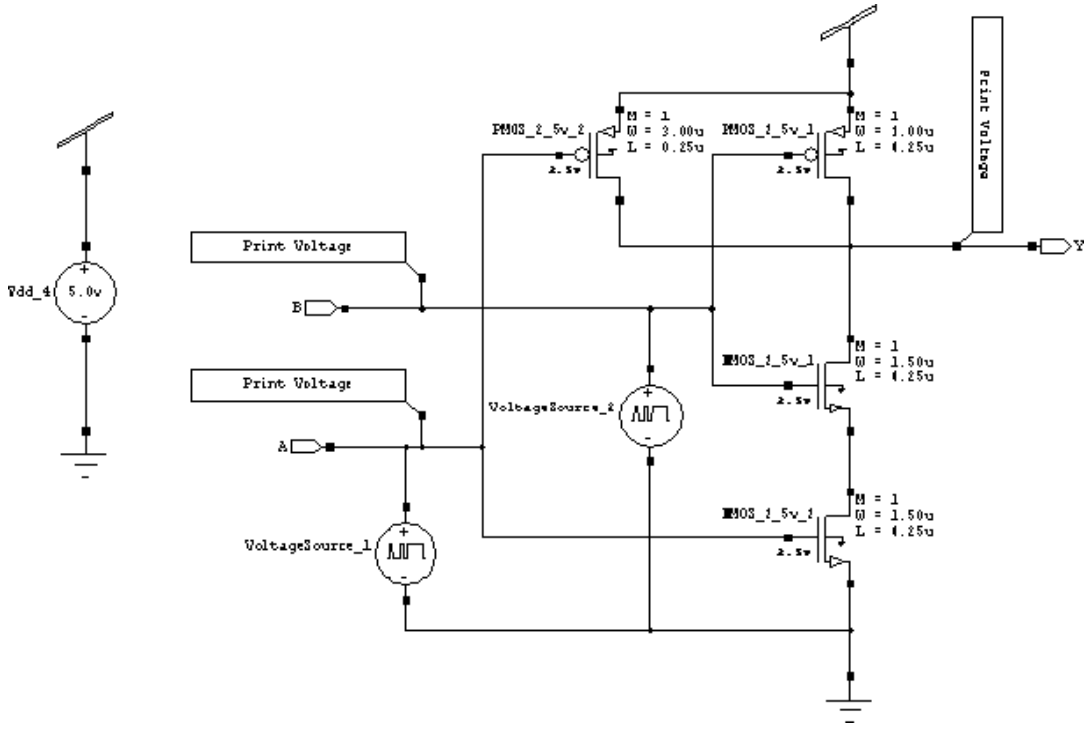
.tran 10ns 1000ns

********* Simulation Settings - Additional SPICE Commands *********

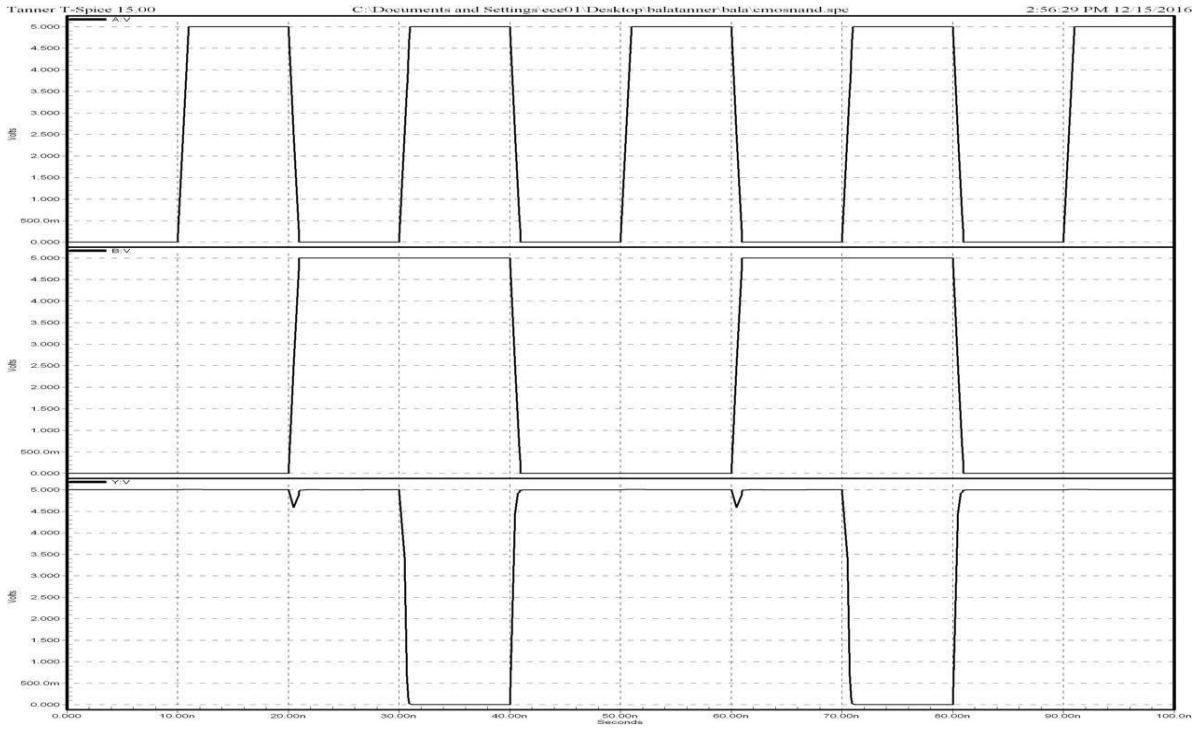
.end

CMOS NAND

SCHEMATIC DIAGRAM:



OUTPUT WAVEFORM:

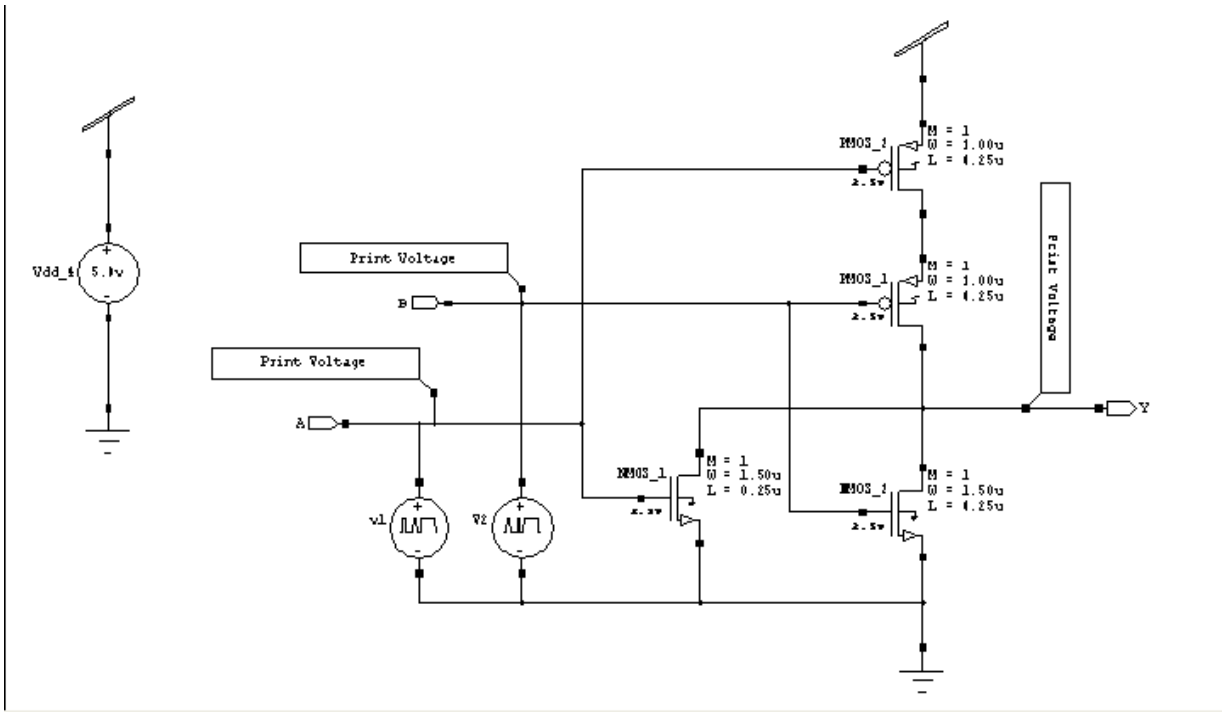


NETLIST:

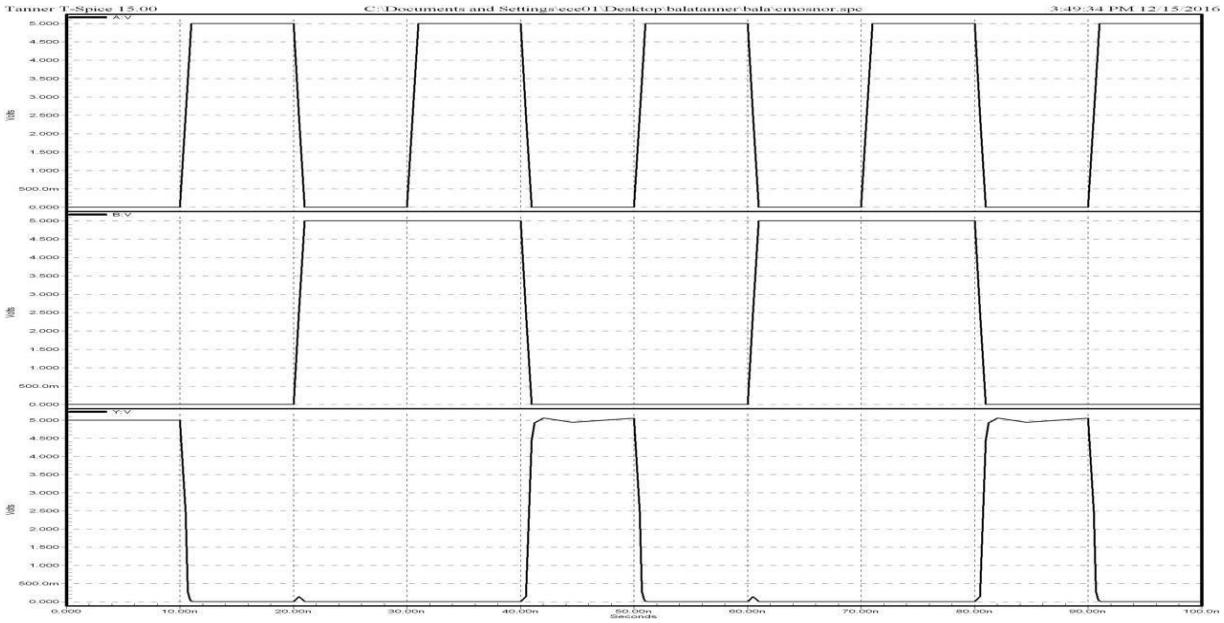
```
********* Simulation Settings - General Section *********
.lib "C:\Documents and Settings\ece01\My Documents\Tanner EDA\Tanner Tools
v15.0\Process\Generic_250nm\Generic_250nm_Tech\Generic_250nm.lib" TT

*-------- Devices With SPICE.ORDER == 0.0 --------
***** Top Level *****
MNMOS_2_5v_1 Y B N_1 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $
$x=5993
+$y=3200 $w=414 $h=600
MNMOS_2_5v_2 N_1 A Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $
+$x=5993 $y=2200 $w=414 $h=600
MPMOS_2_5v_1 Y B Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
+$x=5993 $y=4700 $w=414 $h=600
MPMOS_2_5v_2 Y A Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
+$x=4493 $y=4700 $w=414 $h=600

*-------- Devices With SPICE.ORDER > 0.0 --------
VVdd_4 Vdd Gnd DC 5 $ $x=1200 $y=3800 $w=400 $h=600
VVoltageSource_1 A Gnd BIT({0101} ) $ $x=3300 $y=2100 $w=400 $h=600
VVoltageSource_2 B Gnd BIT({0011} ) $ $x=4900 $y=3000 $w=400 $h=600
.PRINT TRAN V(A) $ $x=2650 $y=3150 $w=1500 $h=300 $r=180
.PRINT TRAN V(B) $ $x=2650 $y=4050 $w=1500 $h=300 $r=180
.PRINT TRAN V(Y) $ $x=7050 $y=4850 $w=300 $h=1500 $r=270
********* Simulation Settings - Analysis Section *********
.tran 10ns 100ns
********* Simulation Settings - Additional SPICE Commands *********
.end
```

CMOS NOR

SCHEMATIC DIAGRAM:



OUTPUT WAVEFORM:



NETLIST:

********* Simulation Settings - General Section *********
.lib "C:\Documents and Settings\ece01\My Documents\Tanner EDA\Tanner Tools v15.0\Process\Generic_250nm\Generic_250nm_Tech\Generic_250nm.lib" TT

*-------- Devices With SPICE.ORDER == 0.0 --------
***** Top Level *****
MNMOS_1 Y A Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=4493 +$y=2300 $w=414 $h=600
MNMOS_2 Y B Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=5993 +$y=2200 $w=414 $h=600
MPMOS_1 Y B N_3 Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $ $x=5993 +$y=3600 $w=414 $h=600
MPMOS_2 N_3 A Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $ $x=5993 +$y=4500 $w=414 $h=600

*-------- Devices With SPICE.ORDER > 0.0 --------
VVdd_4 Vdd Gnd DC 5 $ $x=700 $y=3800 $w=400 $h=600
Vv1 A Gnd BIT({0101}) $ $x=2800 $y=2100 $w=400 $h=600
VV2 B Gnd BIT({0011}) $ $x=3500 $y=2100 $w=400 $h=600
.PRINT TRAN V(A) $ $x=2150 $y=3150 $w=1500 $h=300 $r=180
.PRINT TRAN V(B) $ $x=2750 $y=3850 $w=1500 $h=300 $r=180
.PRINT TRAN V(Y) $ $x=7050 $y=3650 $w=300 $h=1500 $r=270

********* Simulation Settings - Analysis Section *********
.tran 10ns 100ns
********* Simulation Settings - Additional SPICE Commands *********
.end

EXP.NO: 02	DESIGN AND SIMULATION OF A CMOS INVERTER USING DIGITAL FLOW
DATE:	

AIM: To perform the functional verification of a CMOS inverter circuit through schematic entry.

FACILITIES REQUIRED AND PROCEDURE

a) Facilities required to do the experiment

S.No.	SOFTWARE REQUIREMENTS QUANTITY	
1	S-Edit, W-Edit, T-Edit using Tanner Tool.	1

b) Procedure for doing the experiment

S.NO	DETAILS OF THE STEP
1	Draw the schematic of CMOS inverter using S-edit
2	Perform Transient Analysis of CMOS inverter circuit
3	Obtain the spice code using T-edit
4	Obtain the output waveform from W-edit

c) THEORY:

The term CMOS stands for "Complementary Metal Oxide Semiconductor". CMOS technology is one of the most popular technologies in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications. Today's computer memories, CPUs and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices.

One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application specific integrated circuits (ASICs).

NETLIST:

```
* SPICE export by: SEDIT 13.12
* Export time:      Wed Dec 11 11:43:07 2019
* Design:          adm705-1
* Cell:            Cell3
* View:            view0
* Export as:       top- level cell
* Export mode:      hierarchical
* Exclude .model: no
* Exclude .end:     no
* Expand paths:     yes
* Wrap lines:       no
* Root path:       C:\Documents and Settings\Administrator\Desktop\adm705-1
* Exclude global pins: no
* Control property name: SPICE
********* Simulation Settings - General section *********
.lib "C:\Documents and Settings\Administrator\My Documents\Tanner EDA\Tanner Tools
v13.1\Libraries\Models\Generic_025.lib" TT
********* Simulation Settings - Parameters and SPICE Options *********
*-------- Devices: SPICE.ORDER > 0 --------
MNMOS_1 Out N_2 Gnd N_1 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_1 Out N_2 Vdd N_3 PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
VVoltageSource_1 Vdd Gnd DC 5
VVoltageSource_2 N_2 Gnd PULSE(0 5 0 5n 5n 95 n 200n)
.PRINT TRAN V(Out)
```

```
.PRINT TRAN V(N_2)


********* Simulation Settings - Analysis section *********

.tran 350ns 500ns

.dc lin source VVoltageSource_1 0 5 0.5

.print dc v(MNMOS_1,Gnd)


********* Simulation Settings - Additional SPICE commands *********

.end
```

EXP.NO: 03	DESIGN AND SIMULATION OF 4-BIT COUNTER
DATE:	

AIM: To perform the functional verification of the 4-bit counter circuit through schematic entry.

FACILITIES REQUIRED AND PROCEDURE

a) Facilities required for doing the experiment

S.No.	SOFTWARE REQUIREMENTS QUANTITY	
1	S-Edit, W-Edit, T-Edit using Tanner Tool.	1

b) Procedure for doing the experiment

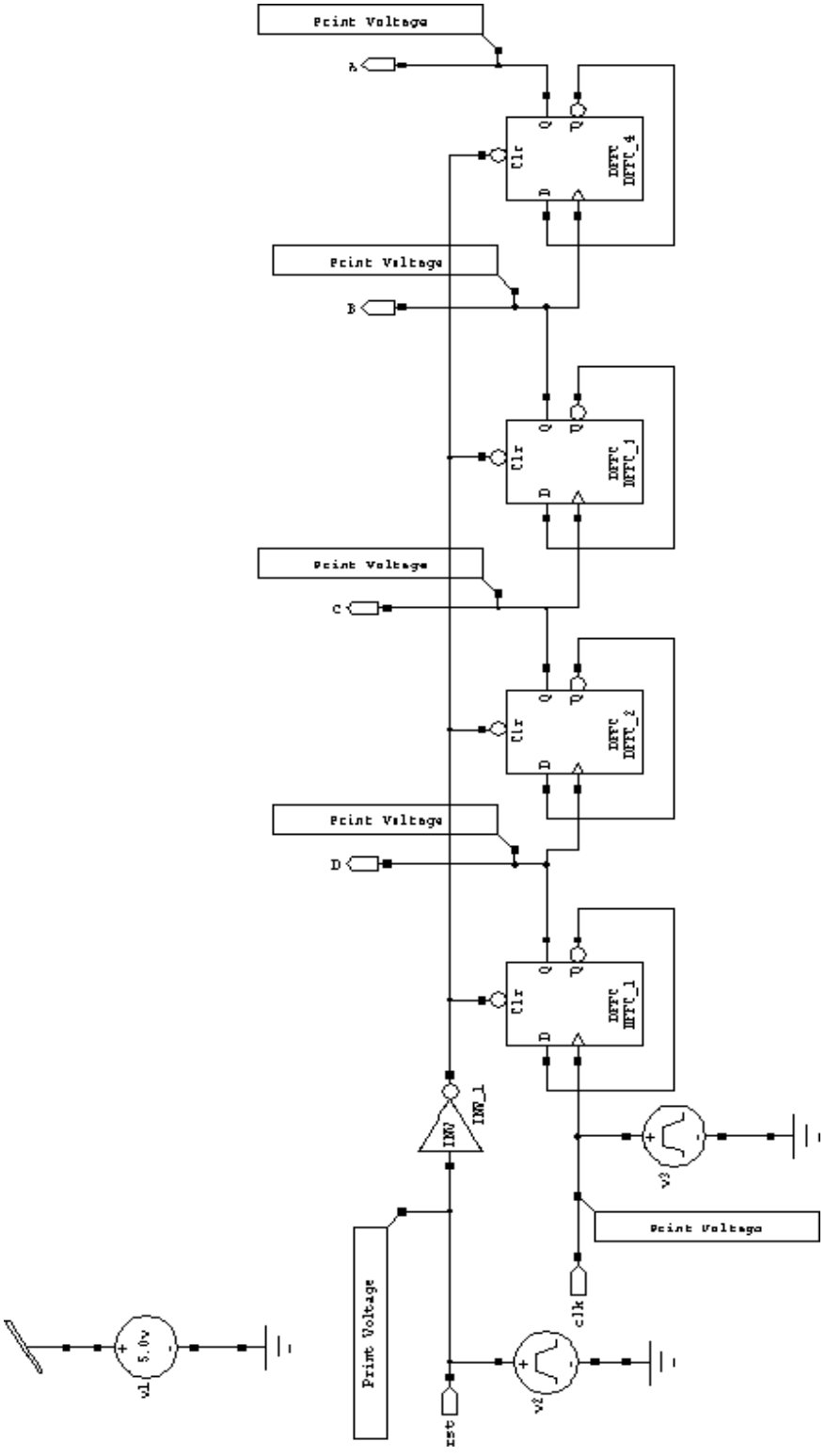
S.NO	DETAILS OF THE STEP
1	Draw the schematic of 4-bit counter using S-edit
2	Perform Transient Analysis of the 4-bit counter
3	Obtain the spice code using T-edit
4	Obtain the output wave form from W-edit

c) THEORY: (COUNTER)

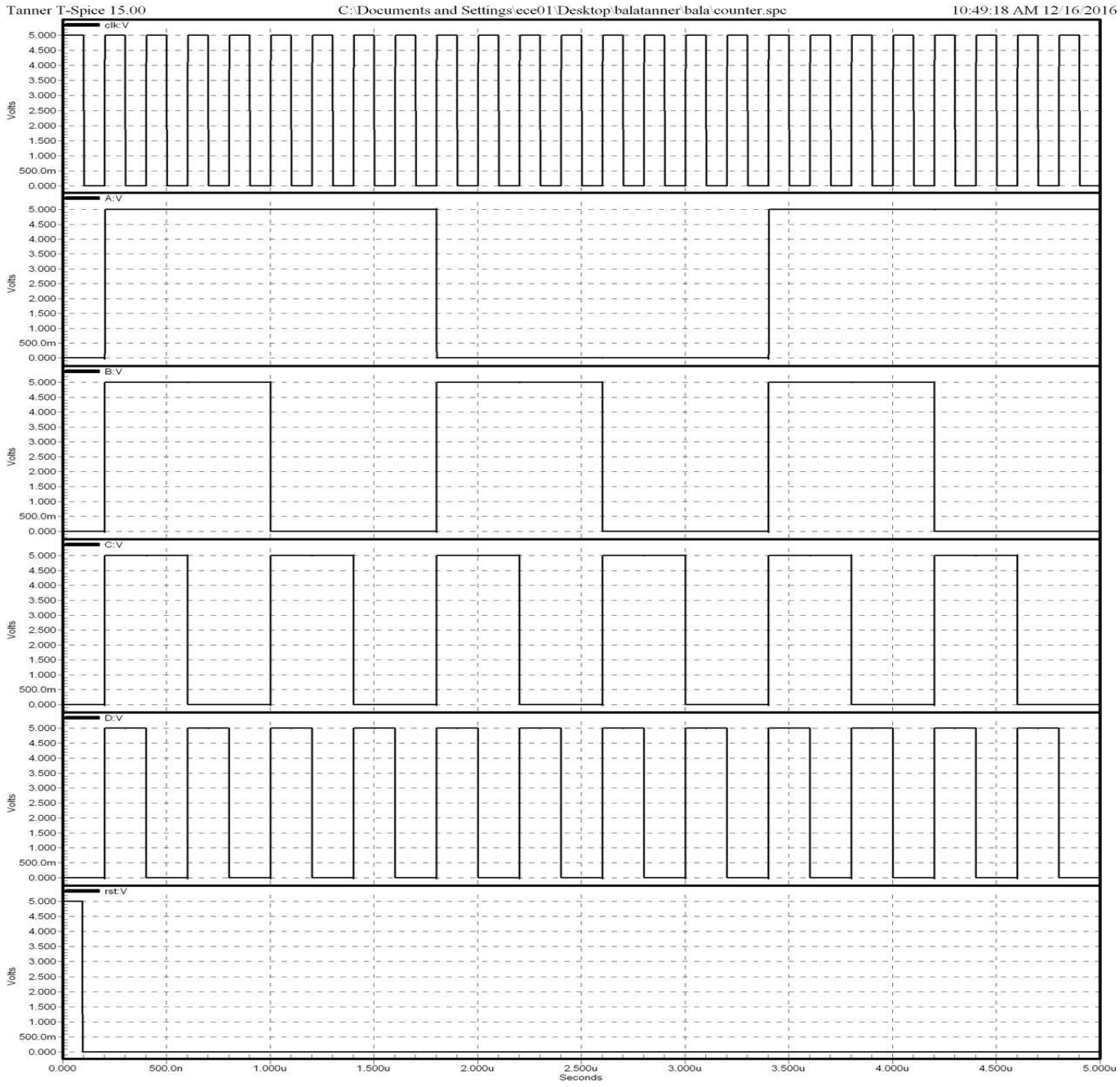
A counter that can change state in either direction, under the control of an up or down selector input, is known as an up/down counter. When the selector is in the up state, the counter increments its value. When the selector is in the down state, the counter decrements the count. Likewise the counter counts in both the directions continuously until attaining the end of the count. The count is initiated by the positive clock pulse. The counter counts from 0000 to 1111 for up count and 1111 to 0000 for down count.

4-BIT COUNTER

SCHEMATIC DIAGRAM:



OUTPUT WAVEFORM:



NETLIST:

```
********* Simulation Settings - General Section *********
.lib "C:\Documents and Settings\ece01\My Documents\Tanner EDA\Tanner Tools
v15.0\Process\Generic_250nm\Generic_250nm_Tech\Generic_250nm.lib" TT
*************** Subcircuits ******************
.subckt DFFC Clk Clr Data Q QB Gnd Vdd
*-------- Devices With SPICE.ORDER < 0.0 --------
* Design: Generic_250nm_LogicGates / Cell: DFFC / View: Main / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: D Flip-Flop with Clear
* Date: 10/15/2008 12:04:43 PM
* Revision: 144 $ $x=7600 $y=600 $w=3600 $h=1200
* Design: Generic_250nm_LogicGates / Cell: DFFC / View: Main / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: D Flip-Flop with Clear
* Date: 10/15/2008 12:04:43 PM
* Revision: 144 $ $x=7600 $y=600 $w=3600 $h=1200

*-------- Devices With SPICE.ORDER == 0.0 --------
MM1p CB Clk Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=1293
+$y=1800 $w=414 $h=600
MM2n CB Clk Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=1293
+$y=1000 $w=414 $h=600
MM3p C CB Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $ $x=2693
+$y=1800 $w=414 $h=600
MM4n C CB Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=2693
$y=1000
+$w=414 $h=600
MM5p 3 Data Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=3993
+$y=5600 $w=414 $h=600
MM6p 4 C 3 Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $ $x=3993
+$y=4700 $w=414 $h=600
MM7n 4 CB 5 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=3993
$y=3900
+$w=414 $h=600
MM8n 5 Data Gnd 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=3993
+$y=3100 $w=414 $h=600
MM9p 6 10 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=5693
+$y=5600 $w=414 $h=600
MM10p 4 CB 6 Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $ $x=6107
+$y=4700 $w=414 $h=600 $m
MM11n 4 C 7 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=5693
$y=3900
+$w=414 $h=600
MM12n 7 10 8 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=5693
$y=3100
```

```
+$w=414 $h=600
MM13n 8 Clr Gnd 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=5693
+$y=2300 $w=414 $h=600
MM14p 9 Clr Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=7293
+$y=5600 $w=414 $h=600
MM15p 4 CB 9 Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $ $x=7293
+$y=4700 $w=414 $h=600
MM16p 10 4 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=7193
+$y=3400 $w=414 $h=600
MM17n 10 4 Gnd 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=7193
+$y=2600 $w=414 $h=600
MM18p 11 10 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=1393
+$y=5200 $w=414 $h=600
MM19p 12 CB 11 Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=1393
+$y=4400 $w=414 $h=600
MM20An 12 Clr 15 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=1393
+$y=3600 $w=414 $h=600
MM20n 15 C 13 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=1393
+$y=2800 $w=414 $h=600
MM21n 13 10 Gnd 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=1393
+$y=2000 $w=414 $h=600
MM22p 17 Clr Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=3093
+$y=5200 $w=414 $h=600
MM23p 12 C 17 Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=3093
+$y=4400 $w=414 $h=600
MM24n 12 CB 17 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=3093
+$y=3600 $w=414 $h=600
MM25Ap Q 17 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=5293
+$y=4400 $w=414 $h=600
MM25p 17 16 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=4493
+$y=5200 $w=414 $h=600
MM26An Q 17 Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=5293
+$y=3600 $w=414 $h=600
MM26n 17 Clr 14 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=4493
+$y=2800 $w=414 $h=600
MM27n 14 16 Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3 u $ $x=4493
+$y=2000 $w=414 $h=600
MM28Ap QB 16 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=8193
+$y=4300 $w=414 $h=600
MM28p 16 12 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=6693
+$y=4400 $w=414 $h=600
```

```
MM29An QB 16 Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $
$x=8193
+$y=3500 $w=414 $h=600
MM29n 16 12 Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=6693
+$y=3600 $w=414 $h=600
.ends
.subckt INV A Out Gnd Vdd
*-------- Devices With SPICE.ORDER < 0.0 --------
* Design: Generic_250nm_LogicGates / Cell: INV / View: Main / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: Inverter
* Date: 5/30/2008 4:06:39 PM
* Revision: 13 $ $x=7600 $y=600 $w=3600 $h=1200
*-------- Devices With SPICE.ORDER == 0.0 --------
MM1n Out A Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=4593
+$y=2600 $w=414 $h=600
MM2p Out A Vdd Vdd PMOS25 W=3u L=250n M=2 AS=1.125p PS=3.75u AD=1.95p PD=7.3u $
+$x=4593 $y=3600 $w=414 $h=600
.ends

*-------- Devices With SPICE.ORDER == 0.0 --------
***** Top Level *****
XDFFC_1 clk N_1 N_2 D N_2 Gnd Vdd DFFC $ $x=3100 $y=3400 $w=800 $h=1000
XDFFC_2 D N_1 N_4 C N_4 Gnd Vdd DFFC $ $x=4900 $y=3400 $w=800 $h=1000
XDFFC_3 C N_1 N_5 B N_5 Gnd Vdd DFFC $ $x=6700 $y=3400 $w=800 $h=1000
XDFFC_4 B N_1 N_6 A N_6 Gnd Vdd DFFC $ $x=8700 $y=3400 $w=800 $h=1000
XINV_1 rst N_1 Gnd Vdd INV $ $x=2300 $y=4100 $w=600 $h=400

*-------- Devices With SPICE.ORDER > 0.0 --------
Vv1 Vdd Gnd DC 5 $ $x=800 $y=6000 $w=400 $h=600
Vv2 rst Gnd PULSE(0 5 0 1n 1n 95n 10u) $ $x=700 $y=3500 $w=400 $h=600
Vv3 clk Gnd PULSE(0 5 0 5n 5n 95n 200n) $ $x=2200 $y=2700 $w=400 $h=600
.PRINT TRAN V(A) $ $x=9550 $y=4550 $w=300 $h=1500 $r=270
.PRINT TRAN V(B) $ $x=7950 $y=4450 $w=300 $h=1500 $r=270
.PRINT TRAN V(C) $ $x=5950 $y=4550 $w=300 $h=1500 $r=270
.PRINT TRAN V(clk) $ $x=1650 $y=2550 $w=300 $h=1500 $r=90
.PRINT TRAN V(D) $ $x=4250 $y=4450 $w=300 $h=1500 $r=270
.PRINT TRAN V(rst) $ $x=950 $y=4550 $w=1500 $h=300 $r=180
********* Simulation Settings - Analysis Section *********
.tran 1u 5u
********* Simulation Settings - Additional SPICE Commands *********
.end
```

EXP.NO: 04	LAYOUT CMOS INVERTOR
DATE:	

AIM: To draw the layout of CMOS Inverter using L-Edit and extract the SPICE code.

FACILITIES REQUIRED AND PROCEDURE

a) Facilities required to do the experiment

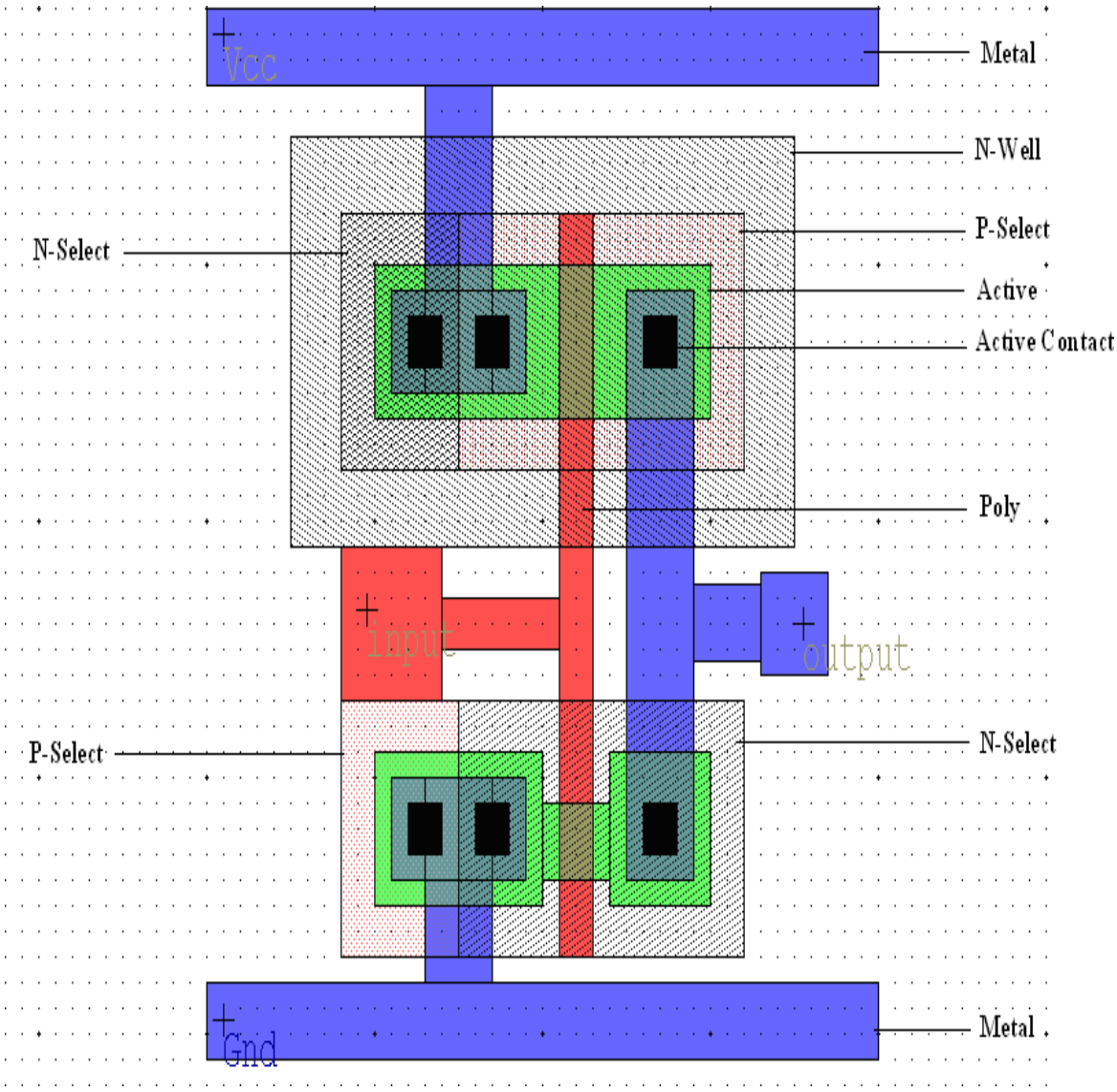
S.No.	SOFTWARE REQUIREMENTS QUANTITY	
1	L-Edit using Tanner Tool.	1

b) Procedure for doing the experiment

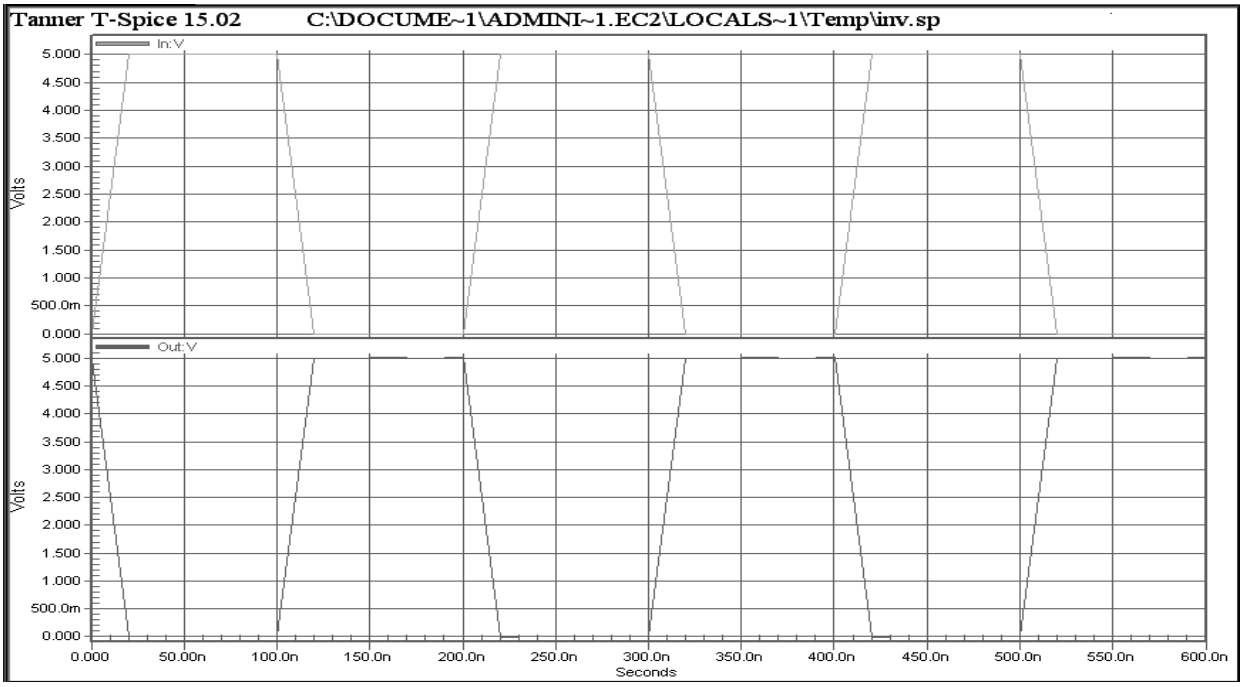
S.NO	DETAILS OF THE STEP
1	Draw the CMOS Inverter layout by obeying the Lambda Rules using L-edit.
2	i.Poly- 2λ ii.Activecontact-2λ iii. ActiveContact–Metal-1λ iv. ActiveContact–Activeregion-2λ v. ActiveRegion–Pselect-3λ vi.Pselect–nWell-3λ
3	Check DRC to verify whether any region violate the Lambda rule
4	Setup the extraction and extract the spice code using T-spice.

CMOS INVERTER:

LAYOUT DAIGRAM:



OUTPUT WAVEFORM:



EXP.NO: 05	AUTOMATIC LAYOUT GENERATION
DATE:	

AIM: To generate the automatic Layout from the schematic using the Tanner tool and verify the layout using simulation.

FACILITIES REQUIRED AND PROCEDURE

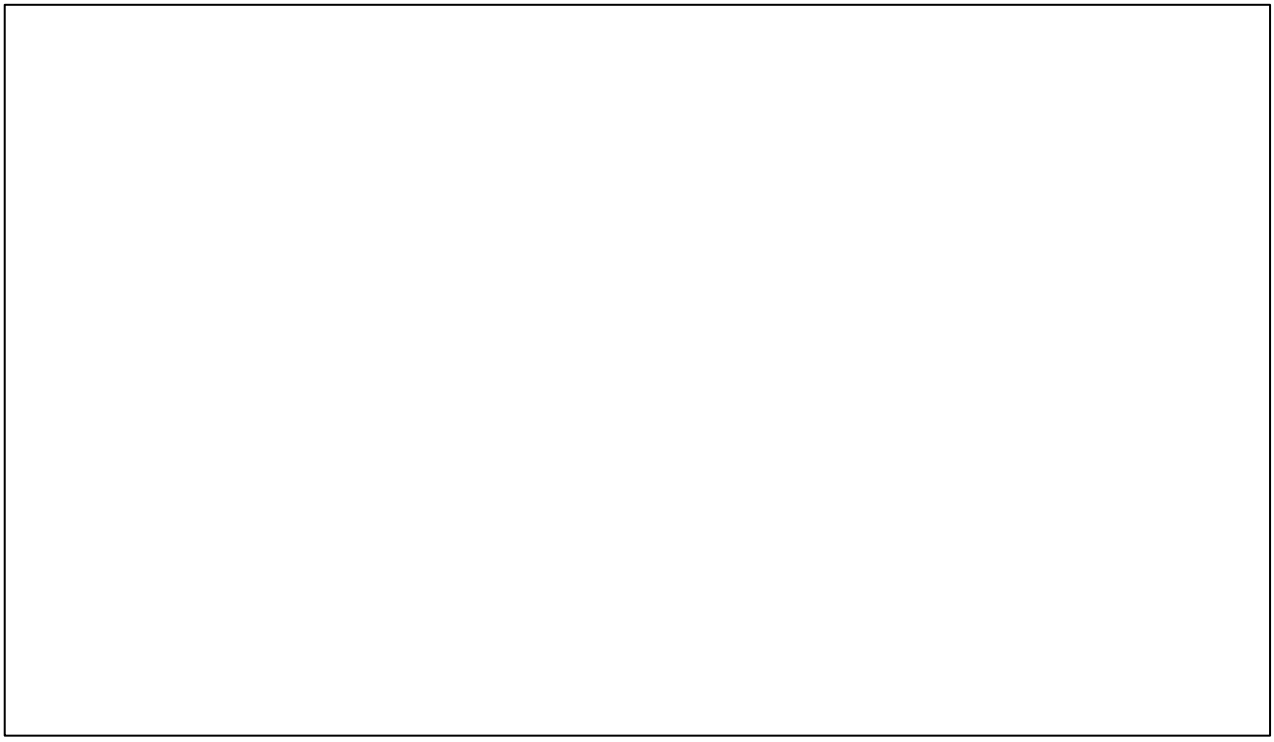
a) Facilities required to do the experiment

S.No.	SOFTWARE REQUIREMENTS QUANTITY	
1	S-Edit,L-Edit using Tanner Tool	1

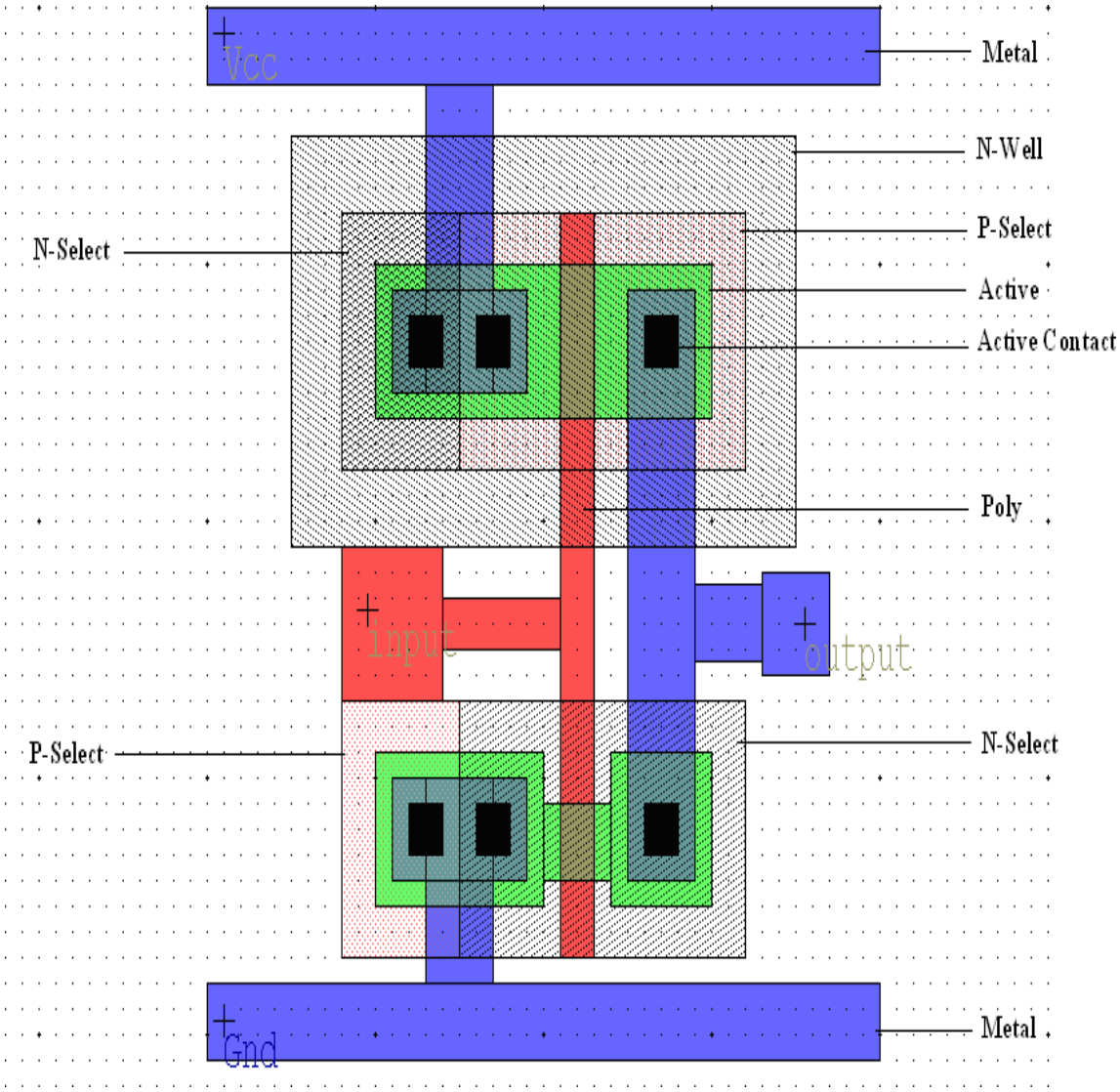
b) Procedure for doing the experiment

S.NO	DETAILS OF THE STEP
1	Draw the schematic using S -Edit and verify the output in W-Edit.
2	Extract the schematic and store it in another location
3	Open the L-Edit, open the design in Ring VCO
4	Create the new cell
5	Open the schematic file(.sdl) using the SDL Navigator
6	Do the necessary connections as per the design.
7	Name the ports and check the design for the DRC Rules
8	Locate the Destination file in the setup Extract window and extract the layout.
9	Include the Library and the print voltage statements in the net list which is obtained.
10	Verify the layout design using W-Edit.

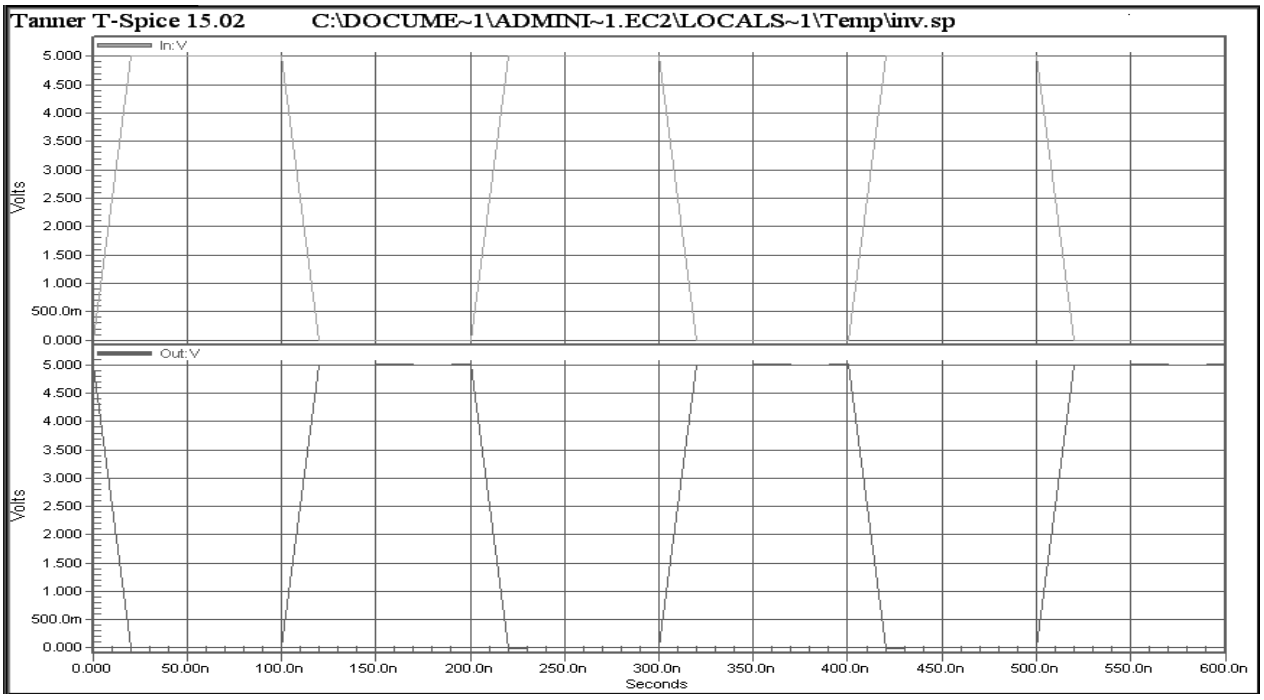
SCHEMATIC DIAGRAM:



LAYOUT GENERATION:



SIMULATED WAVEFORM:



EXP.NO: 06	DESIGN AND SIMULATE A FLIP-FLOP	
DATE:		

AIM: To perform the functional verification of a D- flip flop through schematic entry.

FACILITIES REQUIRED AND PROCEDURE

a) Facilities required to do the experiment

S.No.	SOFTWARE REQUIREMENTS QUANTITY	
1	S-Edit, W-Edit, T-Edit using Tanner Tool.	1

b) Procedure for doing the experiment

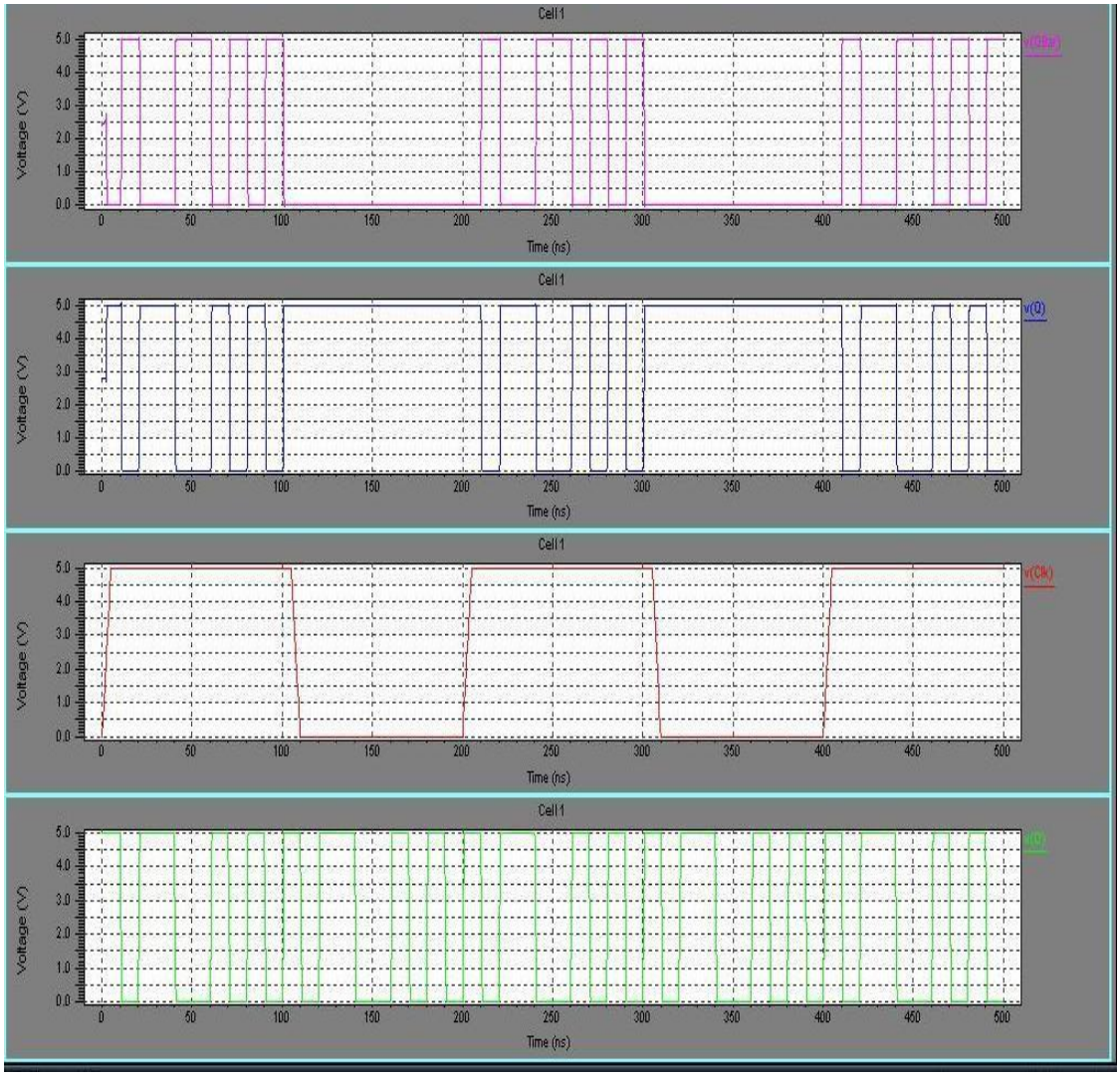
S.NO	DETAILS OF THE STEP
1	Draw the schematic of D- flipflop using S-edit
2	Perform Transient Analysis of D-flipflop
3	Obtain the spice code using T-edit
4	Obtain the output wave form from W-edit

c) THEOR Y: (D-FLIP FLOP)

The D flip- flop tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip- flop stores the value that is on the data line. It can be thought of as a basic memory cell. A D flip- flop can be made from a set/reset flip- flop by tying the set to the reset through an inverter. The result may be clocked.

SCHEMATIC ENTRY:

OUTPUT WAVEFORM:



NETLIST:

Circuit Extracted by Tanner Research's L-Edit Version 13.00 / Extract Version 13.00 ;

* TDB File: Layout1

* Cell: Core Version 1.01

* Extract Definition File: lights.ext

* Extract Date and Time: 12/12/2019 - 09:47

.include lights.md

* NODE NAME ALIASES

* 1 = U1/NAND2C_5/O ut2 (78 , 54)

* 2 = U1/NAND2C_4/O ut2 (44 , 54)

* 3 = U1/NAND2C_3/O ut2 (10 , 54)

* 6 = q (100 , 12.5)

* 6 = U1/NAND2C_3/O ut1 (2 , 52)

* 6 = U1/NAND2C_4/A (20 , 70)

* 7 = Vdd (-101 , 4)

* 7 = U1/NAND2C_1/Vdd (-51 , 86)

* 7 = U1/NAND2C_2/Vdd (-17 , 86)

* 7 = U1/NAND2C_3/Vdd (-17 , 86)

* 7 = U1/NAND2C_4/Vdd (51 , 86)

* 7 = U1/NAND2C_5/Vdd (85 , 86)

* 8 = d (-101 , 106.5)

* 8 = U1/NAND2C_1/A (-82 , 70)

* 8 = U1/NAND2C_5/A (54 , 70)

* 8 = U1/NAND2C_5/B (62 , 63)

* 9 = U1/NAND2C_1/O ut1 (-66 , 52)

* 9 = U1/NAND2C_3/A (-14 , 70)

* 10 = U1/NAND2C_2/O ut1 (-32 , 52)

* 10 = U1/NAND2C_4/B (28 , 63)

```
*       11 = U1/NAND2C_2/B (-40 , 63)
*       11 = U1/NAND2C_5/O ut1 (70 , 52)
*       12 = clk (-101 , 4.5)
*       12 = U1/NAND2C_1/B (-74 , 63)
*       12 = U1/NAND2C_2/A (-48 , 70)
*       13 = U1/NAND2C_2/O ut2 (-24 , 54)
*       14 = U1/NAND2C_1/O ut2 (-58 , 54)
*       17 = Gnd (92 , 4)
*       17 = U1/NAND2C_1/Gnd (-51 , 28)
*       17 = U1/NAND2C_2/Gnd (-17 , 28)
*       17 = U1/NAND2C_3/Gnd (-17 , 28)
*       17 = U1/NAND2C_4/Gnd (51 , 28)
*       17 = U1/NAND2C_5/Gnd (85 , 28)
*       18 = qbar (100 , 98.5)
*       18 = U1/NAND2C_3/B (-6 , 63)
*       18 = U1/NAND2C_4/O ut1 (36 , 52)
M1 Vdd d U1/NAND2C_2/B Vdd PMOS L=2u W=28u AD=84p PD=34u AS=84p PS=34u
M2 U1/NAND2C_2/B d Vdd Vdd PMOS L=2u W=28u AD=84p PD=34u AS=144p PS=68u
M3 U1/NAND2C_5/Out2 U1/NAND2C_2/B Vdd Vdd PMOS L=2u W=28u AD=148p PD=68u
AS=84p PS=34u
M4 Vdd U1/NAND2C_2/O ut1 qbar Vdd PMOS L=2u W=28u AD=84p PD=34u AS=84p PS=34u
M5 qbar q Vdd Vdd PMOS L=2u W=28u AD=84p PD=34u AS=144p PS=68u
M6 U1/NAND2C_4/Out2 qbar Vdd Vdd PMOS L=2u W=28u AD=148p PD=68u AS=84p PS=34u
M7 Vdd qbar q Vdd PMOS L=2u W=28u AD=84p PD=34u AS=84p PS=34u
M8 U1/NAND2C_3/Out2 q Vdd Vdd PMOS L=2u W=28u AD=148p PD=68u AS=84p PS=34u M9
Gnd d 5 Gnd NMOS L=2u W=28u AD=122p PD=47u AS=28p PS=30u
M10 5 d U1/NAN D2C_2/B Gnd NMOS L=2u W=28u AD=28p PD=30u AS=148p PS=68u
```

M11 U1/NAND2C_5/Out2 U1/NAND2C_2/B Gnd Gnd NMOS L=2u W=28u AD=148p PD=68u AS=122p PS=47u

M12 Gnd U1/NAND2C_2/O ut1 4 Gnd NMOS L=2u W=28u AD=122p PD=47u AS=28p PS=30u

M13 4 q qbar Gnd NMOS L=2u W=28u AD=28p PD=30u AS=148p PS=68u

M14 U1/NAND2C_4/Out2 qbar Gnd Gnd NMOS L=2u W=28u AD=148p PD=68u AS=122p PS=47u

M15 U1/NAND2C_3/Out2 q Gnd Gnd NMOS L=2u W=28u AD=148p PD=68u AS=122p PS=47u M16

q U1/NAN D2C_1/Out1 Vdd Vdd PMOS L=2u W=28u AD=84p PD=34u AS=144p PS=68u

M17 Vdd U1/NAND2C_2/B U1/NAND2C_2/O ut1 Vdd PMOS L=2u W=28u AD=84p PD=34u AS=84p PS=34u

M18 U1/NAND2C_2/Out1 clk Vdd Vdd PMOS L=2u W=28u AD=84p PD=34u AS=144p PS=68u

M19 U1/NAND2C_2/Out2 U1/NAND2C_2/O ut1 Vdd Vdd PMOS L=2u W=28u AD=148p PD=68u AS=84p PS=34u

M20 Vdd clk U1/N AND2C_1/Out1 Vdd PMOS L=2u W=28u AD=84p PD=34u AS=84p PS=34u

M21 U1/NAND2C_1/Out1 d Vdd Vdd PMOS L=2u W=28u AD=84p PD=34u AS=144p PS=68u

M22 U1/NAND2C_1/Out2 U1/NAND2C_1/O ut1 Vdd Vdd PMOS L=2u W=28u AD=148p PD=68u AS=84p PS=34u

M23 Gnd qbar 19 Gnd NMOS L=2u W=28u AD=122p PD=47u AS=28p PS=30u

M24 19 U1/NAN D2C_1/Out1 q Gnd NMOS L=2u W=28u AD=28p PD=30u AS=148p PS=68u

M25 Gnd U1/NAND2C_2/B 16 Gnd NMOS L=2u W=28u AD=122p PD=47u AS=28p PS=30u

M26 16 clk U1/NAND2C_2/O ut1 Gnd NMOS L=2u W=28u AD=28p PD=30u AS=148p PS=68u

M27 U1/NAND2C_2/Out2 U1/NAND2C_2/O ut1 Gnd Gnd NMOS L=2u W=28u AD=148p PD=68u AS=122p PS=47u

M28 Gnd clk 15 Gnd NMOS L=2u W=28u AD=122p PD=47u AS=28p PS=30u

M29 15 d U1/NAN D2C_1/Out1 Gnd NMOS L=2u W=28u AD=28p PD=30u AS=148p PS=68u

M30 U1/NAND2C_1/Out2 U1/NAND2C_1/O ut1 Gnd Gnd NMOS L=2u W=28u AD=148p PD=68u AS=122p PS=47u

* Total Nodes: 19

* Total Elements: 30

* Total Number of Shorted Elements not written to the SPICE file: 10

* Output Generation Elapsed Time: 0.000 sec

* Total Extract Elapsed Time: 1.875 sec

.END

EXP.NO: 07	DESIGN AND SIMULATE A CMOS INVERTING AMPLIFIER	
DATE:		

AIM: To perform the functional verification of a CMOS inverting amplifier circuit through schematic entry.

FACILITIES REQUIRED AND PROCEDURE

a) Facilities required to do the experiment

S.No.	SOFTWARE REQUIREMENTS QUANTITY	
1	S-Edit, W-Edit, T-Edit using Tanner Tool.	1

b) Procedure for doing the experiment

S.NO	DETAILS OF THE STEP
1	Draw the schematic of CMOS inverting amplifier using S-edit
2	Perform Transient Analysis of CMOS inverting amplifier circuit
3	Obtain the spice code using T-edit
4	Obtain the output waveform from W-edit

c) THEORY:

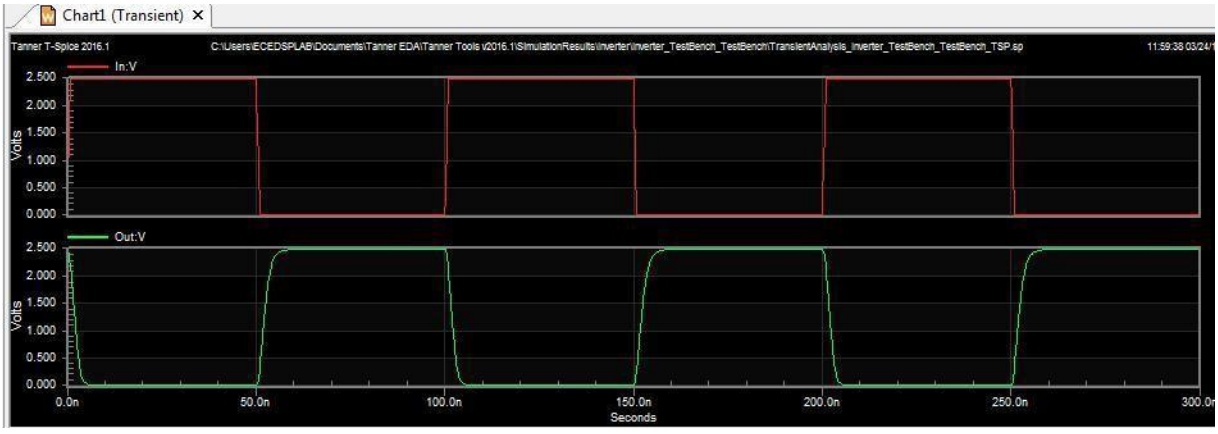
CMOS Inverter consists of nMOS and pMOS transistor in series connected between VDD and GND. The gate of the two transistors are shorted and connected to the input.

When the input to the inverter A = 0, nMOS transistor is OFF and pMOS transistor is ON. The output is pull- up to VDD.

When the input A = 1, nMOS transistor is ON and pMOS transistor is OFF. The Output is Pull-down to GND.

SCHEMATIC ENTRY:

OUTPUT WAVEFORM:



NETLIST:

SPICE export by: SEDIT 13.12

* Export time: Wed Dec 11 11:43:07 2019

* Design: adm705-1

* Cell: Cell3

* View: view0

* Export as: top- level cell

* Export mode: hierarchical

* Exclude .model: no

* Exclude .end: no

* Expand paths: yes

* Wrap lines: no

* Root path: C:\Documents and Settings\Administrator\Desktop\adm705-1

* Exclude global pins: no

* Control property name: SPICE

********* Simulation Settings - General section *********

.lib "C:\Documents and Settings\Administrator\My Documents\Tanner EDA\Tanner Tools v13.1\Libraries\Models\Generic_025.lib" TT

********* Simulation Settings - Parameters and SPICE Options *********

*-------- Devices: SPICE.ORDER > 0 --------

MNMOS_1 Out N_2 Gnd N_1 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u

MPMOS_1 Out N_2 Vdd N_3 PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u

VVoltageSource_1 Vdd Gnd DC 5

VVoltageSource_2 N_2 Gnd PULSE(0 5 0 5n 5n 95n 200n)

.PRINT TRAN V(Out)

.PRINT TRAN V(N_2)

********* Simulation Settings - Analysis section *********

```
.tran 350ns 500ns
.dc lin source VVoltageSource_1 0 5 0.5
.print dc v(MNMOS_1,Gnd)


********* Simulation Settings - Additional SPICE commands *********
.end
```

EXP.NO: 08	DESIGN AND SIMULATION OF COMMON DRAIN AMPLIFIER	
DATE:		

AIM: To perform the Design and Simulation of Common Drain amplifier circuit through schematic entry.

FACILITIES REQUIRED AND PROCEDURE

a) Facilities required to do the experiment

S.No.	SOFTWARE REQUIREMENTS QUANTITY	
1	S-Edit, W-Edit, T-Edit using Tanner Tool.	1

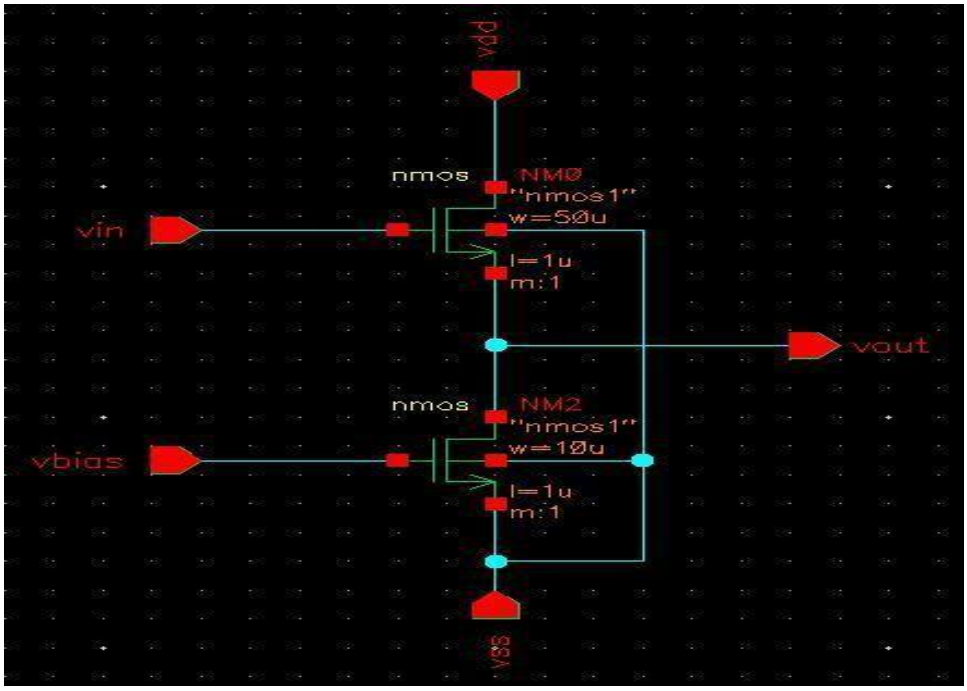
b) Procedure for doing the experiment

S.NO	DETAILS OF THE STEP
1	Draw the schematic of Common drain amplifier using S-edit
2	Perform Transient Analysis of Common drain amplifier circuit
3	Obtain the spice code using T-edit
4	Obtain the output waveform from W-edit

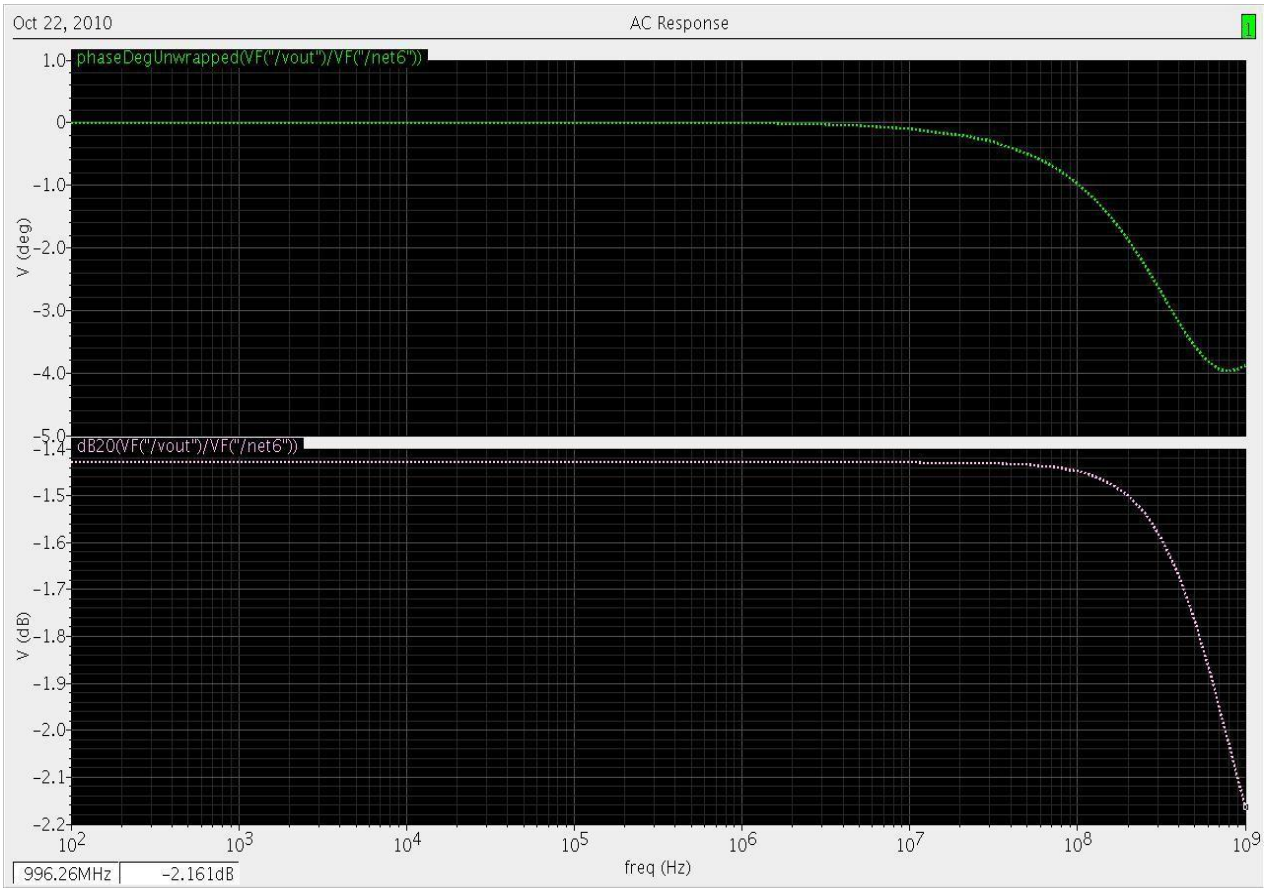
c) THEORY:

Common drain amplifier is a source follower or buffer amplifier circuit using a MOSFET. The output is simply equal to the input minus about 2.2V. The advantage of this circuit is that the MOSFET can provide current and power gain; the MOSFET draws no current from the input. It provides low output impedance to any circuit using the output of the follower, meaning that the output will not drop under load.Its output impedance is not as low as that of an emitter follower using a bipolar transistor (as you can verify by connecting a resistor from the output to -15V), but it has the advantage that the input impedance is infinite.The MOSFET is in saturation, so the current across it is determined by the gate-source voltage. Since a current source keeps the current constant, the gate-source voltage is also constant.

SCHEMATIC ENTRY:



OUTPUT WAVEFORM:



NETLIST:

```
********* Simulation Settings - General Section *********
.lib "C:\Documents and Settings\ece01\My Documents\Tanner EDA\Tanner Tools
v15.0\Process\Generic_250nm\Generic_250nm_Tech\Generic_250nm.lib" TT
*************** Subcircuits ******************
.subckt DFFC Clk Clr Data Q QB Gnd Vdd
*-------- Devices With SPICE.ORDER < 0.0 --------
* Design: Generic_250nm_LogicGates / Cell: DFFC / View: Main / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: D Flip-Flop with Clear
* Date: 10/15/2008 12:04:43 PM
* Revision: 144 $ $x=7600 $y=600 $w=3600 $h=1200
* Design: Generic_250nm_LogicGates / Cell: DFFC / View: Main / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: D Flip-Flop with Clear
* Date: 10/15/2008 12:04:43 PM
* Revision: 144 $ $x=7600 $y=600 $w=3600 $h=1200

*-------- Devices With SPICE.ORDER == 0.0 --------
MM1p CB Clk Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=1293
+$y=1800 $w=414 $h=600
MM2n CB Clk Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=1293
+$y=1000 $w=414 $h=600
MM3p C CB Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $ $x=2693
+$y=1800 $w=414 $h=600
MM4n C CB Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=2693
$y=1000
+$w=414 $h=600
MM5p 3 Data Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=3993
+$y=5600 $w=414 $h=600
MM6p 4 C 3 Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $ $x=3993
+$y=4700 $w=414 $h=600
MM7n 4 CB 5 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=3993
$y=3900
+$w=414 $h=600
MM8n 5 Data Gnd 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=3993
+$y=3100 $w=414 $h=600
MM9p 6 10 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=5693
+$y=5600 $w=414 $h=600
MM10p 4 CB 6 Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=6107
+$y=4700 $w=414 $h=600 $m
MM11n 4 C 7 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=5693
$y=3900
+$w=414 $h=600
```

```
MM12n 7 10 8 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=5693
$y=3100
+$w=414 $h=600
MM13n 8 Clr Gnd 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=5693
+$y=2300 $w=414 $h=600
MM14p 9 Clr Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=7293
+$y=5600 $w=414 $h=600
MM15p 4 CB 9 Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=7293
+$y=4700 $w=414 $h=600
MM16p 10 4 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=7193
+$y=3400 $w=414 $h=600
MM17n 10 4 Gnd 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=7193
+$y=2600 $w=414 $h=600
MM18p 11 10 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=1393
+$y=5200 $w=414 $h=600
MM19p 12 CB 11 Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=1393
+$y=4400 $w=414 $h=600
MM20An 12 Clr 15 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $
$x=1393
+$y=3600 $w=414 $h=600
MM20n 15 C 13 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=1393
+$y=2800 $w=414 $h=600
MM21n 13 10 Gnd 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=1393
+$y=2000 $w=414 $h=600
MM22p 17 Clr Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=3093
+$y=5200 $w=414 $h=600
MM23p 12 C 17 Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=3093
+$y=4400 $w=414 $h=600
MM24n 12 CB 17 0 NMOS25 W=1.50u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=3093
+$y=3600 $w=414 $h=600
MM25Ap Q 17 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=5293
+$y=4400 $w=414 $h=600
MM25p 17 16 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=4493
+$y=5200 $w=414 $h=600
MM26An Q 17 Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=5293
+$y=3600 $w=414 $h=600
MM26n 17 Clr 14 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=4493
+$y=2800 $w=414 $h=600
MM27n 14 16 Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3 u $ $x=4493
+$y=2000 $w=414 $h=600
MM28Ap QB 16 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=8193
+$y=4300 $w=414 $h=600
```

```
MM28p 16 12 Vdd Vdd PMOS25 W=3.00u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u $
$x=6693
+$y=4400 $w=414 $h=600
MM29An QB 16 Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $
$x=8193
+$y=3500 $w=414 $h=600
MM29n 16 12 Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=6693
+$y=3600 $w=414 $h=600
.ends

.subckt INV A Out Gnd Vdd
*-------- Devices With SPICE.ORDER < 0.0 --------
* Design: Generic_250nm_LogicGates / Cell: INV / View: Main / Page:
* Designed by: Tanner EDA Library Development Team
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: Inverter
* Date: 5/30/2008 4:06:39 PM
* Revision: 13 $ $x=7600 $y=600 $w=3600 $h=1200
*-------- Devices With SPICE.ORDER == 0.0 --------
MM1n Out A Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u $ $x=4593
+$y=2600 $w=414 $h=600
MM2p Out A Vdd Vdd PMOS25 W=3u L=250n M=2 AS=1.125p PS=3.75u AD=1.95p PD=7.3u $
+$x=4593 $y=3600 $w=414 $h=600
.ends

*-------- Devices With SPICE.ORDER == 0.0 --------
***** Top Level *****
XDFFC_1 clk N_1 N_2 D N_2 Gnd Vdd DFFC $ $x=3100 $y=3400 $w=800 $h=1000
XDFFC_2 D N_1 N_4 C N_4 Gnd Vdd DFFC $ $x=4900 $y=3400 $w=800 $h=1000
XDFFC_3 C N_1 N_5 B N_5 Gnd Vdd DFFC $ $x=6700 $y=3400 $w=800 $h=1000
XDFFC_4 B N_1 N_6 A N_6 Gnd Vdd DFFC $ $x=8700 $y=3400 $w=800 $h=1000
XINV_1 rst N_1 Gnd Vdd INV $ $x=2300 $y=4100 $w=600 $h=400

*-------- Devices With SPICE.ORDER > 0.0 --------
Vv1 Vdd Gnd DC 5 $ $x=800 $y=6000 $w=400 $h=600
Vv2 rst Gnd PULSE(0 5 0 1n 1n 95n 10u) $ $x=700 $y=3500 $w=400 $h=600
Vv3 clk Gnd PULSE(0 5 0 5n 5n 95n 200n) $ $x=2200 $y=2700 $w=400 $h=600
.PRINT TRAN V(A) $ $x=9550 $y=4550 $w=300 $h=1500 $r=270
.PRINT TRAN V(B) $ $x=7950 $y=4450 $w=300 $h=1500 $r=270
.PRINT TRAN V(C) $ $x=5950 $y=4550 $w=300 $h=1500 $r=270
.PRINT TRAN V(clk) $ $x=1650 $y=2550 $w=300 $h=1500 $r=90
.PRINT TRAN V(D) $ $x=4250 $y=4450 $w=300 $h=1500 $r=270
.PRINT TRAN V(rst) $ $x=950 $y=4550 $w=1500 $h=300 $r=180
********* Simulation Settings - Analysis Section *********
.tran 1u 5u
********* Simulation Settings - Additional SPICE Commands *********
.end
```

EXP.NO: 09	DESIGN AND SIMULATION OF DIFFERENTIAL AMPLIFIER	
DATE:		

AIM: To calculate the gain, bandwidth and CMRR of a differential amplifier through schematic entry using Tanner EDA tool.

FACILITIES REQUIRED AND PROCEDURE

a) Facilities required for doing the experiment

S.No.	SOFTWARE REQUIREMENTS	Quantity
1	S-Edit, W-Edit, T-Edit using Tanner Tool.	1

b) Procedure for doing the experiment

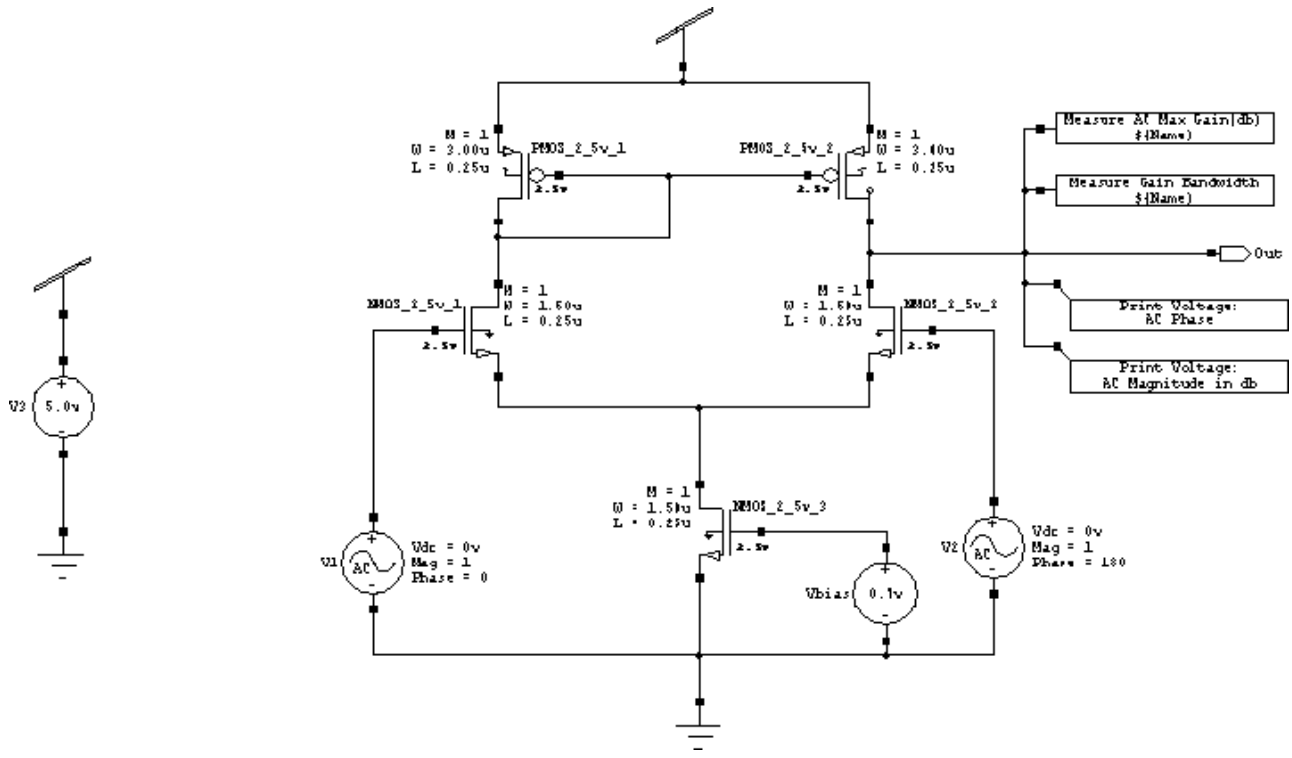
S.No	Details of the step
1	Draw the schematic of the differential amplifier using S-edit and generate the Symbol.
2	Draw the schematic of the differential amplifier circuit using the generated Symbol.
3	Perform AC Analysis of the differential amplifier.
4	Obtain the frequency response from W-edit.
5	Obtain the spice code using T-edit.

PROCEDURE:

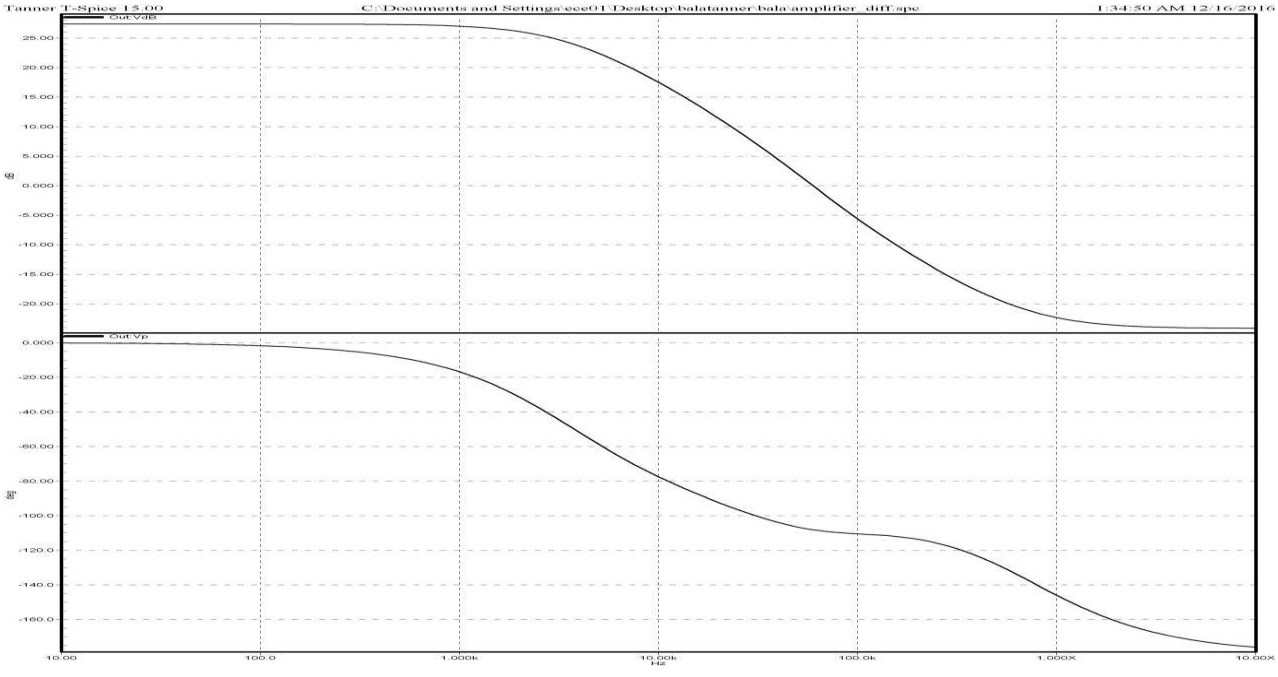
- Enter the schematic of the differential amplifier using S-Edit.
- Perform AC Analysis of the differential amplifier.
- Go to „setup‟‟in that select „spice simulation‟‟. Choose „ac analysis‟‟and give the following values.
- Set „Start frequency =10‟‟,‟‟Stop frequency=10meg‟‟, „No. of frequency=25‟‟, „Sweep type = dec‟‟. Click on „general‟‟type and give path to Generic_250nm.lib.Then Click OK.
- RUN Simulation to get output.
- Obtain the frequency response from W-Edit.
- Obtain the spice code using T-Edit.

SCHEMATICDIAGRAM:

DIFFERENTIAL MODE:



DIFFERENTIAL MODE OUTPUT:



NETLIST:

********* Simulation Settings - General Section *********

.lib "C:\Documents and Settings\ece01\My Documents\Tanner EDA\Tanner Tools v15.0\Process\Generic_250nm\Generic_250nm_Tech\Generic_250nm.lib" TT

*-------- Devices With SPICE.ORDER == 0.0 --------

***** Top Level *****

MNMOS_2_5v_1 N_1 N_3 N_4 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u

+$ $x=3793 $y=4300 $w=414 $h=600

MNMOS_2_5v_2 Out N_5 N_4 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u

+$ $x=6607 $y=4300 $w=414 $h=600 $m

MNMOS_2_5v_3 N_4 N_6 Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u

+$ $x=5507 $y=3000 $w=414 $h=600 $m

MPMOS_2_5v_1 N_1 N_1 Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u

+$ $x=4207 $y=5300 $w=414 $h=600 $m

MPMOS_2_5v_2 Out N_1 Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u

+$ $x=6193 $y=5300 $w=414 $h=600

*-------- Devices With SPICE.ORDER > 0.0 --------

VV3 Vdd Gnd DC 5 $ $x=1200 $y=3800 $w=400 $h=600

VVbias N_6 Gnd DC 700m $ $x=6500 $y=2600 $w=400 $h=600

VV1 N_3 Gnd DC 0 AC 1 0 $ $x=3200 $y=2800 $w=400 $h=600

VV2 N_5 Gnd DC 0 AC 1 180 $ $x=7200 $y=2900 $w=400 $h=600

.PRINT AC Vdb(O ut) $ $x=8350 $y=4050 $w=1500 $h=300

.PRINT AC Vp(O ut) $ $x=8350 $y=4450 $w=1500 $h=300

.MEASURE AC AC_Measure_Gain_1 MAX vdb(Out) ON $ $x=8250 $y=5600 $w=1500 $h=200

.MEASURE AC AC_Measure_GainBandwidthProduct_1_Gain MAX vdb(O ut) OFF

.MEASURE AC AC_Measure_GainBandwidthProduct_1_UGFreq WHEN Vdb(O ut)=0 OFF

.MEASURE AC AC_Measure_GainBandwidthProduct_1 PARAM='AC_Measure_GainBandwidthProduct_1_Gain*AC_Measure_GainBandwidthProduct_1_UGFreq' +ON $ $x=8250 $y=5200 $w=1500 $h=200

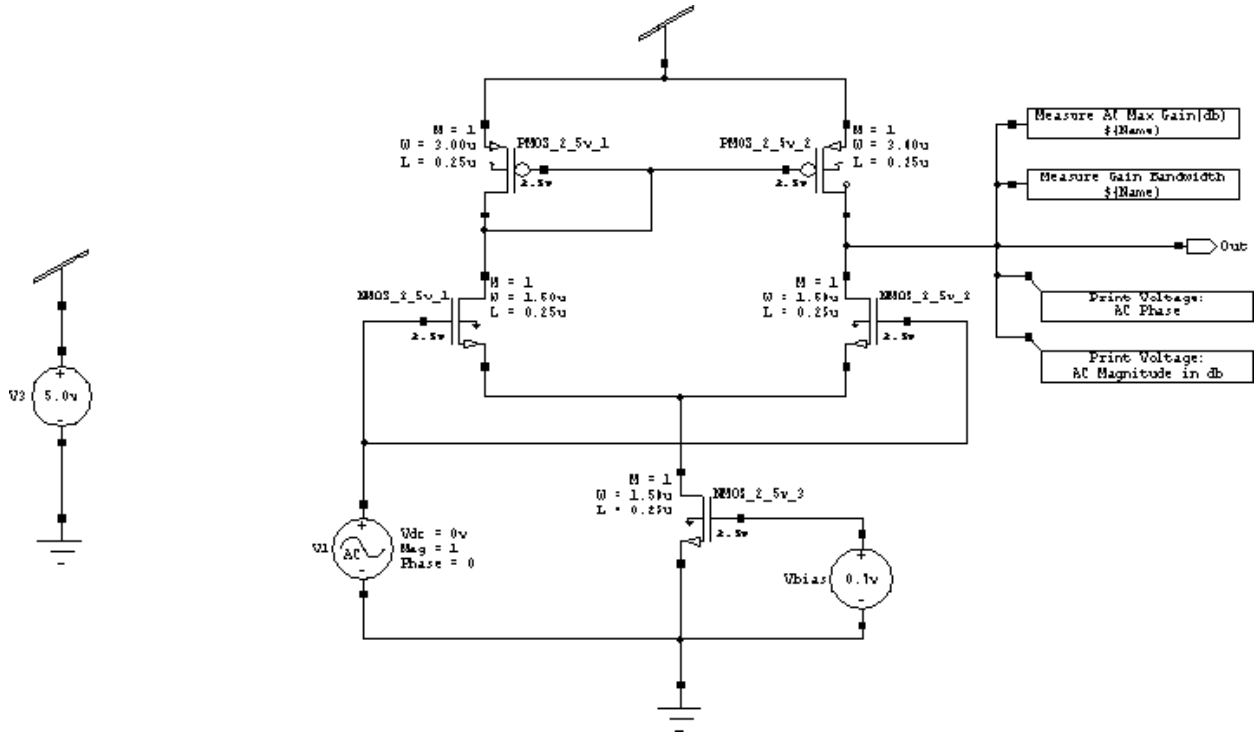
********* Simulation Settings - Analysis Section *********

.ac dec 25 10 10X

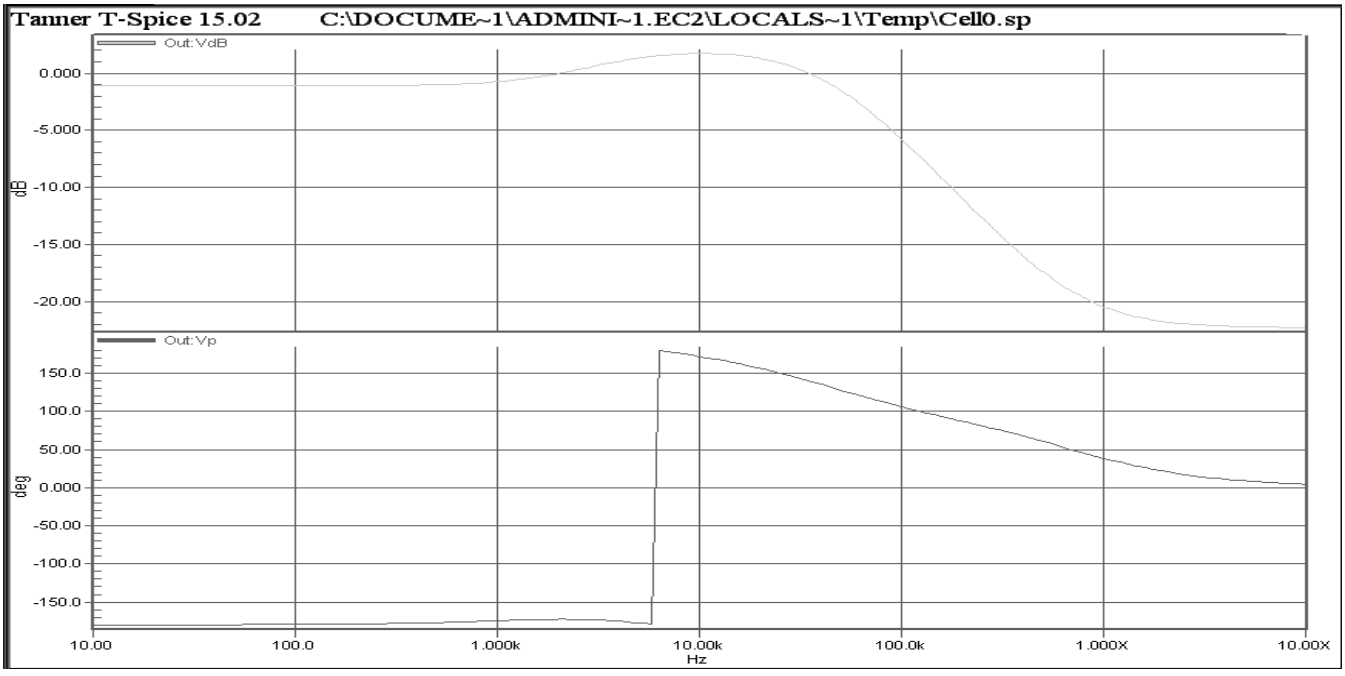
********* Simulation Settings - Additional SPICE Commands *********

.end

COMMON MODE:



COMMON MODE OUTPUT



NETLIST:

********* Simulation Settings - General Section *********

.lib "C:\Documents and Settings\ece01\My Documents\Tanner EDA\Tanner Tools v15.0\Process\Generic_250nm\Generic_250nm_Tech\Generic_250nm.lib" TT

*-------- Devices With SPICE.ORDER == 0.0 --------

***** Top Level *****

MNMOS_2_5v_1 N_1 N_2 N_3 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u

+$ $x=3793 $y=4300 $w=414 $h=600

MNMOS_2_5v_2 Out N_2 N_3 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u

+$ $x=6607 $y=4300 $w=414 $h=600 $m

MNMOS_2_5v_3 N_3 N_5 Gnd 0 NMOS25 W=1.5u L=250n AS=975f PS=4.3u AD=975f PD=4.3u

+$ $x=5507 $y=3000 $w=414 $h=600 $m

MPMOS_2_5v_1 N_1 N_1 Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u

+$ $x=4207 $y=5300 $w=414 $h=600 $m

MPMOS_2_5v_2 Out N_1 Vdd Vdd PMOS25 W=3u L=250n AS=1.95p PS=7.3u AD=1.95p PD=7.3u

+$ $x=6193 $y=5300 $w=414 $h=600

*-------- Devices With SPICE.ORDER > 0.0 --------

VV3 Vdd Gnd DC 5 $ $x=1200 $y=3800 $w=400 $h=600

VVbias N_5 Gnd DC 700m $ $x=6500 $y=2600 $w=400 $h=600

VV1 N_2 Gnd DC 0 AC 1 0 $ $x=3200 $y=2800 $w=400 $h=600

.PRINT AC Vdb(O ut) $ $x=8350 $y=4050 $w=1500 $h=300

.PRINT AC Vp(O ut) $ $x=8350 $y=4450 $w=1500 $h=300

.MEASURE AC AC_Measure_Gain_1 MAX vdb(Out) ON $ $x=8250 $y=5600 $w=1500 $h=200

.MEASURE AC AC_Measure_GainBandwidthProduct_1_Gain MAX vdb(O ut) OFF

```
.MEASURE AC AC_Measure_GainBandwidthProduct_1_UGFreq WHEN Vdb(Out)=0 OFF

.MEASURE AC AC_Measure_GainBandwidthProduct_1
PARAM='AC_Measure_GainBandwidthProduct_1_Gain*AC_Measure_GainBandwidthProduct_1_
UGFreq'

+ON $ $x=8250 $y=5200 $w=1500 $h=200

********* Simulation Settings - Analysis Section *********

.ac dec 25 10 10X

********* Simulation Settings - Additional SPICE Commands *********

.end
```