SCUBA-2 Block Specification

1-Wire Read Data Protocol

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1. Block Overview

1.1 Block Location and Block Interface Within System

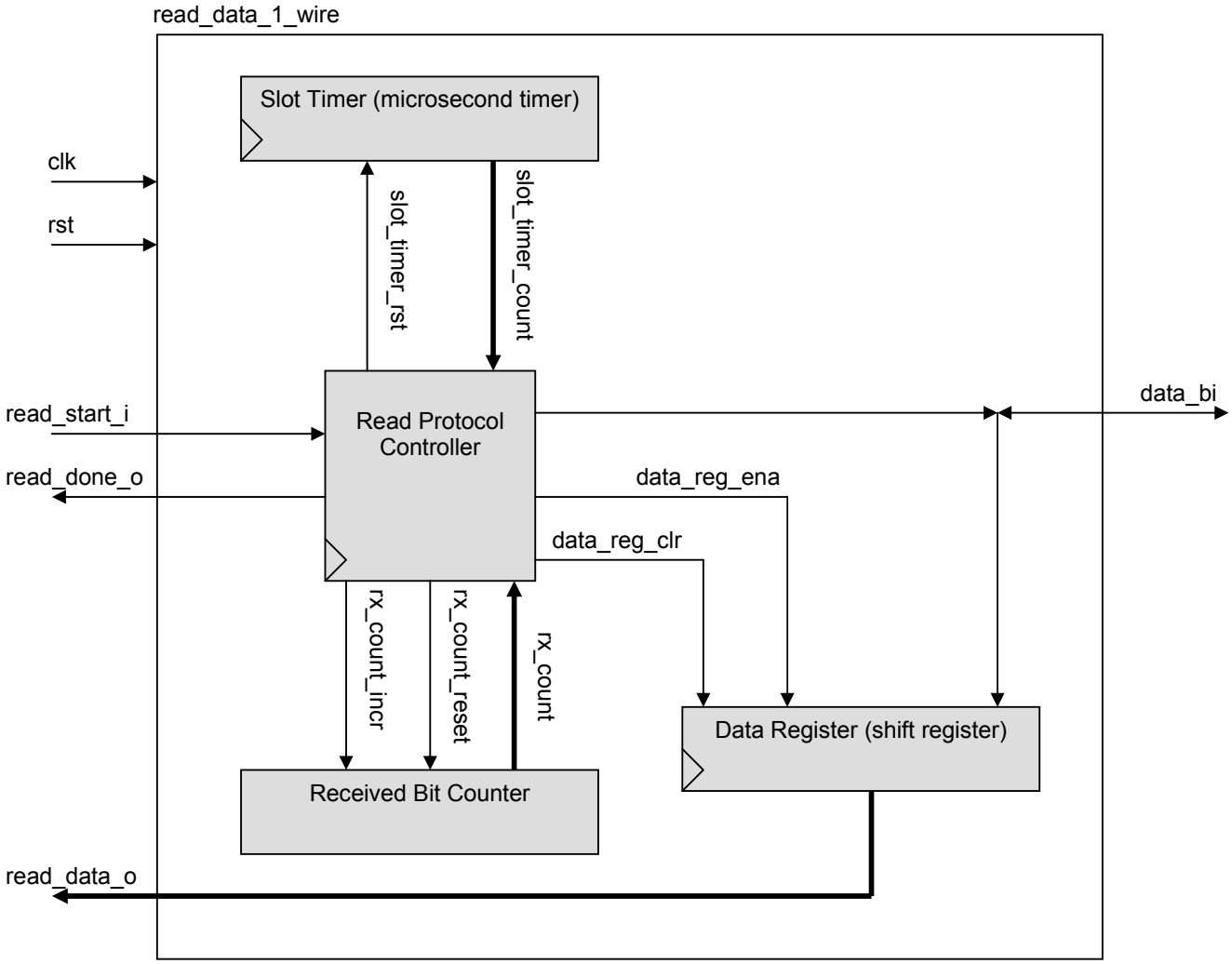
The 1-wire read protocol is part of a group of modules, which collectively enable communication with a device using a 1-wire signalling scheme. Two modules which use 1-wire signalling to communicate are:

- Card_id
- Temperature

1.2 Block Functionality / Features

- Produces read-time slots according to 1-wire signalling specifications
- Listens for and collects serial data, then outputs it as a single vector.
- Parameterized to allow data of different lengths to be collected.

1.3 Block Dataflow



2. Block Interfaces

2.1 Interface Signal Description

Table 1: Interface Signals

Signal	Description	Direction
Global Signals		
clk	Global clock signal.	in
rst	Global active-high asynchronous reset	in
Control Signals		
read_start_i	Active-high start signal. Starts reading of serial data from 1-wire device.	in
read_done_o	Active-high done signal. Indicates that read has completed.	out
Data Signals		
data_bi	Data line to 1-wire device	bidir
read_data_o	Data that was read from 1-wire device.	out

2.2 Interface Protocol and Timing

See datasheet.

3. High-Level Description

3.1 State Machine Description

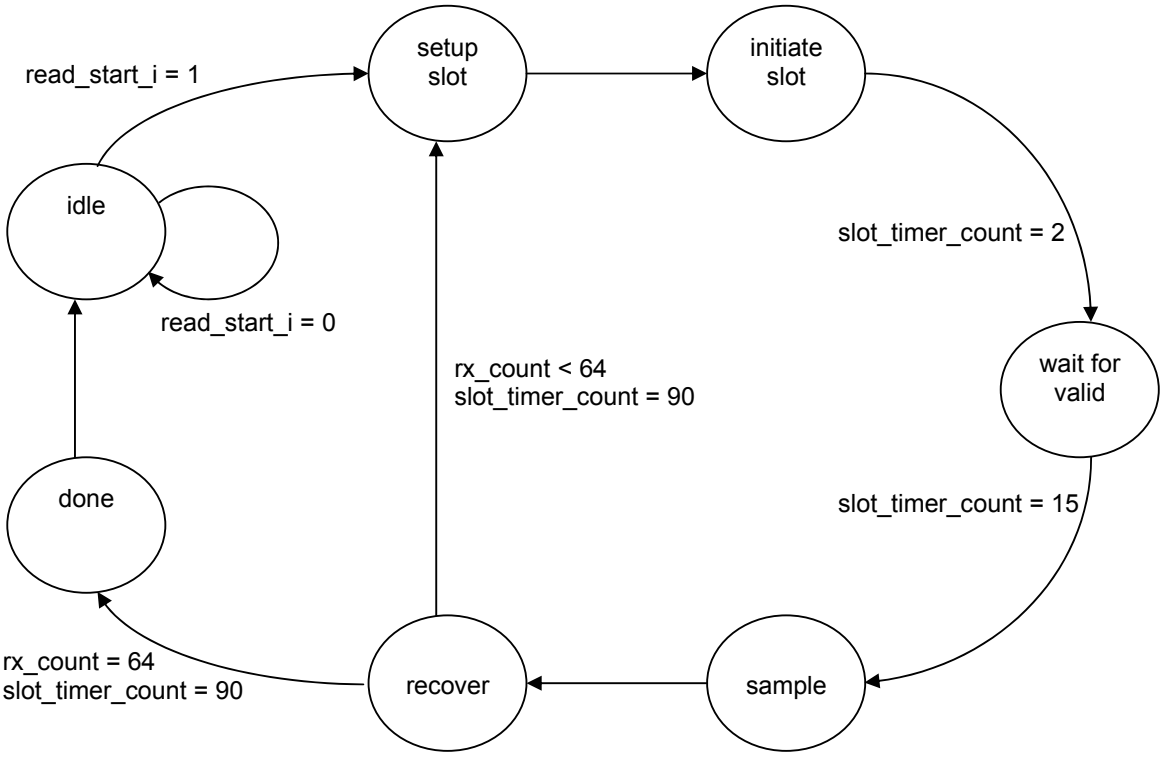


Table 2:State Machine Output Values

State / Signal	idle	setup slot		initiate slot	wait for valid	sample	recover	done
		rx_count = 0	rx_count > 0					
data_reg_ena	0	1	0	0	0	1	0	0
data_reg_clr	0	1	0	0	0	0	0	0
rx_count_incr	0	1	1	0	0	0	0	0
rx_count_reset	1	0	0	0	0	0	0	0
slot_timer_reset	0	1	1	0	0	0	0	0
data_bi	Z	Z	Z	0	Z	Z	Z	Z
read_done_o	0	0	0	0	0	0	0	1

Table 3: State Machine Output Signal Description

Signal	Description
data_reg_ena	Active-high data register enable.
data_reg_clr	Active-high data register clear.
rx_count_incr	Active-high received bit counter increment.
rx_count_reset	Active-high received bit counter reset.
slot_timer_reset	Active-high slot timer reset.
data_bi	Data line to/from 1-wire device.
read_done_o	Active-high signal indicating read completion.

4. Files of the Block

4.1 Source Code

4.1.1 read_data_1_wire.vhd

This file contains the state machine that implements the read protocol. It is compiled into the "components" library.

4.2 Header Code

4.2.1 component_pack.vhd

This file contains the timing parameters for the read protocol. It is compiled into the "sys_param" library.