SCUBA-2 Block Specification

1-Wire Initialization Protocol

February 11, 2004

Block Specification Page 1 of 7

Table of Contents

1.1 Block Location and Block Interface Within System 1.2 Block Functionality / Features 1.3 Block Dataflow 2. Block Interfaces 2.1 Interface Signal Description	3
2. Block Interfaces	
2.1 Interface Signal Description	
2.2 Interface Protocol and Timing	
3. High-Level Description	5
3.1 State Machine Description	5
4. Files of the Block	7
4.1 Source Code	
4.1.1 init_1_wire.vhd	
4.2 Header Code	

1. Block Overview

1.1 Block Location and Block Interface Within System

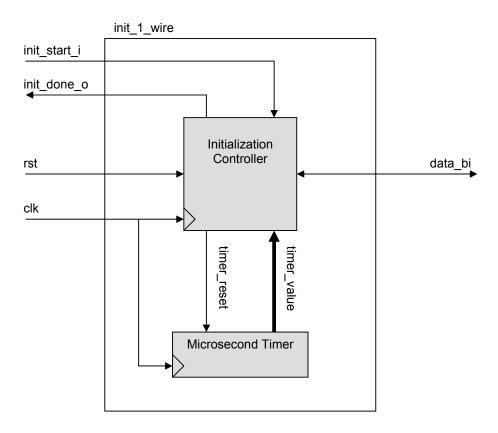
The 1-wire initialization protocol is part of a group of modules, which collectively enable communication with a device using a 1-wire signalling scheme. Two modules which use 1-wire signalling to communicate are:

- Card_id
- Temperature

1.2 Block Functionality / Features

- Produces initialization pulse according to 1-wire signalling specifications
- Listens for presence pulses sent by 1-wire slave devices

1.3 Block Dataflow



Block Specification 3 of 7

2. Block Interfaces

2.1 Interface Signal Description

Table 1: Interface Signals

Signal	Description	Direction
Global Signals		
clk	Global clock signal.	in
rst	Global asynchronous active-high reset.	in
Control Signals init_start_i	Active-high start signal. Starts initialization protocol.	in
init_done_o	Active-high done signal. Indicates that initialization has completed.	out
Data Signals		
data_bi	Data line to 1-wire slave device	bidir

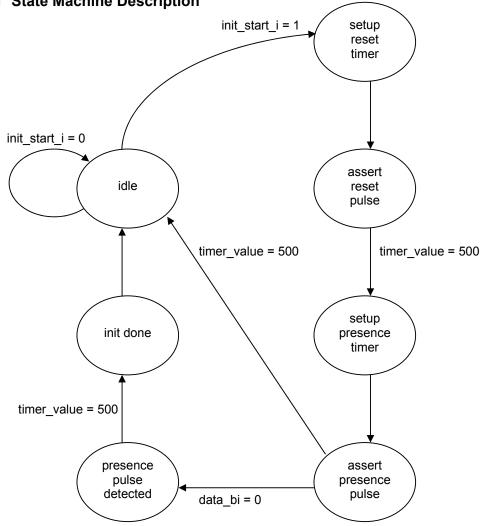
2.2 Interface Protocol and Timing

See datasheet.

Block Specification 4 of 7

3. High-Level Description

3.1 State Machine Description



Block Specification 5 of 7

Table 2: State Machine Outputs

State	Signal	Value
IDLE	data_bi	Z
	timer_reset	0
	init_done_o	0
SETUP_RESET	data_bi	Z
	timer_reset	1
	init_done_o	0
ASSERT_RESET	data_bi	0
AGOLINI_REGET	timer_reset	0
	init_done_o	0
CETUD DDECENCE	doto hi	7
SETUP_PRESENCE	data_bi	Z
	timer_reset	1
	init_done_o	0
ASSERT_PRESENCE	data_bi	Z
	timer_reset	0
	init_done_o	0
DETECTED	data_bi	Z
	timer_reset	0
	init_done_o	0
INIT_DONE	data_bi	Z
	timer_reset	0
	init_done_o	1

Table 3: Description of State Machine Outputs

Signal	Description
data_bi	Bidirectional data line to/from 1-wire device.
timer_reset	Resets the microsecond timer.
init_done_o	Indicates that a 1-wire device was detected.

Block Specification 6 of 7

4. Files of the Block

4.1 Source Code

4.1.1 init_1_wire.vhd

This file contains the state machine that implements the initialization protocol. It is compiled into the "components" library.

4.2 Header Code

4.2.1 component_pack.vhd

This file contains the timing parameters of the initialization protocol. It is compiled into the "sys_param" library.

Block Specification 7 of 7