Clock Card Test Software Description

This document outlines the basic operation and structure of the clock card test software. The purpose of the software is to allow an operator to test the basic hardware functionality of the clock card for diagnosis and test purposes.

Revision History

Revision	Date	Author	Description
1	Dec 20,2003	NRG	Initial document

Test Setup

The following equipment is needed in order to operate the software:

- A clock card programmed with the test software. If the card needs to be programmed, an Altera ByteBlaster cable with the appropriate software installed on a PC will also be required.
- A power source for the clock card.
- A PC with a serial port that has a serial communication program installed (like HyperTerminal or TeraTerm).
- A serial port adapter cable that be plugged into the clock card debug header (covered in another document).
- Equipment suitable to observe the hardware functions of the clock card, such as an oscilloscope or a logic analyzer.

Boot the test PC once all of the electrical connections have been made to the clock card. Then start the serial port application and configure it to 115 Kbaud, 8 data bits, 1 stop bit, no parity and no flow control (software or hardware). The turn on the power to the clock card. You should see a message like the following if the card has been programmed properly:

```
CC Test vxx.yy
>
```

Where xx.yy is the current software version number.

The following sections outline the various tests that can be performed.

Test Commands

All of the software test commands toggle various tests on and off. Turning on a command will automatically turn off the previous one. All test outputs are readable ASCII text, ie values in the range ‘0’..’9’, ‘a’..’z’ and ‘A’..’Z’. Idle state is indicated by transmitting a “>” character to the serial port. Valid test commands are:

r Reset: Resets the clock card software. When complete, the power up message will be displayed and the system will return to an idle state.

IA Read Array ID: Returns the array identification as a hexadecimal number. When complete, the system will return to an idle state.

IS Read Slot ID: Returns the slot identification as a hexadecimal number. When complete, the system will return to an idle state.

IN Read Silicon Serial Number: Returns the silicon serial number as a hexadecimal number. When complete, the system will return to an idle state.

IB Read Box ID: Returns the box ID as a hexadecimal number. When complete, the system will return to an idle state.

S Read System Status: Returns a bit field representing the system status in the following format (see schematic for net names), followed by a line feed:

<+5VOK><EXTND><CONFRDY><SPTTL3>..<SPTTL1><SW6>..SW<2><SW-PB>

0 = off, 1 = on.

The output will continue until toggled off.

Rx Read Data from LVDS Receiver x (0 to 7): Outputs received data in hexadecimal format followed by a line feed (ASCII 10 and 13) until toggled off. Note that this means that the maximum receiver data rate is less than 115 kBaud, even though the receiver is operating at the system specified clock rate.

Tx Transmit Data to LVDS Transmitter x (0 to 2). 0 = CMD, 1 = SYNC, 2 = TXPARE. Outputs pseudo random numbers out the transmitter at the system specified clock rate until toggled off.

W Clear Watchdog Timer: Continuously clears the watchdog timer until toggled off.

J JTAG Test: Sends pseudo random numbers out the JTAG port until toggled off.

FR Fibre Optic Read Test: Reads data from the fibre optic receiver and writes the result in hexadecimal format to the serial port followed by a line feed until toggled off.

FW Fibre Optic Write Test: Writes pseudo random numbers to the fibre optic transmitter until toggled off.

FF Fibre Optic Flag Test: Returns a bit field representing the fibre optic flags in the following format (see schematic for net names), followed by a line feed:

<F_DVPF><F_DVPB>

0 = off, 1 = on.

The output will continue until toggled off.

Lx Toggle LED x (0 to 2) State: Toggles the state of LED x to either off or on. X=0 toggles D1, X=1 toggles D2 and X=2 toggles D3.

E EEPROM Test: Does a read/write verification that all EEPROM locations can be accessed. Returns the result of the test as “P” for pass or “F” for fail. Once complete, the system returns to idle state.

T Temperature Test: Returns the current FPGA temperature in hexadecimal followed by a line feed until toggled off.

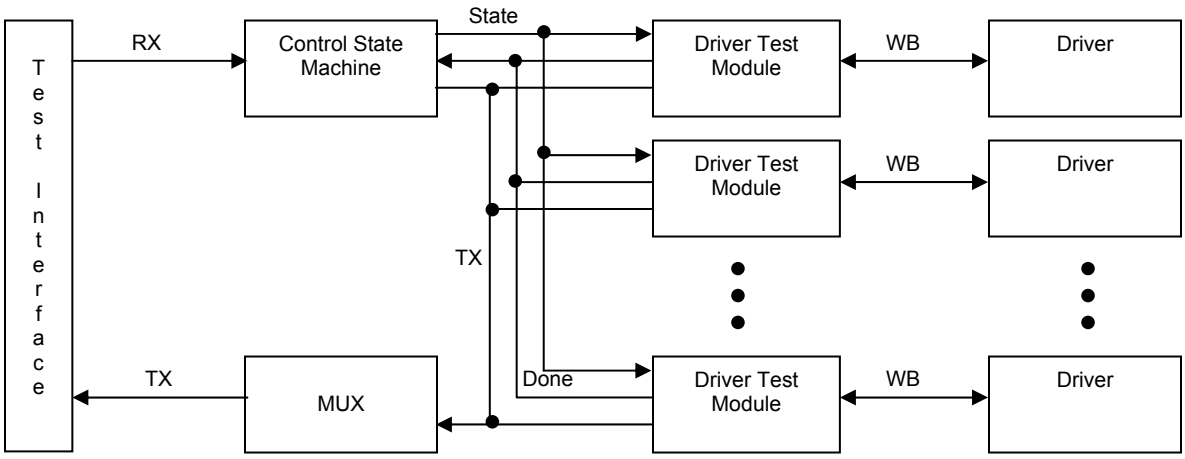
Mx SRAM Memory Test for Bank x (0 or 1): Does a read/write verification that all SRAM locations can be accessed. Returns the result of the test as “P” for pass or “F” for fail. Once complete, the system returns to idle state. Bank 0 refers to U31, Bank 1 U32.

PR Power Supply Card Read Test: Reads data from the power supply card interface and writes the result in hexadecimal format to the serial port followed by a line feed until toggled off.

PW Power Supply Card Write Test: Writes pseudo random numbers to the power supply card until toggled off.

Test Software Architecture

The following figure diagrams the basic structure of the test software:



Note that the figure doesn't show any clock or reset signals, but they will be needed for proper implementation.

The control state machine constantly monitors the serial port, looking for new commands. When in idle state, the control state machine can also transmit data back to the test PC through the multiplexer. The control state machine has 1 state output for each driver test module, plus 1 for idle. When a driver test module's state input is 1, then the module can activate its test sequence. The test module uses a Wish Bone interface to communicate with the hardware driver to execute the test. Any data that needs to be sent to the serial port goes through the multiplexer and to the test PC serial port. Once the test is completed (assuming it does complete), the test module can then assert a done flag back to the control state machine to make the system return to idle.

The intention is that the hardware device drivers will be the same as those used in the final design, but that reset of the software will be used only for testing the clock card functionality.

The test software will require the following driver test modules:

- Read Array ID
- Read Slot ID
- Read Silicon Serial Number
- Read Box ID
- Read Status
- Read LVDS Receiver (replicated 8 times)
- Write LVDS Transmitter (replicated 3 times)
- Clear Watchdog Timer
- Write JTAG
- Read Fibre Optic Receiver
- Write Fibre Optic Transmitter
- Read Fibre Optic Flags
- Toggle Leds
- EEPROM Verification
- Read Temperature
- SRAM Verification (replicated twice)
- Read Power Supply Card

- Write Power Supply Card

Also, the following device driver modules will be required:

- Array ID
- Slot ID
- Silicon Serial Number
- Box ID
- Power Supply Status
- SPTTL
- Dip Switch
- Asynchronous LVDS Receiver (replicated 8 times)
- Asynchronous LVDS Transmitter (replicated 3 times)
- Clear Watchdog Timer
- JTAG
- Fibre Optic Receiver
- Fibre Optic Transmitter
- Fibre Optic Flags
- LEDs
- EEPROM (read and write)
- Temperature
- SRAM Verification (replicated twice) (read and write)
- Power Supply Card Receiver
- Power Supply Card Transmitter