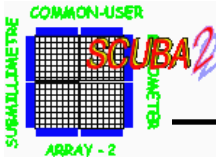


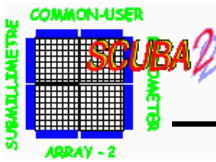
Wishbone Specification for SCUBA 2

v0.1



CHANGE RECORD

| Issue | Date | Section affected | Change Description |
|-------|------------|------------------|--------------------|
| 0.1 | 05/12/2003 | | First Draft |
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This document describes how the FPGA VHDL blocks for SCUBA 2 will implement the Wishbone bus architecture.

The following table, **Table 1**, shows the Wishbone signal name, the corresponding signal name from our own block diagrams, and whether the signal is an input or output relative to the master (Command FSM block).

We will consider the “Command FSM” block on each FPGA as the master, and the remaining blocks as the slaves. If anyone wants to create multiple masters on an FPGA, we have the option of doing that also.

Table 1 Wishbone Signal Description

| Wishbone Signal | Our Signal | Description | Direction |
|-----------------|--------------|--|-----------|
| CLK_I | clk | System clock signal. This signal goes to the master and slaves | in |
| RST_I | reset_n | Asynchronous system reset. This signal goes to the master and slaves. The Wishbone reset is active high. | in |
| DAT_O | r_dout(31:0) | Data going from the master (command FSM block) towards the slaves | out |
| DAT_I | r_din(31:0) | Data going from the slaves towards the master | in |
| ADR_O | r_addr(31:0) | Address signal going from the master. We will use this signal to select the slave block we want to read or write from (the slaves must decode the address to determine if they are the intended target for a read or write). Therefore, we must come up with an address map. | out |
| WE_O | r_wr / r_rd | Write Enable/ Read signal going from the master to the slaves. For write, WE_O = 1 For read, WE_O = 0 | out |
| STB_O | | Strobe signal from the master indicating it's initiating a read or write cycle with a slave | out |
| ACK_I | | Acknowledge signal from the slave to the master indicating that the slave is ready to send/receive data | in |
| CYC_O | | Cycle signal is asserted by the master the entire time during a valid bus cycle (read or write) | out |

For timing diagrams of read and write cycles, and for more information on Wishbone, please refer to the latest Wishbone Spec at:

<http://www.opencores.org/wishbone/>