Command Issued by CC LVDS SC2_ELE_S565_001_002	Size of Cmd (Bytes)	Hexidecimal Command Code (1 Byte)	Card Address (1 Byte) ('?'= '0' or '1')	Port Number (1 Byte)	Data (11 Bytes Max)	Notes (See bb_isa_discussn_revXX.doc for an explaination of what fields the columns with the blue headers represent)
Reserved		0x00				
AC Specific						
Get Active Row	1	0x01	10000000			Return the row that is currently being addressed
Set Active Row	2	0x02	10000000	0..40 (row #)		
Get D/A 'On' Value	2	0x03	10000000	0..40 (row #)		
Set D/A 'On' Value	4	0x04	10000000	0..40 (row #)	0..16383 (14-bit#)	
Activate D/A ('On')	2	0x05	10000000	0..40 (row #)		Turn on DAC <xx>
Get D/A 'Off' Value	2	0x06	10000000	0..40 (row #)		
Set D/A 'Off' Value	4	0x07	10000000	0..40 (row #)	0..16383 (14-bit#)	
Deactivate D/A ('Off')	2	0x08	10000000	0..40 (row #)		Turn off DAC <xx>
		0x09				
		0x0A				
		0x0B				
		0x0C				
		0x0D				
		0x0E				
		0x0F				
RC Specific						
Get 1st Stage Feedback	3	0x10	0????000	0..7 (column#)	0..40 (row#)	
Set 1st Stage Feedback	5	0x11	0????000	0..7 (column#)	0..40 (row#); 0..16383 (14-bit#)	The 1st stage feedback will be different for every pixel in a column.
Refresh 1st Stage Feedback	2	0x12	0????000	0..7 (column#)		
Get SA Bias	2	0x13	0????000	0..7 (column#)		
Set SA Bias	4	0x14	0????000	0..7 (column#)	0..65535 (16-bit#)	This value does not change for every row
Refresh SA Bias	2	0x15	0????000	0..7 (column#)		
Get Offset	2	0x16	0????000	0..7 (column#)		
Set Offset	4	0x17	0????000	0..7 (column#)	0..65535 (16-bit#)	This value does not change for every row
Refresh Offset	2	0x18	0????000	0..7 (column#)		
Get Active Columns	1	0x19	0????000			
Set Active Columns	3	0x1A	0????000	0xFF (invalid)	????????	There are 8 readout columns per RC. Each bit position corresponds to the status of a column. bit 0 (LSB)- Channel0..; bit 7- Channel7. Bit values: 0- Inactive; 1- Active
**Get Frame Settling Delay	1	0x1B	0????000			**This command may not be included in the final version of firmware
**Set Frame Settling Delay	3	0x1C	0????000	0xFF (invalid)	0..255 (# of 50MHzr ref clk cycles)	**This command may not be included in the final version of firmware
		0x1D				
		0x1E				
		0x1F				
BC Specific						
Get Feedback (2nd Stage FB, 2nd Stage Bias, SA FB)	2	0x20	00000???	0..7 (column#)		
Set Feedback (2nd Stage FB, 2nd Stage Bias, SA FB)	4	0x21	00000???	0..7 (column#)	0..65535 (16-bit#)	Records a 16-bit # in memory
Refresh Feedback	2	0x22	00000???	0..7 (column#)		Clocks the recorded number into the DAC
Get Heater (Detector Bias, Pixel Heater)	1	0x23	00000???			
Set Heater (Detector Bias, Pixel Heater)	3	0x24	00000???	0xFF (invalid)	0..65535 (16-bit#)	
Refresh Heater	1	0x25	00000???			
		0x26				
		0x27				
		0x28				
		0x29				
		0x2A				
		0x2B				
		0x2C				
		0x2D				
		0x2E				
		0x2F				
General						
Get Frame-Sequence Number	1	0x30	11111111			
Set Frame-Sequence Number	4	0x31	11111111	0xFF (invalid)	0..65535 (5.46 min of 200Hz frames)	Assumes that the CC will begin at 0 and count up to the given frame number.
Get Frame Row-Order	1	0x32	11111111			
Set Frame Row-Order	13	0x33	11111111	0..3 (row group#)	0..40 x11 (row#'s)	The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, a sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40.
Get Frame Start Row	1	0x34	11111111			
Set Frame Start Row	2	0x35	11111111	0..40 (row#)		Determines which row in the 41-row sequence is designated '1st' in a frame
Get Next n Frames of Data (data includes reading#)	1	0x36	11111111			If no parameters are included, then a single frame will be returned
Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3)	1	0x37	11111111			Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in.
Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3)	3	0x38	11111111	0xFF (invalid)	0..3 (mode#)	"Card Address" field is optional
Get n/16 BB delay	1	0x39	????????			
Set n/16 BB delay	3	0x3A	????????	0xFF (invalid)	0..31 (n/16 fraction# of 50MHz ref clk)	This setting will be different for every card, depending on its position in the subrack. n/16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CC synchronously
Begin MUX	0	0x3B				Begin multiplexing SQUIDs
Stop MUX	0	0x3C				Stop multiplexing SQUIDs
		0x3D				
		0x3E				
		0x3F				
Housekeeping						
CC Online	0	0x40				A status message that notifies other cards that the CC is active
Get Temperature	1	0x41	????????			
Get Serial Number	1	0x42	????????			
Get Voltage Levels	1	0x43	????????			
Get Faceplate LEDs Status	1	0x44	????????			
Set Faceplate LEDs Status	2	0x45	????????	0000????		There are 4 LEDs per faceplate. Each bit position corresponds to an LED. 0- Fault; 1- Undefined; 2- FPGA Run; 3- Power. Bit values: 0- Inactive; 1- Active
Get Card Type	1	0x46	????????			
Get Slot #	1	0x47	????????			
Get Firmware Version #	1	0x48	????????			
Register Reset	1	0x49	????????			Reset certain designated registers to default values encoded in firmware
Run Self-Diagnostics, and Return Status	1	0x4A	????????			For Janos :-)
Prepare For Shutdown	0	0x4B	11111111			Will notify cards that a shutdown is immenant, and that they should perform tasks in preparation for reconfiguration or loss of power
		0x4C				