SCUBA-2 Block Specification

Generic Shift Register

February 11, 2004

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1. Block Overview

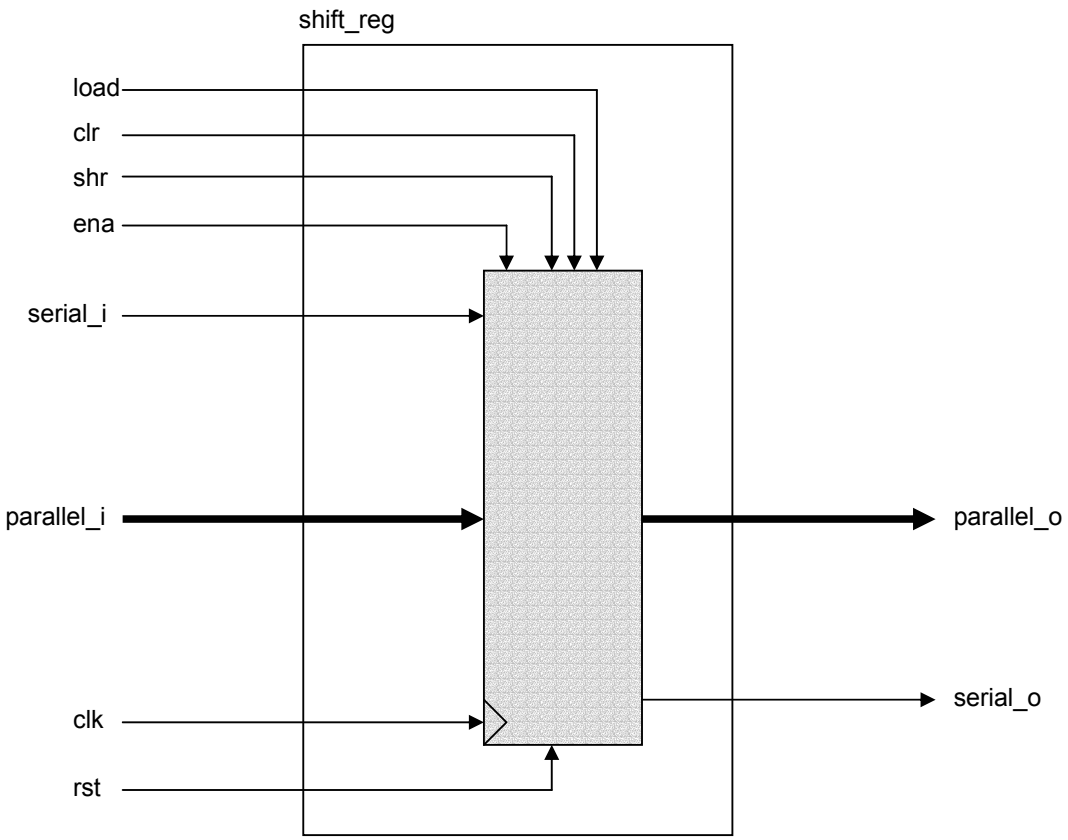
1.1 Block Location and Block Interface Within System

The generic shift register is used as a basic building block within other modules.

1.2 Block Functionality / Features

- Parameterized data width (2 to 512 bits wide)
- Synchronous parallel input and output
- Synchronous serial input and output
- Asynchronous reset
- Synchronous clear
- Synchronous load
- Register enable
- Shift-right or shift-left capability

1.3 Block Dataflow



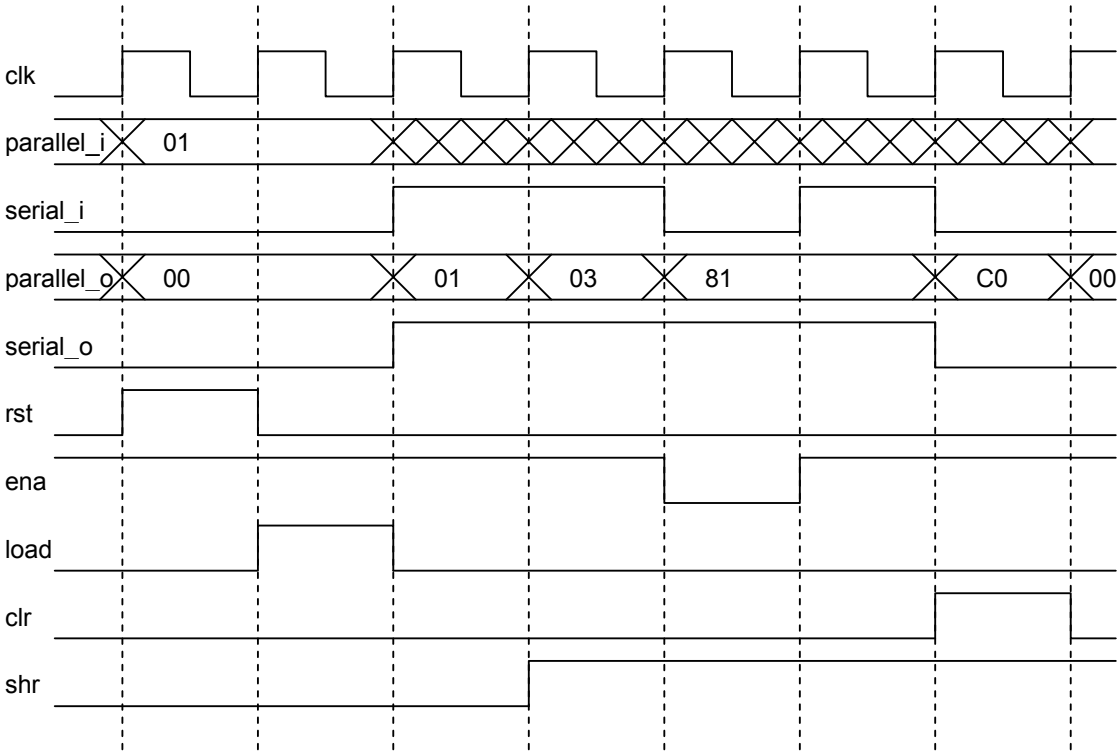
2. Block Interfaces

2.1 Interface Signal Description

Table 1: Interface Signals

Signal	Description	Direction
Global Signals		
clk	Global clock signal	in
rst	Global asynchronous active-high reset	in
Shift Register Controls		
ena	Active-high register enable	in
load	Active-high register synchronous load	in
clr	Active high register synchronous clear	in
shr	Indicates shift direction. For right-shift, shr=1, for left-shift, shr=0.	in
Data Signals		
serial_i	Serial data input	in
serial_o	Serial data output	in
parallel_i	Parallel data input. Used with load signal for parallel load capability.	in
parallel_o	Parallel data output	in

2.2 Interface Protocol and Timing



3. Files of the Block

3.1 Source Code

3.1.1 shift_reg.vhd

This file contains the implementation for the generic shift register. It is compiled into the "components" library.

3.2 Header Code

Not applicable for this block.