Command Issued by CC LVDS	Size of	Hexidecimal	Card Address	Port Number	Data (44 Ryton May)	Notes (See bly ing discussor rovVV do for an explaination of what fields the
SC2_ELE_S565_001_002	Cmd (Bytes)	Command Code (1 Byte)	(1 Byte) ('?'= '0' or '1')	(1 Byte)	(11 Bytes Max)	(See bb_isa_discussn_revXX.doc for an explaination of what fields the columns with the blue headers represent)
Reserved		0x00				
AC Specific		0.03	10000000			
Get Active Row Set Active Row	1 2	0x01 0x02	10000000	040 (row #)		Return the row that is currently being addressed
Get D/A 'On' Value	2	0x03	10000000	040 (row #)		
Set D/A 'On' Value	4	0x04	10000000	040 (row #)	016383 (14-bit#)	
Activate D/A ('On') Get D/A 'Off' Value	2	0x05 0x06	10000000	040 (row #) 040 (row #)		Turn on DAC <xx></xx>
Set D/A 'Off' Value	4	0x07	10000000	040 (row #)	016383 (14-bit#)	
Deactivate D/A ('Off')	2	0x08	10000000	040 (row #)		Tum off DAC <xx></xx>
		0x09 0x0A				
		0x0B				
		0x0C				
		0x0D 0x0E				
		0x0F				
RC Specific						
Get 1st Stage Feedback	3	0x10 0x11	05555000	07 (column#)	040 (row#)	
Set 1st Stage Feedback Refresh 1st Stage Feedback	5 2	0x11	05555000	07 (column#) 07 (column#)	040 (row#); 016383 (14-bit#)	The 1st stage feedback will be different for every pixel in a column.
Get SA Bias	2	0x13	0????000	07 (column#)		
Set SA Bias	4	0x14	05555000	07 (column#)	065535 (16-bit#)	This value does not change for every row
Refresh SA Bias Get Offset	2	0x15 0x16	05555000	07 (column#)		
Set Offset	4	0x16	05555000	07 (column#) 07 (column#)	065535 (16-bit#)	This value does not change for every row
Refresh Offset	2	0x18	03333000	07 (column#)		
Get Active Columns	1	0x19	05555000			
Set Active Columns	3	0x1A	0????000	0xFF (invalid)	3333333	There are 8 readout columns per RC. Each bit position corresponds to the status of a column. bit 0 (LSB)- Channel0; bit 7- Channel7. Bit values: 0- Inactive; 1- Active
**Get Frame Settling Delay	1	0x1B	03333000			**This command may not be included in the final version of firmware
**Set Frame Settling Delay	3	0x1C	05555000	0xFF (invalid)	0255 (# of 50MHzr ref clk cycles)	**This command may not be included in the final version of firmware
		0x1D 0x1E				
		0x1F				
BC Specific Cet Foodback (2nd Stage EP, 2nd Stage Bins, SA EP)	2	0x20	00000???	07 (column#)		T
Get Feedback (2nd Stage FB, 2nd Stage Bias, SA FB) Set Feedback (2nd Stage FB, 2nd Stage Bias, SA FB)	4	0x20 0x21	00000555	07 (column#) 07 (column#)	065535 (16-bit#)	Records a 16-bit # in memory
Refresh Feedback	2	0x22	00000???	07 (column#)	003333 (10-bit#)	Clocks the recorded number into the DAC
Get Heater (Detector Bias, Pixel Heater)	1	0x23	00000???			
Set Heater (Detector Bias, Pixel Heater)	3	0x24 0x25	00000333	0xFF (invalid)	065535 (16-bit#)	
Refresh Heater	1	0x25 0x26	00000222			
		0x27				
		0x28				
		0x29 0x2A				
		0x2A 0x2B				
		0x2C				
		0x2C 0x2D				
		0x2C 0x2D 0x2E				
General		0x2C 0x2D				
Get Frame-Sequence Number	1	0x2C 0x2D 0x2E 0x2F	11111111			
	1 4	0x2C 0x2D 0x2E 0x2F	11111111	0xFF (invalid)	065535 (5.46 min of 200Hz frames)	Assumes that the CC will begin at 0 and count up to the given frame
Get Frame-Sequence Number		0x2C 0x2D 0x2E 0x2F		0xFF (invalid)	0.65535 (5.46 min of 200Hz frames)	Assumes that the CC will begin at 0 and count up to the given frame number.
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order	1 13	0x2C 0x2D 0x2D 0x2F 0x2F 0x30 0x31 0x32	11111111	0xFF (invalid) 03 (row group#)	065535 (5.46 min of 200Hz frames) 040 x11 (row#'s)	
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Get Frame Row-Order	1 13	0x2C 0x2D 0x2E 0x2F 0x30 0x31 0x32 0x33	11111111	03 (row group#)		number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, a sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40.
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order	1 13	0x2C 0x2D 0x2D 0x2F 0x2F 0x30 0x31 0x32	11111111			number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, a sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Get Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#)	1 13	0x2C 0x2D 0x2D 0x2F 0x2F 0x30 0x31 0x31 0x32 0x33 0x33 0x34 0x35	11111111 11111111 11111111 11111111 1111	03 (row group#)		number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame If no parameters are included, then a single frame will be returned
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Get Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3)	1 13 1 2 1	0x2C 0x2D 0x2D 0x2F 0x2F 0x30 0x31 0x32 0x32 0x32 0x33 0x33 0x33 0x34 0x35	11111111 11111111 11111111 11111111 1111	03 (row group#) 040 (row#)	040 x11 (row#'s)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, a sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in.
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Get Frame Start Row Get Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3)	1 1 2 1 1 1 3 3	0x2C 0x2D 0x2E 0x2F 0x2F 0x2F 0x30 0x31 0x31 0x32 0x33 0x33 0x34 0x36 0x36 0x37	1111111 1111111 1111111 1111111 1111111	03 (row group#)		number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame If no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Get Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3)	1 13 1 2 1	0x2C 0x2D 0x2D 0x2F 0x2F 0x30 0x31 0x32 0x32 0x32 0x33 0x33 0x33 0x34 0x35	11111111 11111111 11111111 11111111 1111	03 (row group#) 040 (row#)	040 x11 (row#'s)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, a sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in.
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Get Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay	1 1 2 1 1 1 3 1 1	0x2C 0x2D 0x2E 0x2F 0x2F 0x30 0x31 0x32 0x32 0x32 0x33 0x32 0x33 0x35 0x36 0x37	1111111 1111111 1111111 1111111 111111	03 (row group#) 040 (row#) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame If no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n/16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CC synchronously
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Get Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay	1 1 2 1 1 1 3 1 1 3 3 3 1 3	0x2C 0x2D 0x2D 0x2F 0x2F 0x2F 0x30 0x31 0x31 0x32 0x33 0x33 0x33 0x34 0x35 0x36 0x37 0x38 0x38 0x38	1111111 1111111 1111111 1111111 111111	03 (row group#) 040 (row#) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. In 16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its regises by so that all replies
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Get Frame Start Row Set Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay Begin MUX	1 1 2 1 1 1 3 1 1 3 1 3 0 0 0	0x2C 0x2D 0x2E 0x2F 0x2F 0x30 0x31 0x32 0x30 0x32 0x33 0x33 0x34 0x35 0x36 0x37 0x38 0x39 0x3A	1111111 1111111 1111111 1111111 111111	03 (row group#) 040 (row#) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0.29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n/16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CC synchronously Begin multiplexing SQUIDs
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Start Row Get Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay Begin MUX Stop MUX	1 1 2 1 1 1 3 1 1 3 1 3 0 0 0	0x2C 0x2D 0x2D 0x2F 0x2F 0x2F 0x30 0x31 0x31 0x32 0x33 0x33 0x33 0x34 0x35 0x36 0x37 0x38 0x38 0x38	1111111 1111111 1111111 1111111 111111	03 (row group#) 040 (row#) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0.29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n/16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CC synchronously Begin multiplexing SQUIDs
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Get Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay Begin MUX Stop MUX Housekeeping	1 1 2 2 1 1 1 1 3 1 3 1 3 0 0 0 0 0 0 0 0 0 0 0	0x2C	1111111 1111111 1111111 1111111 111111	03 (row group#) 040 (row#) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0.29 (in time), and a fourth command will specify the order of rows 30.40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n'16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CS synchronously Begin multiplexing SQUIDs
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Start Row Set Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set N/16 BB delay Set n/16 BB delay Begin MUX Stop MUX	1 1 2 1 1 1 3 1 1 3 1 3 0 0 0	0x2C 0x2D 0x2D 0x2F 0x2F 0x30 0x31 0x32 0x31 0x32 0x33 0x33 0x33 0x35 0x36 0x37 0x38 0x38 0x39 0x30 0x30 0x30 0x31	1111111 1111111 1111111 1111111 111111	03 (row group#) 040 (row#) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0.29 (in time), and a fourth command will specify the order of rows 30.40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n/16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CC synchronously Begin multiplexing SQUIDs
Get Frame-Sequence Number Get Frame Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Start Row Get Frame Start Row Get Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set n/16 BB delay Set n/16 BB delay Begin MUX Stop MUX Housekeeping CC Online Get Temperature Get Serial Number	1 1 2 1 1 1 3 3 1 1 3 3 0 0 0 0 1 1 1 1 1 1 1	0x2C	11111111 11111111 11111111 11111111 1111	03 (row group#) 040 (row#) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0.29 (in time), and a fourth command will specify the order of rows 30.40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n'16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CS synchronously Begin multiplexing SQUIDs
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Get Frame Start Row Set Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay Begin MUX Stop MUX Housekeeping CC Online Get Temperature Get Serial Number Get Voltage Levels	1 1 2 1 1 1 3 3 1 1 3 3 1 1 3 3 1 1 1 1	0x2C 0x2D 0x2F 0x2F 0x30 0x31 0x32 0x31 0x32 0x33 0x33 0x33 0x34 0x35 0x36 0x37 0x38 0x38 0x39 0x38 0x30 0x3C 0x3C 0x3C 0x3C 0x3C 0x3C 0x3C	1111111 1111111 1111111 1111111 111111	03 (row group#) 040 (row#) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0.29 (in time), and a fourth command will specify the order of rows 30.40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n'16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CS synchronously Begin multiplexing SQUIDs
Get Frame-Sequence Number Get Frame Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Get Frame Start Row Get Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set n/16 BB delay Set n/16 BB delay Begin MUX Stop MUX Housekeeping CC Online Get Temperature Get Serial Number Get Voltage Levels Get Faceplate LEDs Status	1 1 2 2 1 1 1 3 3 3 0 0 0 0 1 1 1 1 1 1 1 1 1 1	0x2C	11111111 11111111 11111111 11111111 1111	03 (row group#) 040 (row#) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0.29 (in time), and a fourth command will specify the order of rows 3.0-40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n'16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CC synchronously Begin multiplexing SQUIDs A status message that notifies other cards that the CC is active
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Get Frame Start Row Set Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay Begin MUX Stop MUX Housekeeping CC Online Get Temperature Get Serial Number Get Voltage Levels	1 1 2 1 1 1 3 3 1 1 3 3 1 1 3 3 1 1 1 1	0x2C	11111111 11111111 11111111 11111111 1111	03 (row group#) 040 (row#) 0xFF (invalid) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, a sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n'16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CS synchronously Begin multiplexing SQUIDs Stop multiplexing SQUIDs
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay Begin MUX Stop MUX Housekeeping CC Online Get Temperature Get Serial Number Get Veltage Levels Get Faceplate LEDs Status Get Card Type	1 1 2 2 1 1 1 3 3 3 0 0 0 0 1 1 1 1 1 1 1 1 1 1	0x2C	1111111 1111111 1111111 1111111 111111	03 (row group#) 040 (row#) 0xFF (invalid) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0.29 (in time), and a fourth command will specify the order of rows 30.40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n/16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CC synchronously. Begin multiplexing SQUIDs A status message that notifies other cards that the CC is active There are 4 LEDs per faceplate. Each bit position corresponds to an LED. 0- Fault; 1- Undefined; 2- FPGA Run; 3- Power. Bit values: 0-
Get Frame-Sequence Number Get Frame Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Get Frame Start Row Get Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay Begin MUX Stop MUX Housskeeping CC Online Get Temperature Get Serial Number Get Voltage Levels Get Faceplate LEDs Status Get Card Type Get Card Type Get Slot #	1 1 1 2 1 1 1 1 2 2 1 1 1 1 1 1 2 2 1 1 1 1 1 1 2 1 1 1 1 1 1 2 1 1 1 1 1 1 1 2 1	0x2C	11111111 11111111 11111111 11111111 1111	03 (row group#) 040 (row#) 0xFF (invalid) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0.29 (in time), and a fourth command will specify the order of rows 30.40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n/16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CC synchronously. Begin multiplexing SQUIDs A status message that notifies other cards that the CC is active There are 4 LEDs per faceplate. Each bit position corresponds to an LED. 0- Fault; 1- Undefined; 2- FPGA Run; 3- Power. Bit values: 0-
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Get Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay Begin MUX Stop MUX Housekeeping CC Online Get Temperature Get Serial Number Get Voltage Levels Get Faceplate LEDs Status Get Card Type Get Card Type Get Sirint #F Get Firm #F Get Fi	4 1 13 1 2 1 1 1 1 3 1 3 1 3 0 0 0 1 1 1 1 1 1 1 1	0x2C 0x2D 0x2F 0x2F 0x30 0x31 0x32 0x31 0x32 0x33 0x33 0x34 0x35 0x36 0x37 0x38 0x38 0x39 0x30 0x30 0x30 0x30 0x30 0x30 0x30	11111111 11111111 11111111 11111111 1111	03 (row group#) 040 (row#) 0xFF (invalid) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame If no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n/16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CC synchronously. Begin multiplexing SQUIDs A status message that notifies other cards that the CC is active There are 4 LEDs per faceplate. Each bit position corresponds to an LED. 0- Fault; 1- Undefined; 2- FPGA Run; 3- Power. Bit values: 0- Inactive; 1- Active
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Get Frame Start Row Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay Begin MUX Stop MUX Housekeeping CC Online Get Temperature Get Serial Number Get Voltage Levels Get Faceplate LEDs Status Get Card Type Get Slot #	1 1 1 2 1 1 1 1 2 2 1 1 1 1 1 1 2 2 1 1 1 1 1 1 2 1 1 1 1 1 1 2 1 1 1 1 1 1 1 2 1	0x2C	11111111 11111111 11111111 11111111 1111	03 (row group#) 040 (row#) 0xFF (invalid) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0.29 (in time), and a fourth command will specify the order of rows 30.40. Determines which row in the 41-row sequence is designated '1st' in a frame if no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n/16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CC synchronously. Begin multiplexing SQUIDs A status message that notifies other cards that the CC is active There are 4 LEDs per faceplate. Each bit position corresponds to an LED. 0- Fault; 1- Undefined; 2- FPGA Run; 3- Power. Bit values: 0-
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Get Frame Row-Order Get Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay Begin MUX Stop MUX Housskeeping CC Online Get Temperature Get Serial Number Get Temperature Get Temperature Get Serial Number Get Voltage Levels Get Fraceplate LEDs Status Get Card Type Get Slot # Get Firmware Version # Register Reset Run Self-Diagnostics, and Return Status	4 1 13 1 2 1 1 1 3 1 3 1 3 0 0 0 0 1 1 1 1 1 1 1 1	0x2C	11111111 11111111 11111111 11111111 1111	03 (row group#) 040 (row#) 0xFF (invalid) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame If no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n'16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CS synchronously. Begin multiplexing SQUIDs A status message that notifies other cards that the CC is active There are 4 LEDs per faceplate. Each bit position corresponds to an LED. 0 - Fault; 1- Undefined; 2 - FPGA Run; 3 - Power. Bit values: 0-Inactive; 1 - Active
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Get Frame Start Row Get Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay Housekeping CC Online Get Temperature Get Temperature Get Serial Number Get Voltage Levels Get Faceplate LEDs Status Get Card Type Get Sirt # Get Firmware Version # Register Reset	4 1 13 1 1 2 1 1 1 1 3 0 0 0 1 1 1 1 1 1 2 2 1 1 1 1 1 1 1 1 1	0x2C 0x2D 0x2D 0x2F 0x3D 0x3D 0x3D 0x31 0x31 0x32 0x33 0x32 0x33 0x32 0x33 0x35 0x36 0x37 0x36 0x39 0x39 0x30 0x36 0x37 0x36 0x37 0x38 0x39 0x30 0x30 0x30 0x31 0x32 0x32 0x33 0x35 0x36 0x37 0x36 0x37 0x36 0x37 0x38 0x39 0x30 0x40	11111111 11111111 11111111 11111111 111111	03 (row group#) 040 (row#) 0xFF (invalid) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one byte is used per row. In one command, a sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. There commands each containing a sequence of 17 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame If no parameters are included, then a single frame will be returned. If no parameters are included, then a single frame will be returned. Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. In 16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CC synchronously Begin multiplexing SQUIDs A status message that notifies other cards that the CC is active There are 4 LEDs per faceplate. Each bit position corresponds to an LED. O- Fault, 1- Undefined; 2- FPGA Run; 3- Power. Bit values: 0- Inactive, 1- Active
Get Frame-Sequence Number Set Frame-Sequence Number Get Frame Row-Order Set Frame Row-Order Set Frame Row-Order Set Frame Start Row Get Next n Frames of Data (data includes reading#) Get Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Set Mode (1- SM, 2- EM1, 3- EM2, 4- EM3) Get n/16 BB delay Set n/16 BB delay Begin MUX Stop MUX Housekeeping CC Online Get Temperature Get Serial Number Get Temperature Get Temper	4 1 13 1 2 1 1 1 3 1 3 1 3 0 0 0 0 1 1 1 1 1 1 1 1	0x2C	11111111 11111111 11111111 11111111 1111	03 (row group#) 040 (row#) 0xFF (invalid) 0xFF (invalid)	0.40 x11 (row#s) 0.3 (mode#)	number. The frame pixel order is specified as a series of rows. To specify a row, we need 6 bits, therefore, one by tei sued per row. In one command, a sequence of up to 11 rows can be specified at once, therefore 41/11 = 4 individual commands are necessary to specify a full row-addressing sequence. Three commands each containing a sequence of 10 rows will specify the order of rows 0-29 (in time), and a fourth command will specify the order of rows 30-40. Determines which row in the 41-row sequence is designated '1st' in a frame If no parameters are included, then a single frame will be returned Each mode will have a set of 'active columns' that are uniquely associated with it. All other parameters remain the same regardless of what mode you are in. 'Card Address' field is optional This setting will be different for every card, depending on its position in the subrack. n'16 refers to the the number of sixteenths of a 50 MHz reference clock cycle the card will delay its replies by so that all replies arrive at the CS synchronously. Begin multiplexing SQUIDs A status message that notifies other cards that the CC is active There are 4 LEDs per faceplate. Each bit position corresponds to an LED. 0-Fault; 1- Undefined; 2-FPGA Run; 3-Power. Bit values: 0-Inactive; 1-Active Reset certain designated registers to default values encoded in firmware For Janos:-)