SCUBA-2 Block Specification

1-Wire Write Data Protocol

February 13, 2004

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1. Block Overview

1.1 Block Location and Block Interface Within System

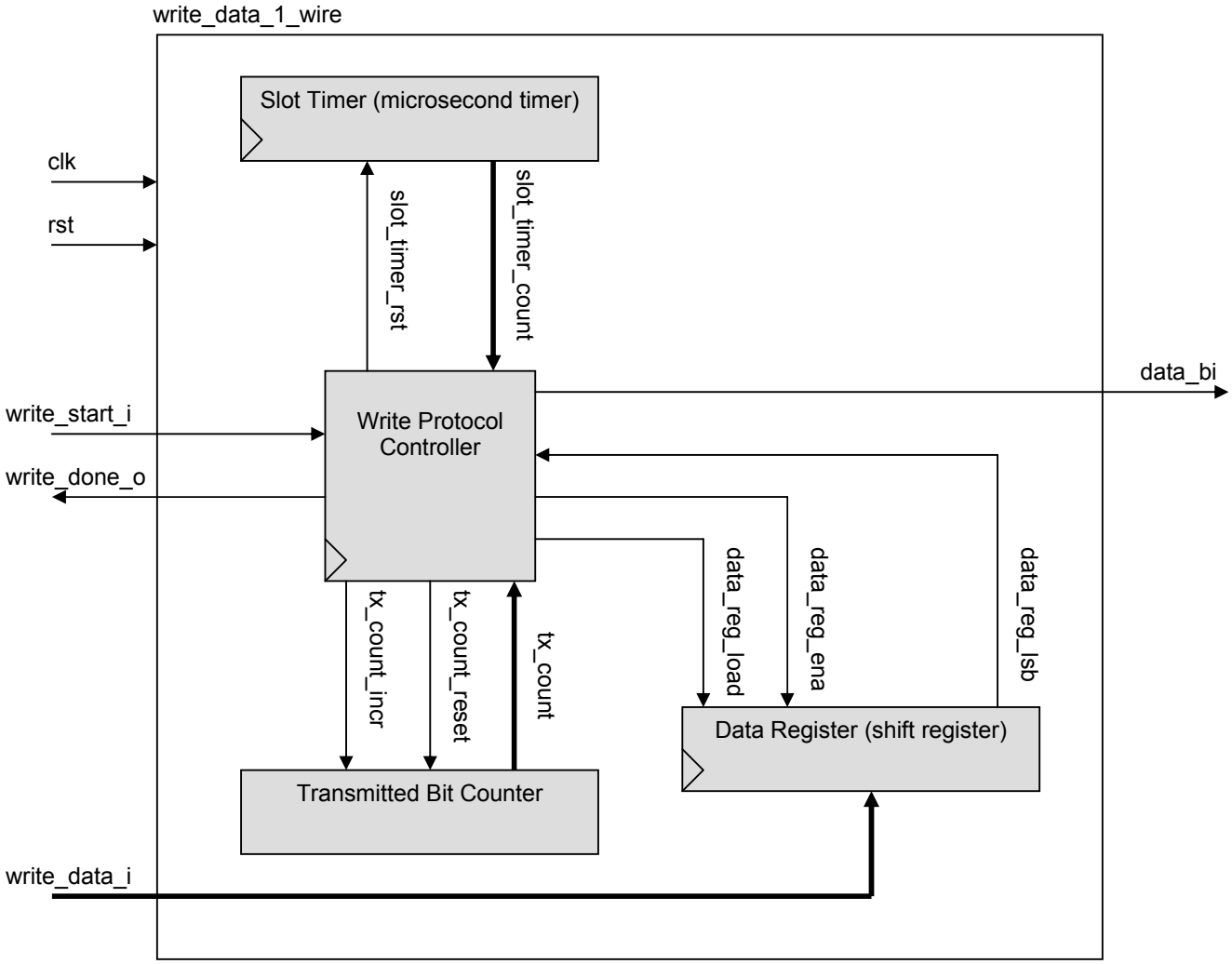
The 1-wire write protocol is part of a group of modules, which collectively enable communication with a device using a 1-wire signalling scheme. Two modules which use 1-wire signalling to communicate are:

- Card_id
- Temperature

1.2 Block Functionality / Features

- Produces write-time slots according to 1-wire signalling specifications
- Transmits a fixed length of data to 1-wire device.
- Parameterized to allow data of different lengths to be transmitted.

1.3 Block Dataflow



2. Block Interfaces

2.1 Interface Signal Description

Table 1: Interface Signals

Signal	Description	Direction
Global Signals		
clk	Global clock signal.	in
rst	Global active-high asynchronous reset	in
Control Signals		
write_start_i	Active-high start signal. Starts writing of data to 1-wire device.	in
write_done_o	Active-high done signal. Indicates that write has completed.	out
Data Signals		
data_bi	Data line to 1-wire device	bidir
write_data_i	Data that will be written to 1-wire device.	in

2.2 Interface Protocol and Timing

See datasheet.

3. High-Level Description

3.1 State Machine Description

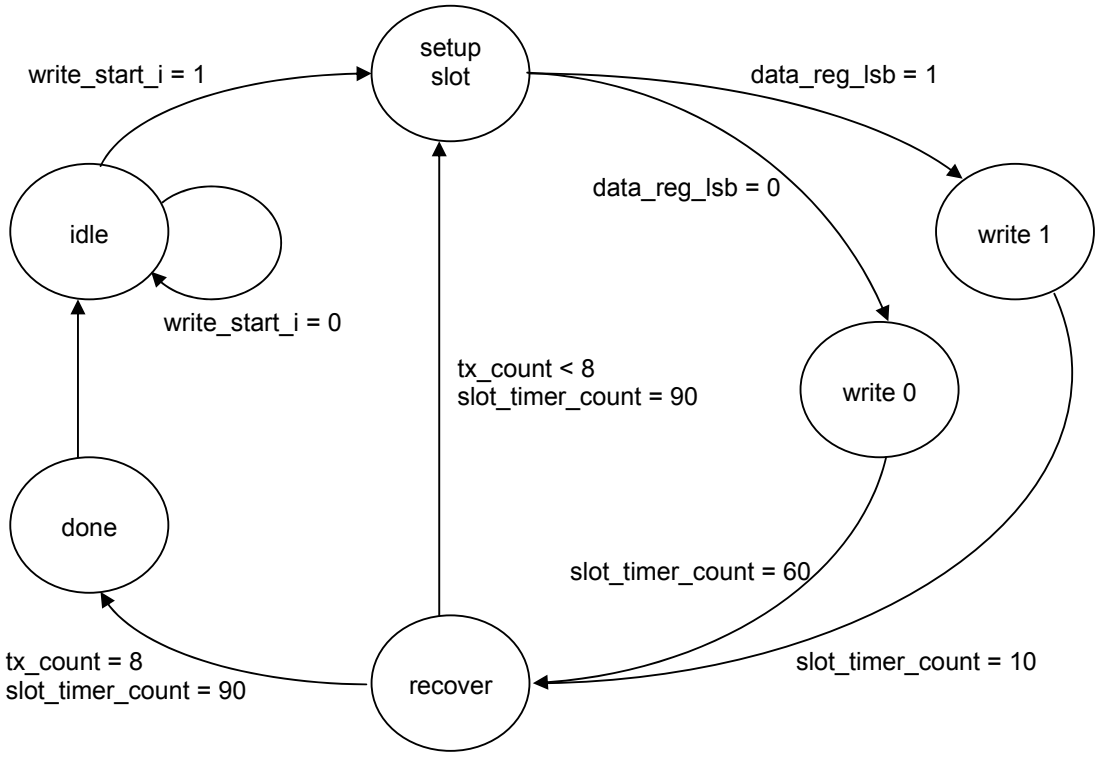


Table 2:State Machine Output Values

State / Signal	idle	setup slot	write 1	write 0	recover	done
data_reg_ena	1	1	0	0	0	0
data_reg_load	1	0	0	0	0	0
tx_count_incr	0	1	0	0	0	0
tx_count_reset	1	0	0	0	0	0
slot_timer_reset	0	1	0	0	0	0
data_bi	Z	Z	0	0	Z	Z
write_done_o	0	0	0	0	0	1

Table 3: State Machine Output Signal Description

Signal	Description
data_reg_ena	Active-high data register enable.
data_reg_load	Active-high data register parallel load.
tx_count_incr	Active-high transmitted bit counter increment.
tx_count_reset	Active-high transmitted bit counter reset.
slot_timer_reset	Active-high slot timer reset.
data_bi	Data line to/from 1-wire device.
write_done_o	Active-high signal indicating write completion.

4. Files of the Block

4.1 Source Code

4.1.1 write_data_1_wire.vhd

This file contains the state machine that implements the write protocol. It is compiled into the "components" library.

4.2 Header Code

4.2.1 component_pack.vhd

This file contains the timing parameters for the write protocol. It is compiled into the "sys_param" library.