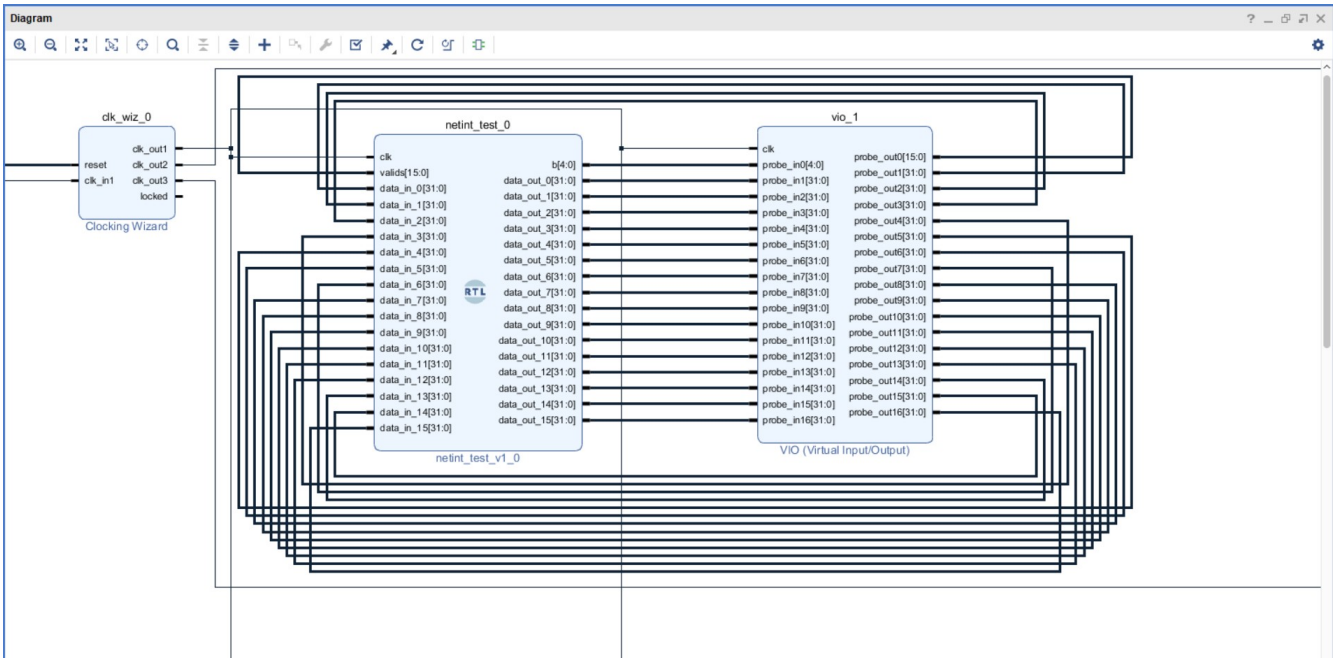
Sept. 15, 2019 Kevan Thompson

NETINT FPGA Test

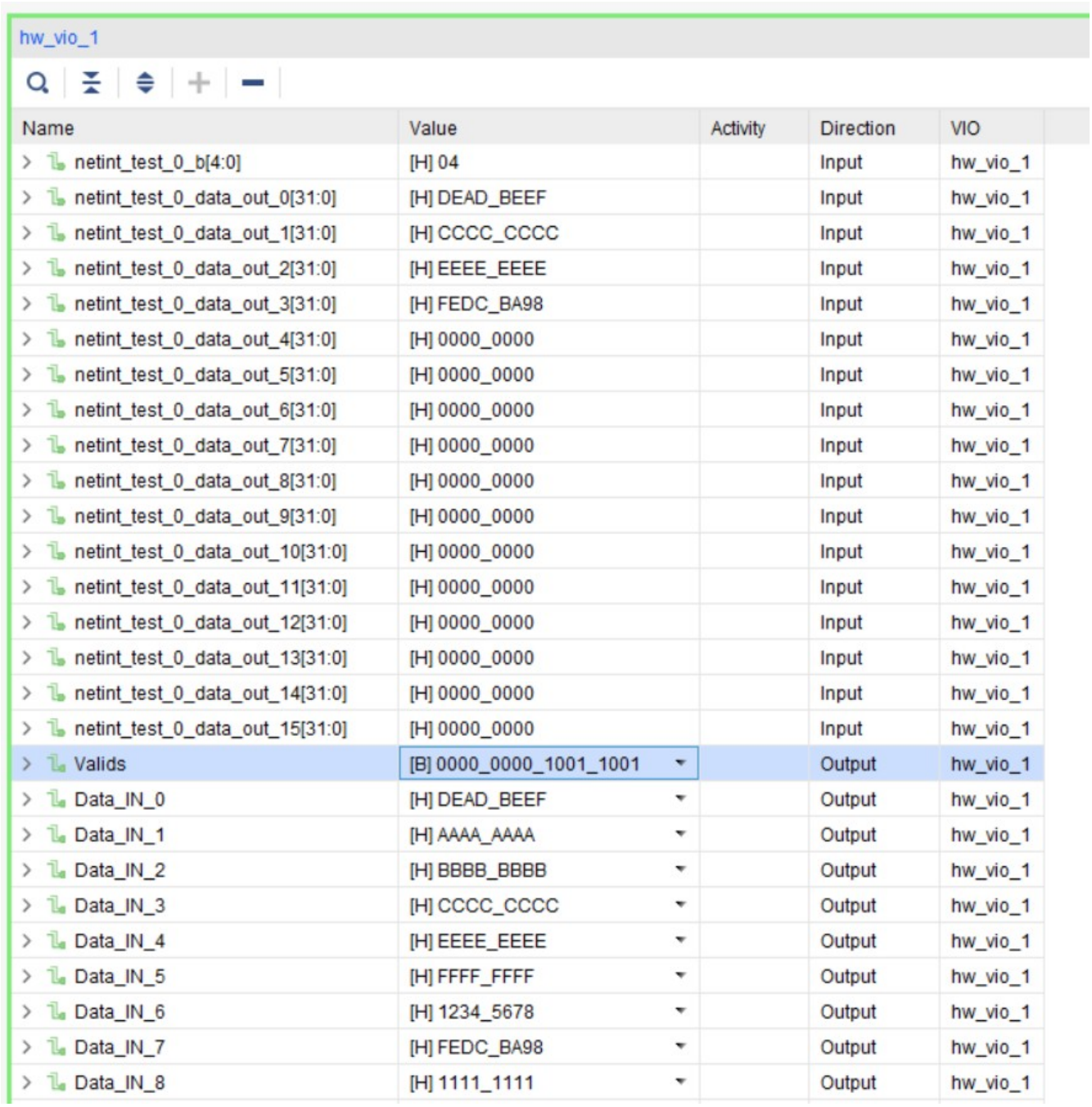
I implemented this design on an Arty board. This board has an Artix-7 XC7A35T FPGA on it. To test the design I connected each input and output to a Xilinx Virtual Input Output (VIO). (See figure below) With a system clock of 100MHz.



This design used 2189 LUTs, and 517 Registers. (See utilization below)

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)
design_1_wrapper	12908	13764	292	96	4329	11608	1300	5784
dbg_hub (dbg_hub)	473	727	0	0	211	449	24	302
design_1_i (design_1)	12435	13037	292	96	4163	11159	1276	5458
axi_uartlite_0 (design_1_axi_uartlite_0_0)	97	105	0	0	39	87	10	63
clk_wiz_0 (design_1_clk_wiz_1_0)	0	0	0	0	0	0	0	0
mdm_1 (design_1_mdm_1_0)	85	109	0	0	43	78	7	39
microblaze_0 (design_1_microblaze_0_0)	626	332	32	0	208	445	181	175
microblaze_0_axi_periph (design_1_microblaze_...	1707	2630	32	0	778	1357	350	853
microblaze_0_local_memory (microblaze_0_local...	7	4	0	0	6	7	0	1
mig_7series_0 (design_1_mig_7series_0_1)	5863	5034	4	0	1898	5137	726	2383
netint_test_0 (design_1_netint_test_0_0)	2189	517	0	0	662	2189	0	484
rst_CLK100MHZ_100M (design_1_rst_CLK100M...	18	39	0	0	13	17	1	15
rst_mig_7series_0_83M (design_1_rst_mig_7se...	15	33	0	0	10	14	1	13
util_vector_logic_0 (design_1_util_vector_logic_0...	0	0	0	0	0	0	0	0
vio_1 (design_1_vio_1_2)	1830	4234	224	96	1111	1830	0	1290

You can see in the VIO screen shot below that bits 0, 3, 4, and 7 of Valids are set. Register b is showing the value 4, and first 4 buffers have stored the data for Data_IN_0, Data_IN_3, Data_IN_4, and 7.



hw_vio_1

Name	Value	Activity	Direction	VIO
netint_test_0_b[4:0]	[H] 04		Input	hw_vio_1
netint_test_0_data_out_0[31:0]	[H] DEAD_BEEF		Input	hw_vio_1
netint_test_0_data_out_1[31:0]	[H] CCCC_CCCC		Input	hw_vio_1
netint_test_0_data_out_2[31:0]	[H] EEEE_EEEE		Input	hw_vio_1
netint_test_0_data_out_3[31:0]	[H] FEDC_BA98		Input	hw_vio_1
netint_test_0_data_out_4[31:0]	[H] 0000_0000		Input	hw_vio_1
netint_test_0_data_out_5[31:0]	[H] 0000_0000		Input	hw_vio_1
netint_test_0_data_out_6[31:0]	[H] 0000_0000		Input	hw_vio_1
netint_test_0_data_out_7[31:0]	[H] 0000_0000		Input	hw_vio_1
netint_test_0_data_out_8[31:0]	[H] 0000_0000		Input	hw_vio_1
netint_test_0_data_out_9[31:0]	[H] 0000_0000		Input	hw_vio_1
netint_test_0_data_out_10[31:0]	[H] 0000_0000		Input	hw_vio_1
netint_test_0_data_out_11[31:0]	[H] 0000_0000		Input	hw_vio_1
netint_test_0_data_out_12[31:0]	[H] 0000_0000		Input	hw_vio_1
netint_test_0_data_out_13[31:0]	[H] 0000_0000		Input	hw_vio_1
netint_test_0_data_out_14[31:0]	[H] 0000_0000		Input	hw_vio_1
netint_test_0_data_out_15[31:0]	[H] 0000_0000		Input	hw_vio_1
Valids	[B] 0000_0000_1001_1001		Output	hw_vio_1
Data_IN_0	[H] DEAD_BEEF		Output	hw_vio_1
Data_IN_1	[H] AAAA_AAAA		Output	hw_vio_1
Data_IN_2	[H] BBBB_BBBB		Output	hw_vio_1
Data_IN_3	[H] CCCC_CCCC		Output	hw_vio_1
Data_IN_4	[H] EEEE_EEEE		Output	hw_vio_1
Data_IN_5	[H] FFFF_FFFF		Output	hw_vio_1
Data_IN_6	[H] 1234_5678		Output	hw_vio_1
Data_IN_7	[H] FEDC_BA98		Output	hw_vio_1
Data_IN_8	[H] 1111_1111		Output	hw_vio_1