THE UNIVERSITY OF MELBOURNE

Semester 1 Assessment, 2021

Department of Electrical and Electronic Engineering
ELEN90066 Embedded System Design

Writing time: 180 minutes
Reading time: 15 minutes
Scanning and submission time: 30 minutes
TOTAL time: 225 minutes

This paper has 13 pages

Authorised materials:

This is an open book, hand-written exam and the following materials are permitted:

- Any material loaded onto Canvas as part of the subject content.
- Notes (printed, hand-written and digital/electronic).
- Online books and materials .
- Language dictionaries.
- Calculators (any model), computers, electronic tablets, pens, rulers, etc.

Instructions to students:

- Attempt **ALL** questions.
- The questions carry weight in proportion to the marks in brackets after the question numbers. These marks total **100 marks**.
- All answers on this exam must be handwritten (whether using pen and paper or a tablet).
- All working must be scanned and submitted to Gradescope before the end of the exam time. Ensure your student number is written on each answer page that you upload.
- Submission time is reserved for scanning and uploading. It is your responsibility to submit within the allocated submission time and late submissions will attract a penalty. If you have difficulties in submitting your answers, inform your Subject Coordinator immediately.
- Any updates to the exam will be made via Canvas announcements during the examination time.
- Collusion is **not allowed under any circumstances**. Collusion includes, but is not limited to, talking to, phoning, emailing, texting or using the internet to communicate with other students. Similarly, you cannot communicate with any other person via any means about the content of this exam during the examination time. If another student contacts you during the examination period, please inform the subject coordinator immediately.
- Plagiarism, through the use of sources without proper acknowledgement or referencing, **is not permitted** and can attract serious penalties. Plagiarism includes copying and pasting from the Internet without clear acknowledgement and paraphrasing or presenting someone else's work as your own. Note that this definition also applies to work completed during the semester as part of a group. All responses to this exam paper must be entirely your own work, unless otherwise acknowledged.

Question 1 (12 marks)

Consider a system comprising a device that acts as a data source and another device that acts as a data sink as shown in Figure 2 below:

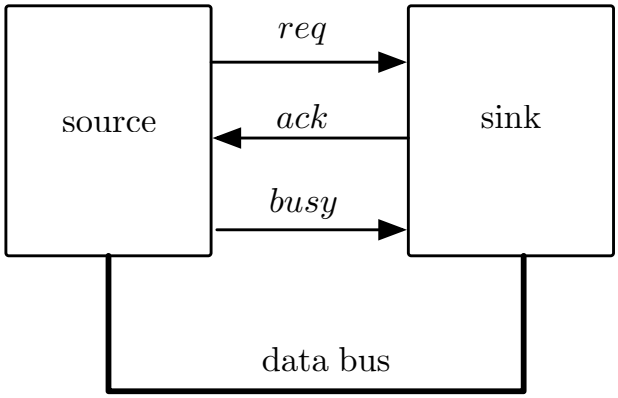


Figure 1: Data source and sink for Question 1

The devices are connected to a data bus in order to facilitate the transfer of data from source to sink. The source device has two output control signals, **req** and **busy** which are connected as inputs to the source device. The sink has one output control signal, **ack**, which is connected as an input to the source device.

All input and output control signals are of type *pure*. Note that the data bus signals are not part of the control mechanism of either device and can therefore be ignored for the remainder of this question.

Assuming the data bus is idle, the transfer of data is initiated by the source by setting the **req** signal to be present. The following process is then followed:

- The sink responds to the **req** signal being present by setting the **ack** signal to be present when it is ready to receive data.
- The source then takes control of the data bus, releases the **req** signal, and sets the **busy** signal to be present while the data transfer takes place. The sink begins capturing the data and removes the presence of the **ack** signal.
- Once the data transfer has finished, the source removes the **busy** signal and the sink then processes the data.
- If another request for data transfer from the source comes in while the sink is still processing data, the sink will remember the pending request and service it as soon as it has finished processing the current data.
- If another request for data transfer from the source comes in after the sink has processed all data, the process above is repeated.

Question 1 (continued)

(a) [**4 marks**] Draw a Finite State Machine representing the operation of the **source** device with:

input: *ack* : pure
outputs: *req*, *busy* : pure

(b) [**4 marks**] Draw a Finite State Machine representing the operation of the **sink** device with:

inputs: *req*, *busy* : pure
output: *ack* : pure

(c) [**4 marks**] Draw a Finite State Machine representing the synchronous composition of the source and sink Finite State Machines.

Question 2 (13 marks)

Consider a system modelled by the following Finite State Machine (FSM)

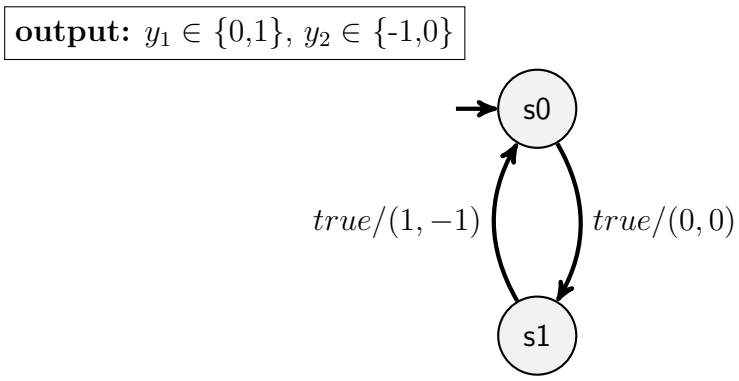


Figure 2: FSM for Questions 2 (a) and 2 (b)

The output expressions in the above FSM diagram are given as the pair (y_1, y_2).

(a) **[2 marks]** Give an *execution trace* of the Finite State Machine.

(b) **[8 marks]** For each of the following LTL formulae, determine whether it is TRUE or FALSE for the FSM above. You **MUST** give an explanation for your answer. If FALSE, give a counterexample.

(i) $\mathbf{G}(y_1 > 0)$

(ii) $\mathbf{F}(y_1 \leq 0)$

(iii) $\mathbf{FG}(y_2 \leq y_1)$

(iv) $\mathbf{GF}(y_2 = y_1)$

(v) $\mathbf{FG}(|y_1 - y_2| \leq 1)$

(vi) $(y_2 \leq y_1)$

(vii) $(y_2 \leq y_1)\mathbf{U}(y_2 = 2)$

(viii) $(|y_1 - y_2| \leq 1)\mathbf{U}(|y_1 - y_2| = 2)$

(c) **[3 marks]** Are the following two relations equivalent, where p is an LTL formula?

$$\neg\mathbf{X}p \qquad \text{and} \qquad \mathbf{X}\neg p$$

Prove your answer.

Question 3 (14 marks)

Consider a model of a *synchronous buffer* that accepts integers in the range $[0, 127]$, via an input port `in`, and outputs them via an output port `out` after a certain delay. A block diagram of the inputs and output of the buffer is shown in Figure 3.

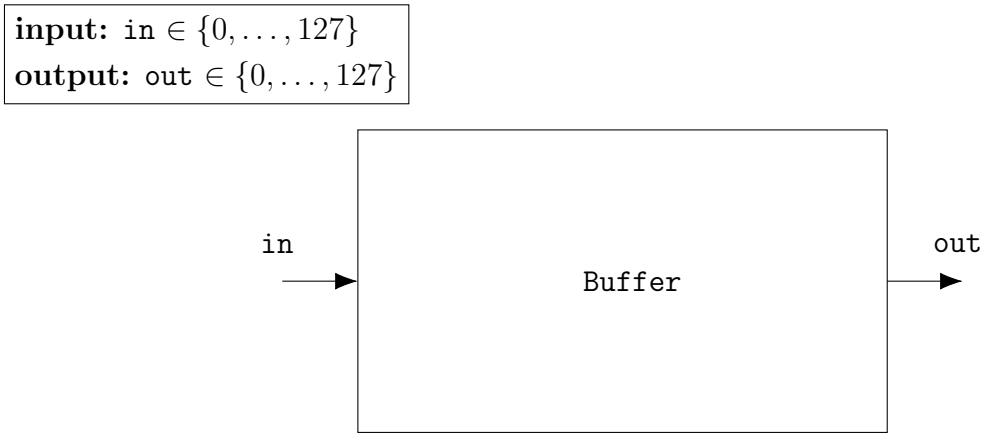


Figure 3: Synchronous buffer for Question 3

The buffer is time triggered – that is, it reacts *once* on every positive edge of a periodic clock signal (not shown on the block diagram). The buffer has a capacity of one integer, so that whenever an input value is supplied to the empty buffer it is stored in an internal memory, causing the buffer to be full. When the buffer is full, it simply ignores (or loses) further inputs until it gets a chance to output the stored value to the output `out`.

The delay between the reception of an input value and the transmission of the corresponding output value is at least `LB` and at most `UB` time units, respectively. In other words, the buffer can produce the output only after the *lower bound* `LB` (time units) on the delay and is guaranteed to produce the output within the *upper bound* `UB` (time units) of receiving an input. It is assumed that each time unit is equal to one clock cycle.

(a) [**5 marks**] Draw an Extended Finite State Machine modelling the behaviour of the synchronous buffer as described above. You can consider the buffer to have two states, `Empty` and `Full`. Be sure to list any variables defined as part of the machine.

Question 3 (continued)

(b) **[6 marks]** Consider two instances of the synchronous buffer connected in parallel as shown in Figure 4.

input: `in` $\in \{0, \ldots, 127\}$
output: `out1, out2` $\in \{0, \ldots, 127\}$

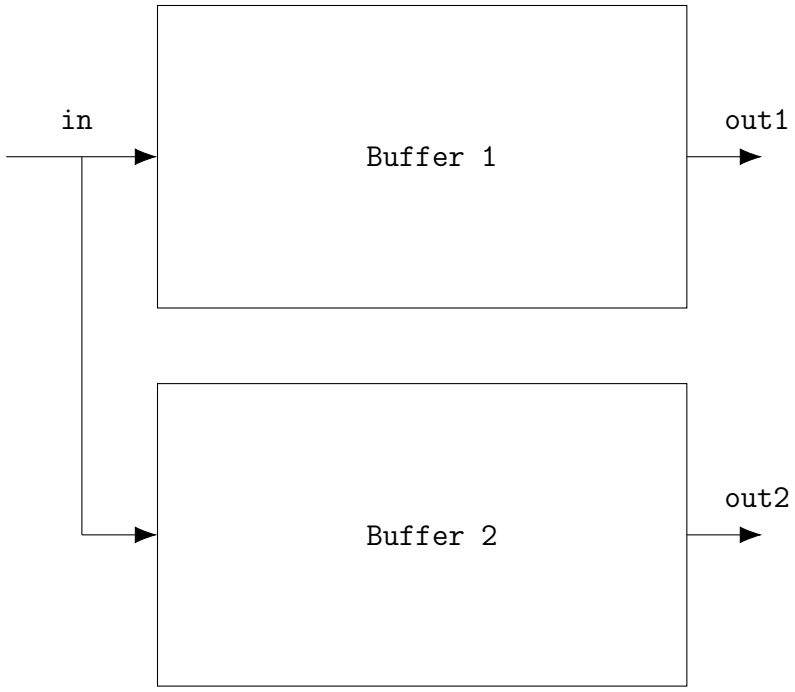


Figure 4: Synchronous buffers in parallel

The delay between the reception of an input value and the transmission of the corresponding output value is at least $\texttt{LB}_\texttt{i}$ and at most $\texttt{UB}_\texttt{i}$ time units, respectively, for each buffer, where $i \in \{1, 2\}$ refers to the buffer number.

Draw the Extended Finite State machine resulting from this composition. Be sure to list any variables defined as part of the composed machine.

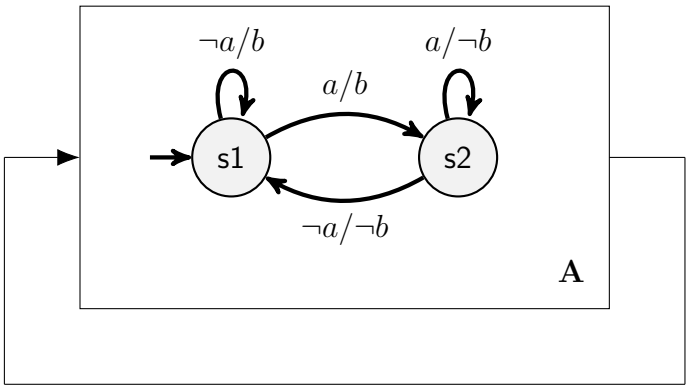
(c) **[3 marks]** Assume that $\texttt{UB}_1 < \texttt{LB}_2$ for the composition in Figure 4. Does this assumption always guarantee that the first component produces its output before the second? Explain your answer, either by providing a proof or a counterexample.

Question 4 (14 marks)

For all compositions in this question, you are to assume a Synchronous Reactive Model of Computation.

(a) **[2 marks]** Consider a system **A** modelled by the following Finite State Machine (FSM):

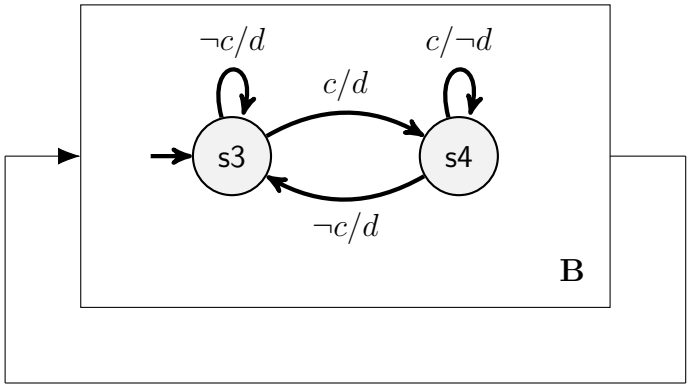
input: a :pure
output: b :pure



Is the feedback composition is well-formed? Explain your answer.

(b) **[2 marks]** Consider a system **B** modelled by the following Finite State Machine (FSM):

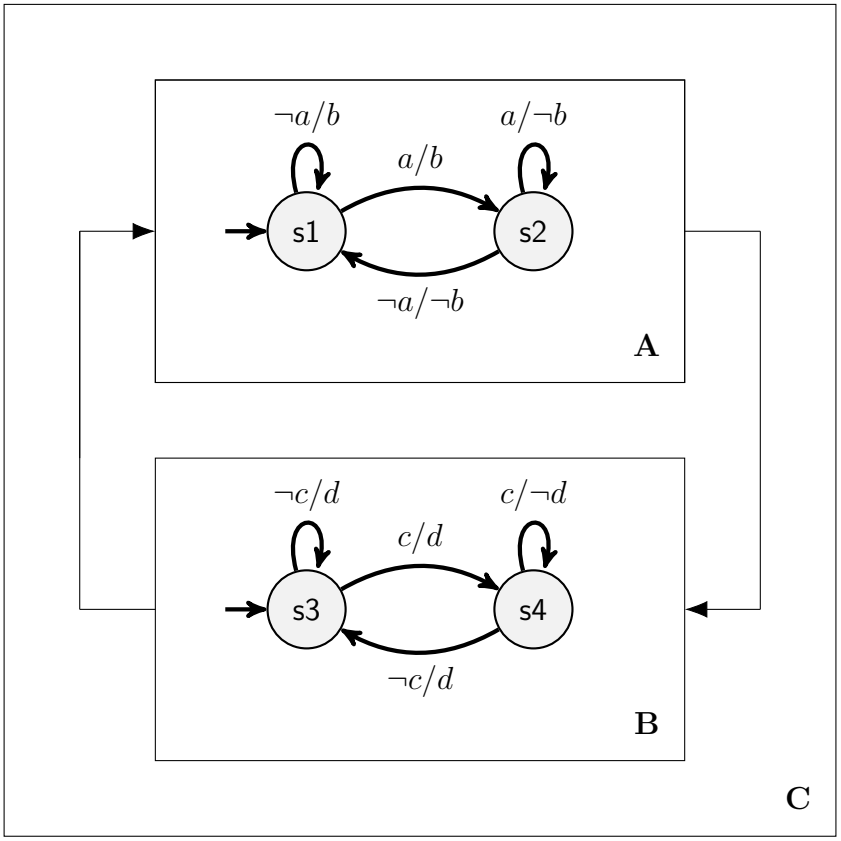
input: c :pure
output: d :pure



Is the feedback composition is well-formed? Explain your answer.

Question 4 (continued)

(c) **[4 marks]** Consider the system **A** combined with system **B** in a feedback composition as shown below to form system **C**. Note that the output port of **B** is drawn on the left and the input port on the right for convenience.

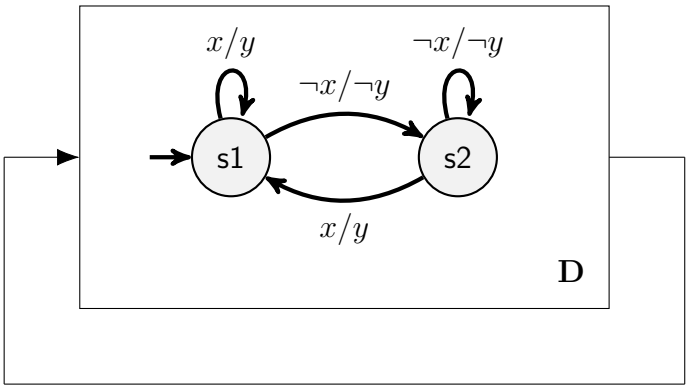


Show that feedback composition **C** is well-formed, and draw the Finite State Machine model for the composite system.

Question 4 (continued)

(d) **[6 marks]** Consider the machine **D** below

input: x :pure
output: y :pure



Redraw this feedback composition as a non-deterministic state machine so that it is no longer ill-formed but yields identical output behaviour.

Give the set theoretic description for the composed machine, that is the 5-tuple:

$$(States, Inputs, Outputs, update, initialState)$$

Question 5 (16 marks)

Consider six tasks τ_1, ..., τ_6 with release times, execution times, and deadlines presented below.

	τ_1	τ_2	τ_3	τ_4	τ_5	τ_6
release time, r_i	0	2	5	4	1	2
execution time, e_i	3	2	2	3	1	3
deadline, d_i	8	8	13	10	6	14

We say task τ_i precedes task τ_j if the predecessor must complete the execution of τ_i before τ_j can execute. The precedence relationships between tasks τ_1, ...,τ_6 are as the following

- τ_1 precedes τ_3;
- τ_1 precedes τ_4;
- τ_2 precedes τ_4;
- τ_2 precedes τ_5;
- τ_3 precedes τ_6;
- τ_4 precedes τ_6;
- τ_5 precedes τ_4.

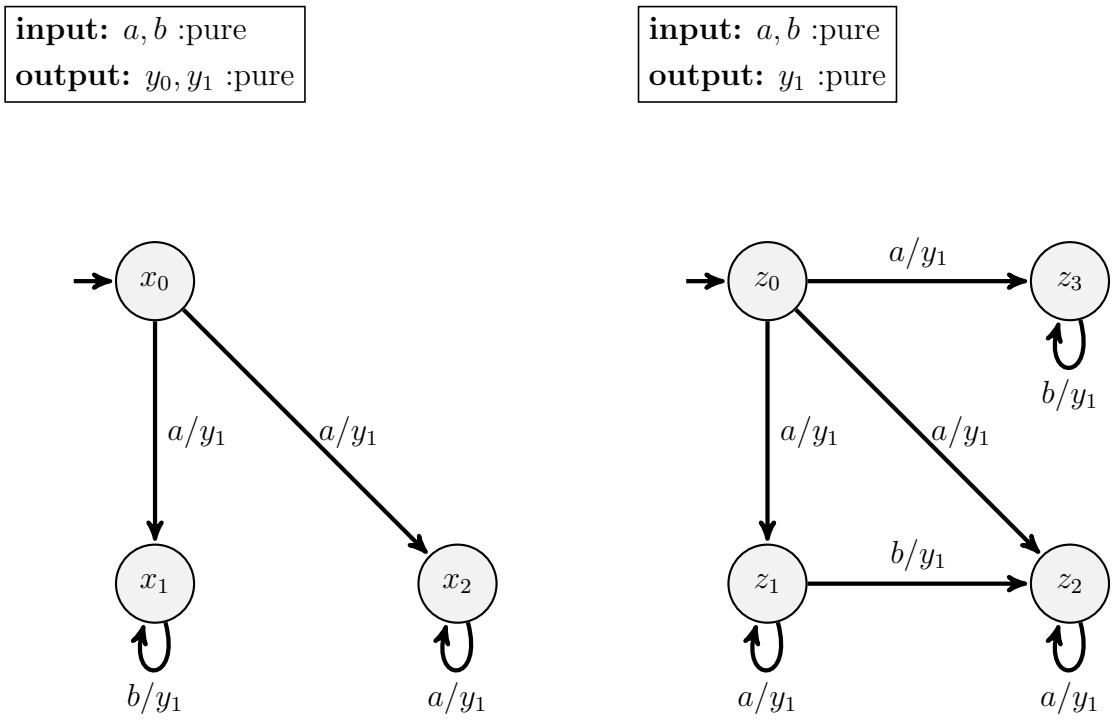
(a) [**4 marks**] Draw the directed acyclic graph representing the precedence of the tasks where a directed edge marks a precedence.

(b) [**4 marks**] Does a scheduling approach based on Latest Deadline First (LDF) yield a feasible deadline? Explain why if the answer is no, and construct the schedule if the answer is yes.

(c) [**8 marks**] Does Earliest Deadline First with Precedence (EDF*) yield a feasible schedule? Explain why if the answer is no, and construct the schedule if the answer is yes.

Question 6 (10 marks)

Consider Finite State Machines Σ_1 and Σ_2 depicted in Figure 5.



(a) System Σ_1 (b) System Σ_2

Figure 5: Systems Σ_1 and Σ_2 for Question 6.

(a) [**5 marks**] Is Σ_1 simulated by Σ_2? Prove your answer.

(b) [**5 marks**] Is Σ_2 simulated by Σ_1? Prove your answer.

Question 7 (12 marks)

Figure 6 depicts the area of operation of a robot. The red line depicts its path as it starts its motion from region R_0 and exits the area from the left edge. Let logical propositions r_i correspond to the robot being in regions R_i where $i \in \{1, 2, \ ..., 14\}$.

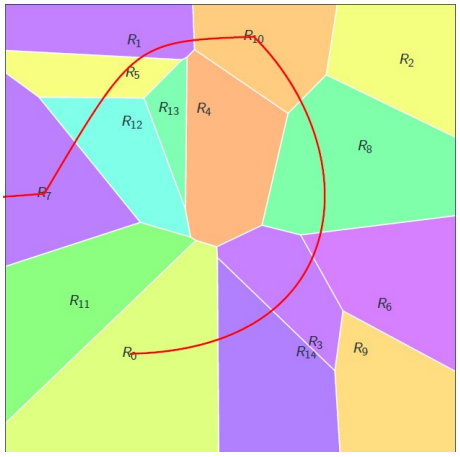


Figure 6: Area of operation of the robot of Question 7.

(a) [**4 marks**] What does the LTL formula ϕ as defined below mean? Provide both a natural language translation, and an interpretation, of the specification.

$$\phi := r_i \wedge \mathbf{F} r_7 \wedge \mathbf{F} r_{10} \wedge \mathbf{G} \neg r_4$$

(b) [**3 marks**] Does the robot meet specification ϕ? Explain.

(c) [**5 marks**] Consider the case where the aim of the robot is to exclusively visit regions R_{14}, R_3, R_4, R_8, R_2 and remain in R_2 after starting its motion from R_0. Write this as an LTL specification.

Question 8 (9 marks)

(a) **[4 marks]** The Sharp GP2Y0A02YK0F Infra Red (IR) sensor modelled in workshops has an output voltage level that is non-linear according to the diagram in Figure 7.

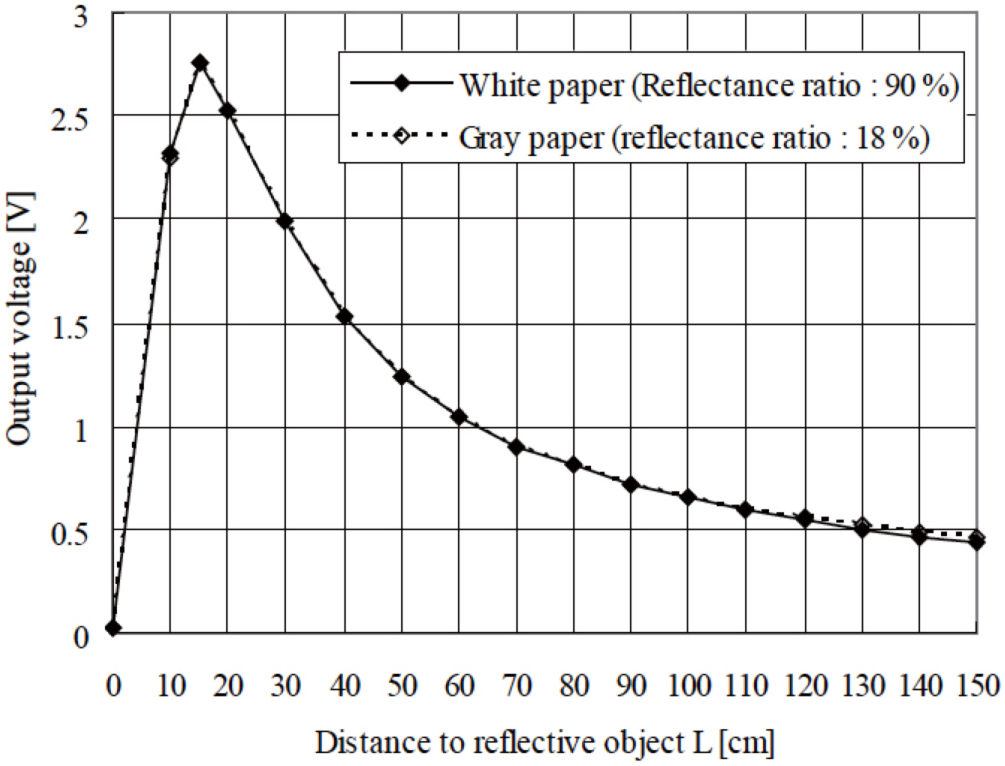


Figure 7: Distance measuring characteristics (output, GP2Y0A02YK0F)

Assuming an *affine* model for the sensor, and choosing an appropriate operating range, estimate the *bias* and *sensitivity* parameters of the sensor. Provide all calculations.

(b) **[2 marks]** Assume now that the output terminal voltage of the IR sensor can range between 0V and 2.85V. The output signal from the IR sensor is converted to a 10-bit binary number via an Analog to Digital Converter for use in an obstacle avoidance algorithm by dividing this voltage range into *equally spaced* voltage steps. What is the precision and dynamic range (dB) of the sensor?

(c) **[3 marks]** Name an additional sensor you would add to the Kobuki robot in order for it to perform better with either obstacle avoidance or hill climbing / descending? Explain how the sensor data would be used by your main navigation algorithm.

END OF EXAMINATION