Question 1 Source input: ack: pure output: req, busy: pure 7ack/reg true true/rea idle init true 17 busy ack/Treg, busy Send true/busy

Sink input: reg, busy: pure cutput: ack: pure real ack reg/ack idle listen true lack, Wait Treg 1 busy/Tack proces (receive) true

Composition true true Tidle, idle init, listery truel Truel in't wait send, receive July idle process true true