Embedded Pico Systems

Design Guide

Timing Controller – Generation 2 for Pervasive Displays 4.41″ Panel

TC2-P441-231_v1.1

Classification: **Confidential**

Document Revision: **A**

Table of Contents

1 Pinout

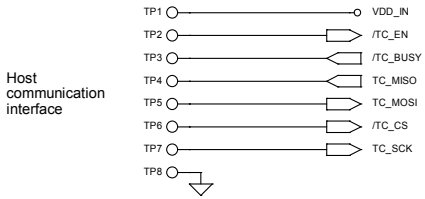
NOTE Forward slash "/" in front of the pin name indicates the signal is active low.

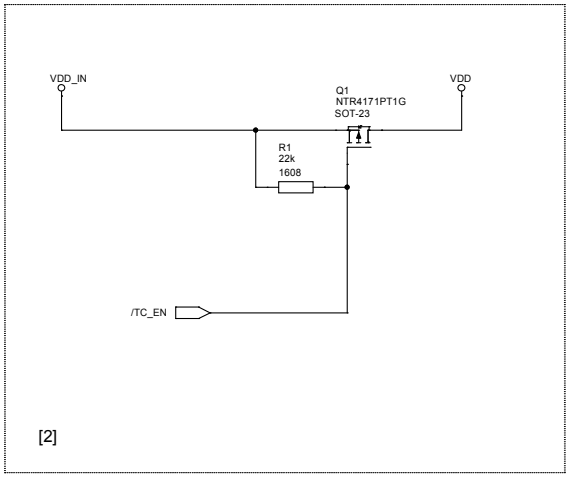
No.	Pin Name	Remarks
1	FLASH_HOLD	External flash hold output
2	DISCHARGE_VDL (TC_BOOT)	Charge pump negative voltage discharge output Bootloader input – connect to test point or 4-pin header
3	/TC_RESET	Bootloader input – connect to test point or 4-pin header
4	TC_TXD	Bootloader data output – connect to test point or 4-pin header
5	/SPI_FLASH_CS	External flash chip select output
6	n/c	Leave open
7	n/c	Leave open
8	DISCHARGE_VCC	Display VCC voltage discharge output
9	/TC_BUSY	Host interface busy output
10	TC_MISO	Host interface data output
11	TC_MOSI	Host interface data input
12	/TC_CS	Host interface chip select input
13	TC_SCK	Host interface clock input
14	DISCHARGE_VDH	Charge pump positive voltage discharge output
15	n/c	Leave open
16	n/c	Leave open
17	n/c	Leave open
18	DC_PWR_EN	Display VCC voltage enable output
19	VDD	Digital power supply input
20	VREFN	Analog power supply ground
21	VREFP	Analog power supply input
22	ADC_TEMP	Temperature sensor measurement input
23	DISP_/RESET	Display source driver reset output
24	TC_RXD	Bootloader data input – connect to test point or 4-pin header
25	SPI_MISO	Serial interface data input
26	SPI_MOSI	Serial interface data output
27	SPI_SCK	Serial interface clock output
28	/SPID_DISP_CS	Display chip select output
29	DISP_OE1	Display gate driver OE output
30	DISP_CLKG	Display gate driver clock output
31	DISP_STV_IN	Display source driver start pulse output
32	DISP_STV_OUT	Display source driver start pulse input
33	VSS	Digital power supply ground (exposed pad)

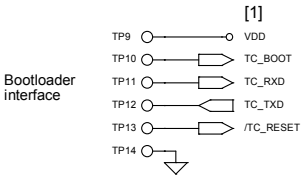
/TC_RESET, TC_BOOT, TC_RXD and TC_TXD are the bootloader interface pins. Although firmware upgrade by the user is not supported at this stage, it is advised to connect this interface to test points or a connector to allow taking advantage of this functionality in the future.

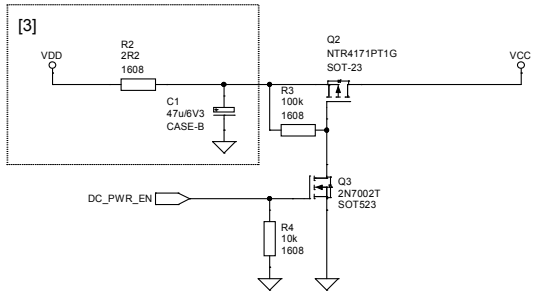
2 Reference Design

Schematic









Note	Description
[1]	VDD requirements
[2]	Power switch proposal
[3]	Peak current suppressor

Signal	Source	Voltage
VDD_IN	External	2.7-3.6V
VDD	Internal	2.7-3.6V
VCC	Internal	2.7-3.6V

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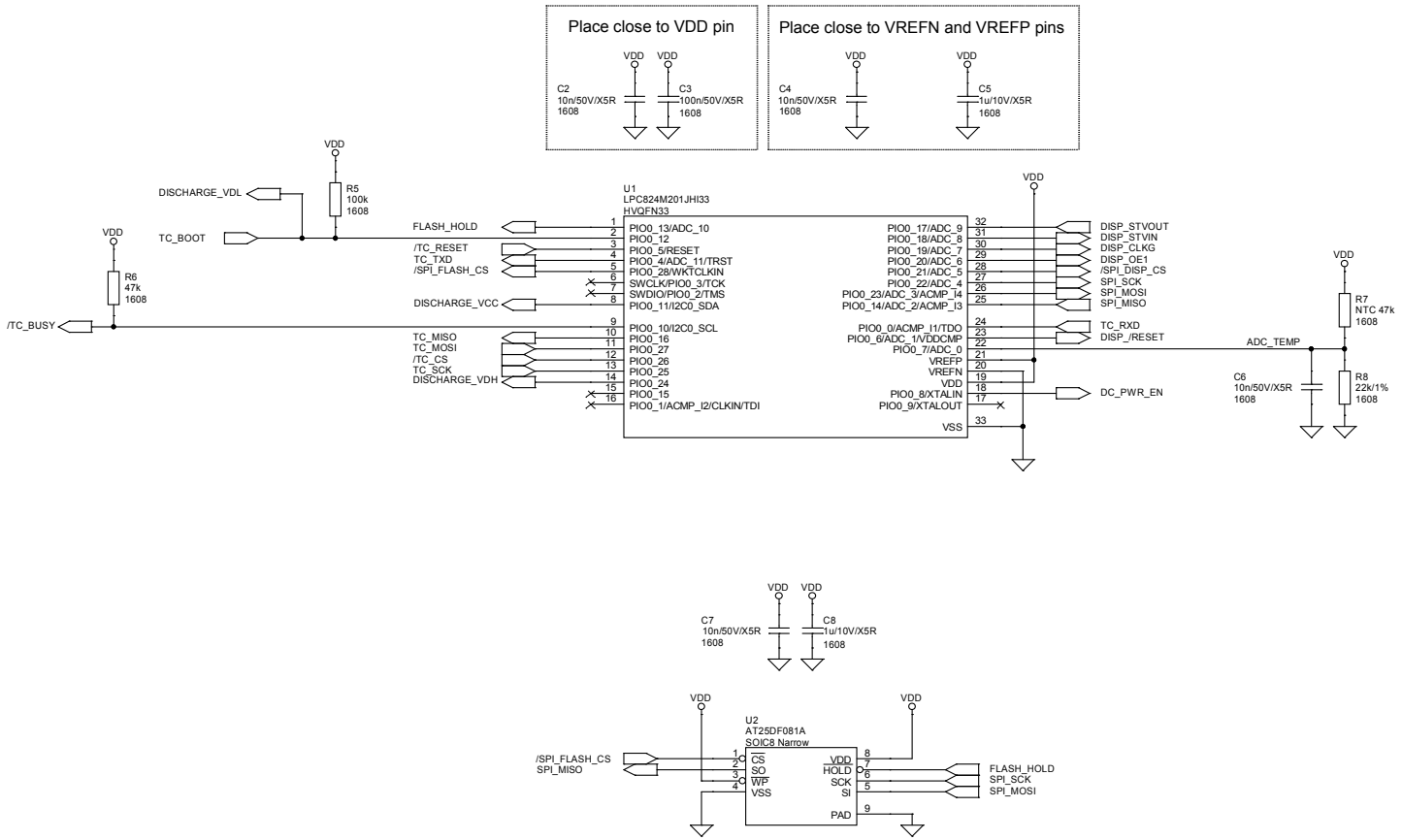
Name: TCon Gen2 Pervasive 4.41" Reference Design						
Code: TC2-P441-RD						
Class: Development						
Created by: PJ	Stage: Blue	Status: Aproved	Reference No.: 2064/15-PJ		Rev: A	Var: 1
Verified by: AK,MP	Date: Friday, December 04, 2015		Page Name: PWR_CON	Page Size: A3	Page No.: 1 of 3	



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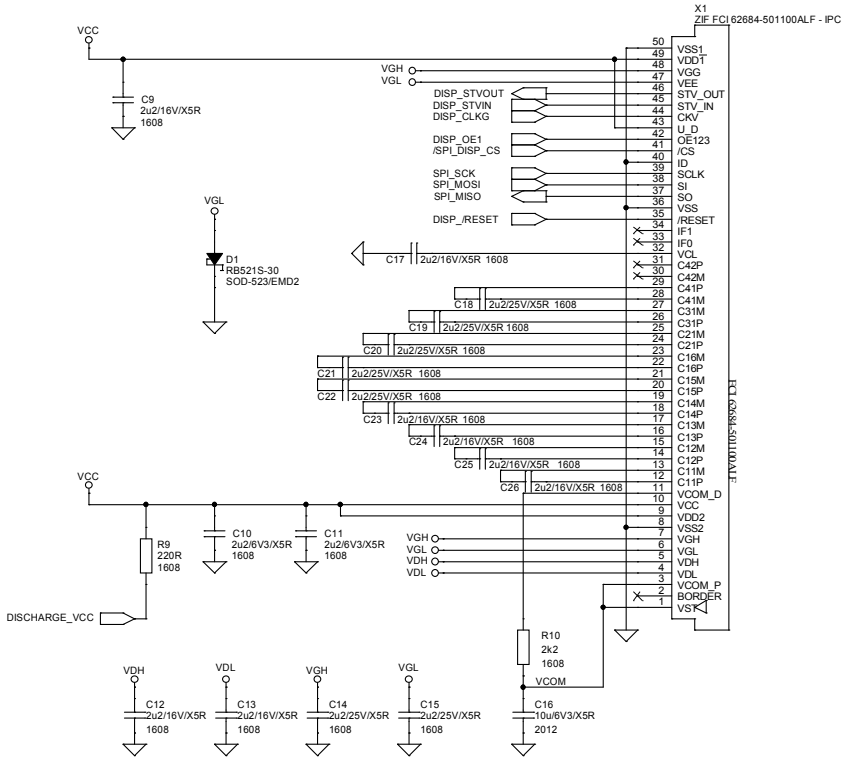
Created by: PJ	Stage: Blue	Status: Aproved	Reference No.: 2064/15-PJ		Rev: A	Var: 1
Verified by: AK,MP	Date: Friday, December 04, 2015		Page Name: LOGIC	Page Size: A3	Page No.: 2 of 3	



Signal	Source	Voltage
VDD	Internal	2.7-3.6V
VCC	Internal	2.7-3.6V
VCOM	Internal	-1.8V
VDH	Internal	14V
VDL	Internal	-14V
VGH	Internal	19V
VGL	Internal	-19V

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Created by: PJ	Stage: Blue	Status: Aproved	Reference No.: 2064/15-PJ		Rev: A	Var: 1
Verified by: AK,MP	Date: Friday, December 04, 2015		Page Name: DISPLAY	Page Size: A3	Page No.: 3 of 3	

Bill Of Materials

#	Reference Designator	Value	Package	Manufacturer Part #	QTY	Notes
1	C1	47uF/6V3	CASE-B	TM3B476K6R3CBA	1	
2	C2,C4,C6,C7	10nF/50V/X5R	1608	VJ0603Y103KXAAC	4	This MPN is X7R
3	C3	100nF/50V/X5R	1608	C1608X7R1H104K080AA	1	This MPN is X7R
4	C5,C8	1uF/10V/X5R	1608	GRM188R61E105KA12D	2	This MPN is 25V
5	C9,C12,C13,C17,C23,C24, C25,C26	2.2uF/16V/X5R	1608	C1608X5R1C225M	8	
6	C10,C11	2.2uF/6V3/X5R	1608	C1608X5R1C225M	2	This MPN is 16V
7	C14,C15,C18,C19,C20,C21, C22	2.2uF/25V/X5R	1608	GRM188R61E225KA12D	7	
8	C16	10uF/6V3/X5R	2012	CC0805KRX5R5BB106	1	
9	D1	RB521S-30	SOD-523	RB521S-30TE61	1	Possible replacement: Schottky diode with Ir<30uA Vrrm>25V
10	Q1,Q2	NTR4171P	SOT-23	NTR4171PT1G	2	Only this MPN
11	Q3	2N7002T	SOT523	2N7002T-7-F	1	
12	R1	22kR	1608	ERJ-3GEYJ223V	1	
13	R2	2.2R	1608	ERJ-3GEYJ2R2V	1	
14	R3,R5	100kR	1608	CRCW0603100KJNEA	2	
15	R4	10kR	1608	CRCW060310K0JNEA	1	
16	R6	47kR	1608	ERJ-3GEYJ473V	1	
17	R7	NTC 47kR (B=4030K)	1608	NCP18WB473E03RB	1	Only this MPN
18	R8	22kR/1%	1608	CRCW060322K0FKEA	1	
19	R9	220R	1608	ERJ-3GEYJ221V	1	
20	R10	2.2kR	1608	ERJ-3GEYJ222V	1	
21	U1	TC2-P441	HVQFN33	TC2-P441-231_v1.1	1	Only this MPN
22	U2	AT25DF081A	SOIC8	AT25DF081A-SSH	1	Possible replacements: A25L020CO-F
23	X1	FCI 62684-501100ALF	N/A	62684-501100ALF	1	Possible replacement: FH28E-50S-0.5SH(05)

Table 2.1: TC2-P441-231_v1.1 Reference Design Bill of Materials

2.1 Notes

This section elaborates on the notes found on the schematics.

[1] VDD Requirements

VDD has to be supplied from a stable power supply in the range of 2.7V to 3.6V. An example solution based on MCP1623 Low-Voltage Input Boost Regulator is shown on the Figure 2.1 below. Please note the example is provided as a guidance only, that can be referred to if the power supply provided by the host is not stable or below operating range.

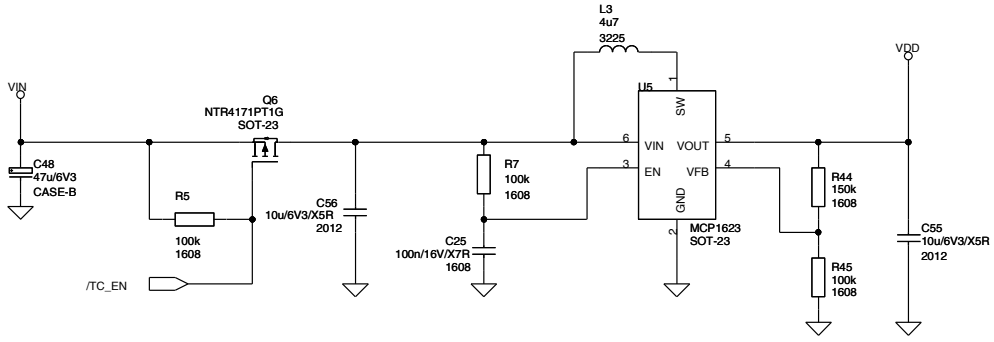

Figure 2.1: VDD stabilization example

[2] Power Switch Proposal

It is recommended to use an analog switch for the system to conserve the battery energy. The switch is driven by /TC_EN signal (active low) that has to be provided by the host.

[3] Peak current suppressor

Current peaks appear on the display power supply VCC during charge pump start. If the application works from small coin cells batteries it is advised to design the peak current suppressor built from C1, R2 components.

2.2 Additional Board Layout Guidelines

- SPI_SCK, SPI_MOSI, and SPI_MISO should be laid out on top of the ground plane. No other signal line should lead along the above mentioned lines, in close proximity.
- The trace between C1 capacitor, through Q2 transistor source, to VCC, should be kept thick and straight to ensure low resistance and inductance.
- C46 capacitor and Q2 transistor should be placed close to the display VCC input voltage (close to C10 and C11 capacitors).
- C2, C3 decoupling capacitors should be grouped in a pair and connected between the TC pins VDD and VSS with as short trace as possible. The 10nF capacitor should be placed closer to the VDD pin than the 100nF capacitor.

- C4, C5 decoupling capacitors should be grouped in a pair and connected between the TC pins VREFP and VREFN with as short trace as possible. The VREFN should be connected directly to the TC exposed ground pad (pin 33), and VREFP with the TC supply VDD with a short trace. The 100nF capacitor should be placed closer to the VREFP pin than the 1uF capacitor.
- C9, C10, C11, C12, C13, C14 and C15 decoupling capacitors should be placed close to the X1 ZIF connector.
- C16, C17, C18, C19, C20, C21, C22, C23, C24, C25 and C26 charge pump capacitors should be placed close to the X1 ZIF connector with maximum 20 mm long traces.
- Node between the TC pin 22, R7, R8 resistors, and C6 capacitor is noise sensitive. It is recommended to keep this node area small and place the C6 capacitor close to the TC pin 22. C6 capacitor ground should be well connected with TC ground (low impedance.)

3 Revision History

Document Revision	Release Date	Document Status	Supersedes
A	2015-12-04	Approved	–

Table 3.1: Revision history

Document Revision	Change Log
A	Initial version

Table 3.2: Change log

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