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DIGITAL AUDIO
dynamic range control of digital audio signals

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DIGITAL AUDIO : DYNAMIC RANGE CONTROL OF DIGITAL AUDIO SIGNALS

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Summary

Digital methods for control of the dynamic range of digitally coded audio signals are described. Block diagram representations are given for both the realisation of static and dynamic characteristics of a dynamic range controller. The methods for calculating coefficients representing the controlling parameters are derived and the effect of restricting the accuracy of the processing by the use of fixed wordlength arithmetic is examined. One form of distortion introduced because of this restricted accuracy processing can be described as 'zipper' noise and was successfully removed by adaptive smoothing of the gain control signal. The techniques were verified using a high speed audio signal processor, COPAS–2, thereby confirming that practical real-time digital dynamic range control is feasible.

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1. Introduction

Dynamic range control (DRC) devices have been used for many years both for the protection of equipment from overload, and also for artistic purposes. The aim of such a device is to increase or decrease the dynamic range of an audio signal in a prescribed way without introducing perceptible distortion. Conventionally, such devices have been constructed using analogue technology and demanded skilful design to meet tight specifications. This Report describes methods for producing these effects using digital techniques where, in principle, the accuracy of the processing is only limited by the digital wordlengths used. For this reason, the effects of limiting the accuracy of digital arithmetic at various stages in the processing are covered in some detail. The experimental work was undertaken on a BBC–designed programmable audio signal processor, COPAS –2. A companion Report[1] discusses the hardware and programming methods for this digital signal processor. This was programmed to realise a combined expander/compressor/limiter in real-time and provided the means for verifying the techniques used. This DRC includes signal detection by either peak or rms content; a delay which can be used to eliminate overshooting; and adaptive filtering of the control signal to ensure smooth variations in gain. All the parameters for the DRC are variable and in the experimental equipment a standard interface (IEEE–488) linked to a desktop computer provided a versatile method for controlling these parameters. The digital processing required for these operations is well within the range of modern digital hardware and used less than 25% of the computing power of the COPAS–2 equipment.

2. Discussion of current analogue techniques for dynamic range control

One of the first applications of dynamic range control of audio signals in broadcasting was to the protection of transmitters against overload. It is necessary to modify the dynamic range of the broadcast signal because the channel has a defined peak limit at which severe distortion and overload can occur, and a lower limit determined by noise. Usually, the dynamic range of the source material may be expected to be greater than that of the broadcast channel and therefore some kind of gain control must be used to maximise the service area without overloading the transmitter. With manual control it is inevitable that occasional overload will occur on unexpected programme peaks; without it, sustained quiet passages will be spoiled by channel noise. A DRC is an automatic gain control device which modifies the dynamic range without introducing perceptible distortion.

A limiter is one such device which has been developed for specific broadcasting applications.[2,3] They have also been used to prevent overcutting in the preparation of audio discs and to control levels before analogue to digital conversion.

In the circumstances described above the limiter is only active for a small proportion of the time. In other cases a compressor may be used to effect a larger change to the dynamic range by being active over a wider range of input signal levels. For example, compressors have been used for a long time to match the relatively wide dynamic range of sound-programme signals to the much narrower dynamic range of AM radio transmissions. In a multi-track recording studio, tape hiss, hum and other low level interference can add up to intolerable levels if precautions are not taken in controlling the dynamic range of the material to be recorded. A compresssor can also be used to smooth out the variations in level caused when a vocalist moves toward and away from the microphone or to create special effects by altering the natural decay characteristic of an instrument such as a guitar. By using a pre-emphasis network ahead of the compressor, the device can be made especially sensitive to high frequency or sibilant sounds in speech or vocal tracks, and so remove the phenomenon of 's–blasting'. (Such a device is often termed a 'de–esser').

A third class of dynamic range control devices achieves the opposite effect to compressors. Expanders and noise gates, when used carefully, can generate a more acceptable dynamic range

* COPAS is an acronym denoting COmputer for Processing Audio Signals

from heavily compressed input. This feature is the basis for many noise reduction systems.[4] Noise gates are of particular interest in multi-track recording in which, during track-laying operations, some tracks may have an effective dynamic range of less than 20dB. Sounds picked up at levels lower than this can be regarded as noise and would degrade the quality of the final mixdown. Similarly, where a large measure of compression is applied to a sound signal, a noise gate avoids the amplification of extraneous noises. The noise gate in each case detects low signal levels and attenuates them further so that they do not intrude.

In an audio mixing console it has been customary to provide a small number of versatile dynamic range control devices (between one and four) which may be patched into the appropriate processing channel. The requirements for very low noise and distortion demand very high standards of analogue circuit performance and makes them somewhat expensive pieces of equipment; it is only through the recent advances in the large scale integration of analogue circuits that it has been practical to include a DRC device for every channel.

Fig. 1 illustrates three methods by which dynamic range control can be achieved. The first limiters[2] were constructed in the manner of Fig. 1a and since this is a negative feedback device, it does have the advantage that the exact shape of the control characteristic is unimportant. However, because of delay in the control system, the gain cannot be reduced until after an excessive level has appeared at the output. It is therefore inevitable that overshoots will occur at the output. The alternative input-controlled configuration of Fig. 1b can in principle adjust precisely to the required dynamic range specification for all input level variations, but now demands a precisely specified control characteristic. By using a short preliminary delay, overshoot at the limiter output can be totally eliminated. The attributes of these two methods can be combined as shown in Fig. 1c in which one variable gain element is used in a feedback configuration and the control signal thus derived is applied to a second variable gain element operating on the delayed input signal. In this case, it is not necessary to use variable gain elements with accurately specified gain characteristics but the two elements must be matched, – a much easier task. Modern high performance analogue limiters often use this technique, but the method cannot be easily applied to compressors or expanders. The main technical difficulties in designing this type of unit is the close matching required for the variable gain elements and the high cost of analogue delay lines. These difficulties can be overcome when the signal processing is accomplished digitally.

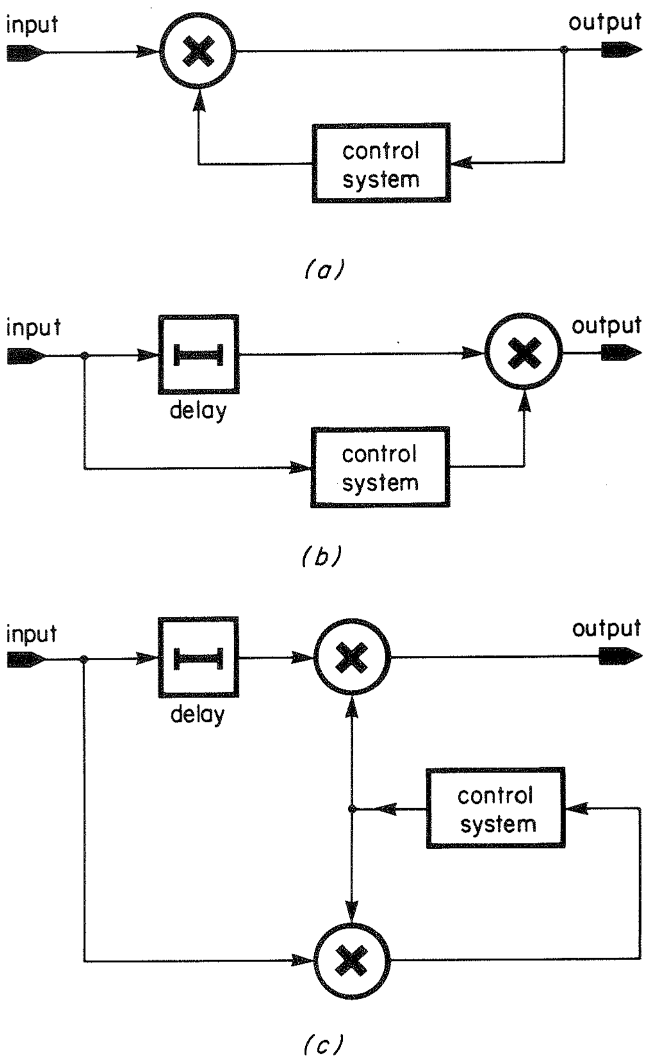

Fig. 1 – Possible limiter configurations

(a) Output controlled, servo feedback type.
(b) Input controlled for feedforward type with preliminary delay.
(c) Feedback limiter with duplicate gain stage and preliminary delay.

3. Dynamic characteristics and their digital realisation

The control system of a dynamic range control device incorporates signal level sensing circuitry. In a protective limiter, these circuits will almost certainly be based on peak detection. In other cases, and in particular for artistic purposes, r.m.s. detection may be used on the assumption that it gives better indication of loudness than either peak or average value. Recently, some manufacturers have used a combination of peak and r.m.s. detection so that, to a certain extent, the peak level of the output can be controlled independently of the loudness.

The performance of a level detector is specified in terms of its transient response, conveniently represented by an attack time, recovery time and, for some applications, a hold time. Choice of these parameters will affect the distortion and noise masking qualities of the DRC.

For the purposes of this Report, attack time, T_a, is defined as the time required for the DRC gain to go from its initial value to within approximately 4 dB (63.2%) of its final value upon sudden application of a transient signal, e.g. a toneburst. In the literature, other definitions are frequently used, and attack time, T_{a90}, has been defined as the time taken to come within 1 dB (90%) of final gain. An IEC Recommendation[5] for automatic gain control devices specifies the time taken after a toneburst is applied for an initial 6 dB overshoot to be reduced to within 2 dB of its final value. This applies to limiters in particular and is illustrated in Fig. 2. In early BBC work on protective limiters, the attack time T_{a12}, was defined as the time taken after a toneburst is applied

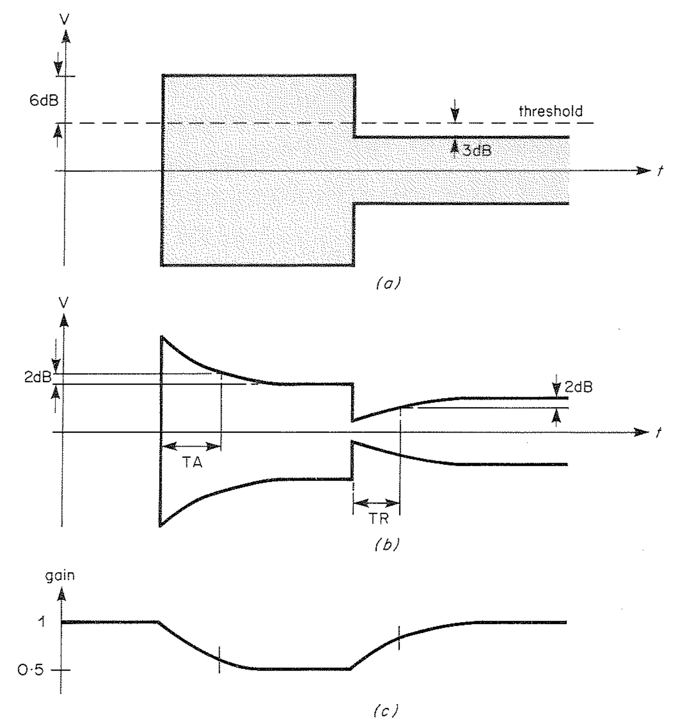

Fig. 2 — Specification of attack and recovery times

(a) Envelope of the input signal

(b) Envelope of the output signal

(c) DRC gain

for an initial 12 dB overshoot at the output to be reduced by 4 dB. This derives from the simplicity of measuring the attack time using a linear display such as an oscilloscope.[2] If the attack characteristics in each case are exponential, then these various attack time definitions are simply related by,

$$T_a = 1.97\ T_{a12} = 0.43\ T_{a90}$$

The recovery time, T_r, which is sometimes referred to as the release time or decay time, is also subject to a range of definitions. Fig. 2 shows that after the application of the tone-burst, a steady state of gain reduction is attained. If the input level is then reduced so that the gain is no longer influenced by the input signal, the IEC Recommendation specifies the recovery time as the time taken for the output level to increase to within 2 dB of its final level, In the more general context of DRC devices described in this Report, the recovery time is defined as the time taken for the gain to reach within 4 dB of its final value when the input signal decreases.

A hold time, T_h, is the time that the DRC gain remains constant after the input signal level decreases. This has been reported to be useful with short recovery times to reduce the audibility of gain changes[4] but is not considered further here.

3.1 Implementation

A digital implementation which permits independent control of attack and recovery times is shown in block diagram form in Fig. 3. Operation of the device is based on a peak-value store which introduces a one-sample delay represented in z-transform notation by z^{-1}: The magnitude of the input is obtained by full wave rectification and is compared with the current value of the peak store. The difference is passed to a non-linear characteristic which has unity gain when the input is greater than the value in the peak store, but is otherwise zero. When the input is greater than the value held in the peak store, a proportion of the difference is added to the peak store. In this way an exponential attack characteristic is obtained with time constant determined by the coefficient, *TA*. A 'leakage' path is provided by the *TR* multiplier which decrements the peak store by a proportion of itself at each sampling instant, so producing an exponential recovery characteristic. For long recovery times, the value of *TR* may be impractically small and so the product is scaled by binary shifting to extend the recovery time. The logarithm of the output is calculated so that the detected signal can be compared with thresholds calibrated

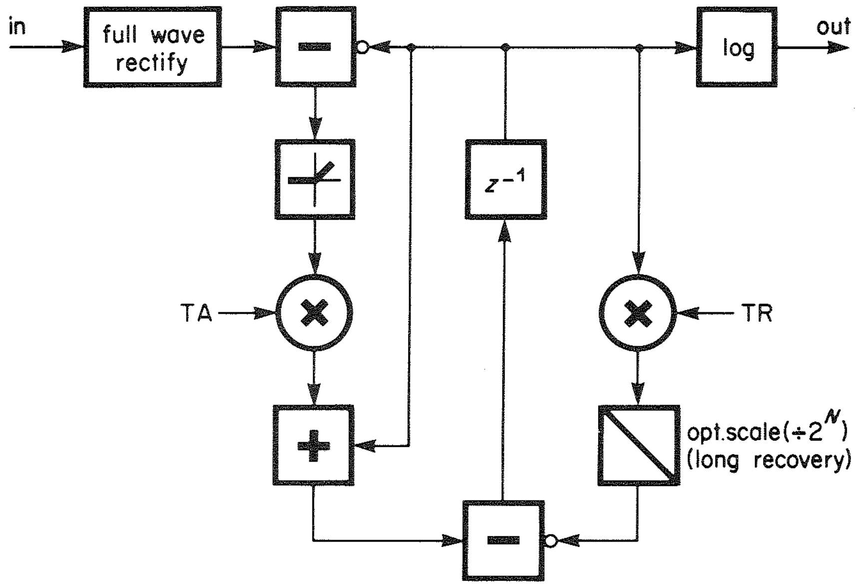

Fig. 3 — Block diagram of peak measuring method.

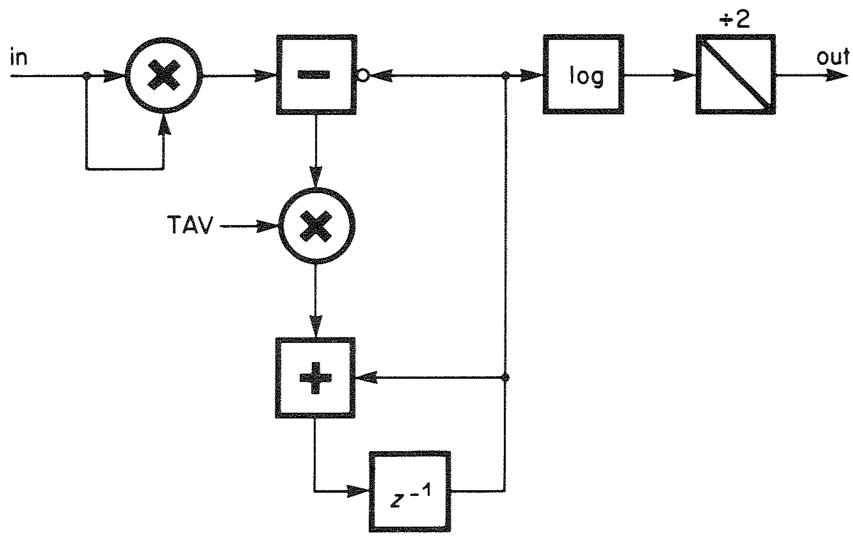

Fig. 4 — Block diagram of r.m.s. measuring method.

in dB. Methods for calculating this logarithm are discussed in Section 5.1.

For some applications, r.m.s. detection will be preferred and this can be achieved using the block diagram shown in Fig. 4. This uses a conventional first-order filter section to provide exponential averaging of the square of the input. In the averaging circuit, a proportion of the difference between the average store value determined by *TAV* and the applied signal at the input is added to the average store value at each sampling instant. The logarithm of the output is taken and divided by two to provide the square root function and the signal is then suitable for comparison with thresholds as before.

A comparison of Figs. 3 and 4 reveals that the underlying structure in each case is that of a first order recursive digital filter. The following analysis can be applied to both to derive values for the filter coefficients, though for the peak detector, interaction between attack and recovery time constants must be assumed to be negligible. In practice, this is a reasonable assumption since the longest attack times would be in the region of

10 ms and the shortest recovery about 100 ms.

The transfer function, $H(z)$, of such a low-pass first order filter section with coefficient, a is easily calculated using z plane notation as,

$$H(z) = \frac{a}{1-(1-a)z^{-1}}$$

and the magnitude of the amplitude response, $|H(z)|^2$ is given by:-

$$|H(z)|^2 = H(z).H(z^{-1})$$

$$= \frac{a^2}{a^2 + 2(1-a)(1-\cos\theta)}$$

where $\theta = wT$ and T is the sampling period of the digital filter. For a sampling frequency of 32 kHz and a time constant $\tau > 60\mu s$, then at the -3 dB point, $\theta < 0.5$ and using the approximation $2(1-\cos\theta) \approx \theta^2$, we have

$$|H(z)|^2 \approx \frac{a^2}{a^2 + (1-a)\theta^2}$$

The time constant of this digital filter is found from the -3 dB point at which $|H(z)|^2 = 0.5$ and by solving for w,

$$w_{3\,\text{dB}} = \frac{\theta}{T} = \left[\frac{a^2}{(1-a)}\right]^{1/2}$$

For the corresponding analogue filter, $w_{3\,\text{dB}} = 1/\tau$ and thus

$$\tau = T\left[\frac{(1-a)}{a^2}\right]^{1/2}$$

Hence for a given attack, release or averaging time, the digital filter coefficient a can be calculated and used in the implementations of Fig. 3 and 4.

Peak and r.m.s. detection can be combined to give an auto-recovery mode. This inserts a short recovery time for isolated peaks but with signals of higher average level, the recovery time is extended, thus avoiding excessive limiting or compression. A method of implementing the auto-recovery mode is shown schematically in Fig. 5.

Even with short attack times, brief signal peaks or transients may cause overshoot at the output of a limiter. This can be avoided by using a short delay (about 300 μs) in the signal path to give the detection circuits time to act before a peak occurs a technique used successfully in analogue limiters. A digital delay can be easily extended to permit overshoot-free performance with much longer attack times.

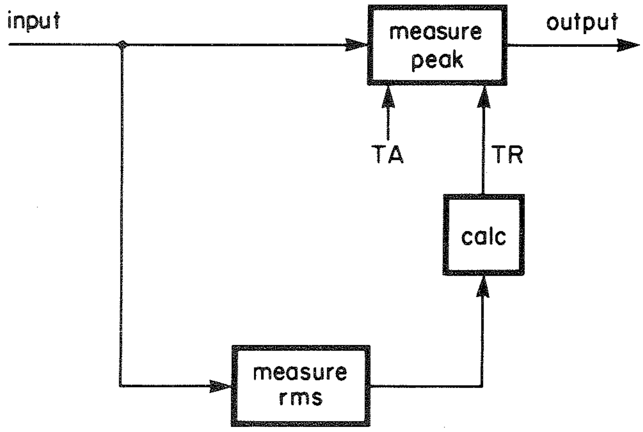

Fig. 5 — Block diagram of proposed method for auto-recovery time.

4. Static characteristics and their digital realisation

This Report is chiefly concerned with three dynamic range control devices, i.e. the limiter, compressor and expander. The steady-state input/output and gain characteristics (static characteristics) for examples of each of these devices are shown in Fig. 6. Each of the characteristics produce a series of straight line sections using a dB scale so that within each section the limiting, compression or expansion behaviour is independent of level.[6] In each case, the characteristic is specified by the following two parameters:

— Threshold:- The signal level at which the required action (e.g.) compression is initiated, usually expressed in decibels relative to normal programme line-up level.

— Ratio:- This is the ratio between changes in level, measured in dB, at the input and output of the DRC. These ratios are normalised so that for a limiter or compressor, the change in input is related to a 1 dB change in output; and for an expander or noise gate, a 1 dB change in input is related to the change in output.

In Fig. 6, a four region DRC is specified by three thresholds and three ratios, the parameter names and values for which are detailed in Table 1.

ETH	expander threshold	−50 dB
ER	expand ratio	1 : 2
CTH	compressor threshold	−35 dB
CR	compressor ratio	3 : 1
LTH	limiter threshold	−15 dB
LR	limiting ratio	100 : 1

Table 1: Example specification for a four region DRC.

In principle, a larger number of these regions could be used to give a piecewise linear approximation to any desired static characteristic. When digital processing is used to implement these characteristics, the calculations in the control path can be sufficiently precise for the input controlled configuration of Fig. 1b to be used. It is, however, necessary to perform the side-chain processing on logarithmic values before conversion to a linear ouput level control signal.

4.1. Calculation of parameter values

When carrying out arithmetic processing on a programmable processor, the use of fractional arithmetic has been shown to be desirable.[1] The specification for thresholds and ratios can be converted to fractional values in the following ways:-

(a) A ratio may be converted to a slope, corresponding to the slope of the gain characteristic. For the example so far considered, three new parameters are defined and are shown in Table 2 with their corresponding values.

ES	expander slope = 1 −1/*ER*	−1
CS	compressor slope = 1 − 1/*CR*	0.67
LS	limiter slope = 1 − 1/*LR*	0.99

Table 2 : Calculation of DRC slopes for ratios in Table 1.

For typical values of *CR* and *LR*, $0 \leqslant CS < 1$ and $0 \leqslant LS < 1$ but for an expander, $ER \leqslant 1$, and so *ES* can have a slope greater than −1. In an expander implementation special arrangements must be made to perform this non-fractional multiplication.

(b) The range of threshold values may be expressed as fractional logarithms. We are concerned only with the magnitude of the input signals which for a 16 bit input, ranges from zero through 2^{-15} up to $1 - 2^{-15}$. Thus valid real logarithms, calculated with a base of 2 and excepting the zero-input case, will produce logarithms in the range −15 to $-\delta$, where δ will depend on the accuracy of computation. To obtain a fractional result, these results are scaled by a factor of 16 and the value −1 is reserved for the zero-input case.

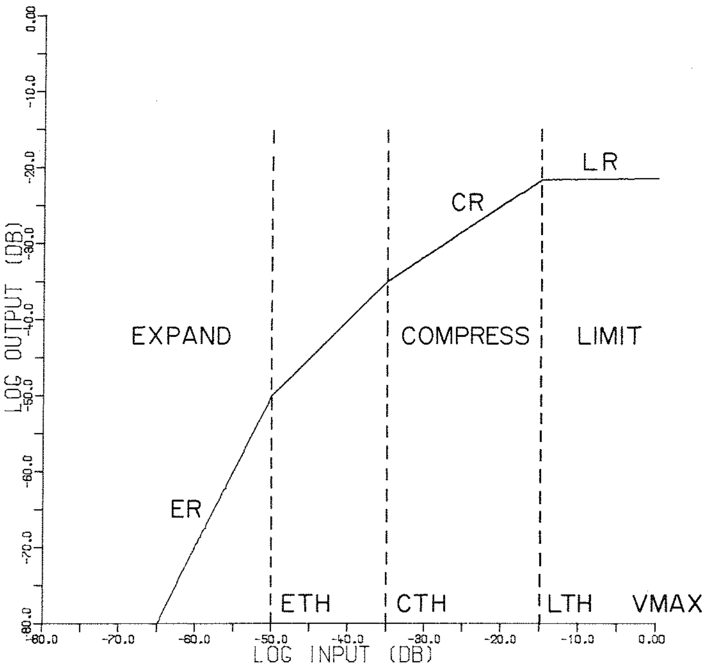

Fig. 6a—Input/output characteristic.

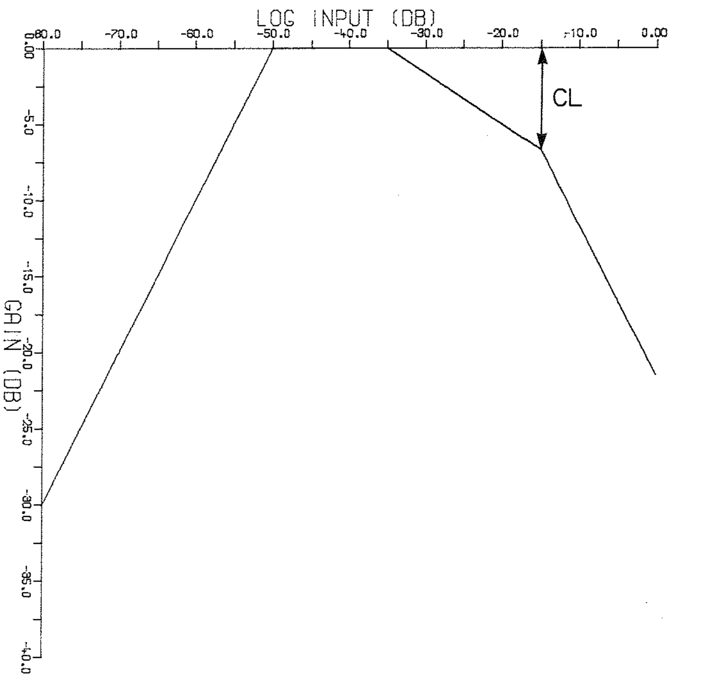

Fig. 6b — DRC gain characteristic.

Now consider a general case in which *VMAX* represents the maximum input signal level in dB, (i.e. the largest permissible input to the analogue-to-digital converter), and a scaling factor S is chosen so that all combinations of specifications produce fractional logarithmic values, then the parameter for the compression threshold can be calculated from

$$CT = \frac{1}{S}\log_2\left\{10^{((CTH - VMAX)/20)}\right\}$$

and the selection of S will satisfy

$$(CTH - VMAX) > 20\log_{10}(2^{-S})$$

The parameters ET and LT can be calculated in a similar way. These values may be stored as look-up tables for a variety of DRC specifications with the benefit that no associated real-time computation is required during execution of the DRC program. In the multiple segment characteristic of Fig. 6a, a correction, CL, must be made to the gain at the limiter threshold to account for the effect of the compressor up to that point. From a geometrical consideration of the gain characteristic of Fig. 6b, this can be calculated from

$$CL = CS\,(CT - LT)$$

With a number of combinations of CS, CT and LT it may not be practicable to store all possible values of CL in a look-up table and the parameter must be calculated by the system controller. The value of CL is then updated for each new compressor or limiter selection.

4.2. Implementation

A method for implementing the four section DRC is shown in block diagram form in Fig. 7. The logarithmic input from the detector is compared with each the three thresholds and if none are exceeded, i.e. input lies in the 'normal'

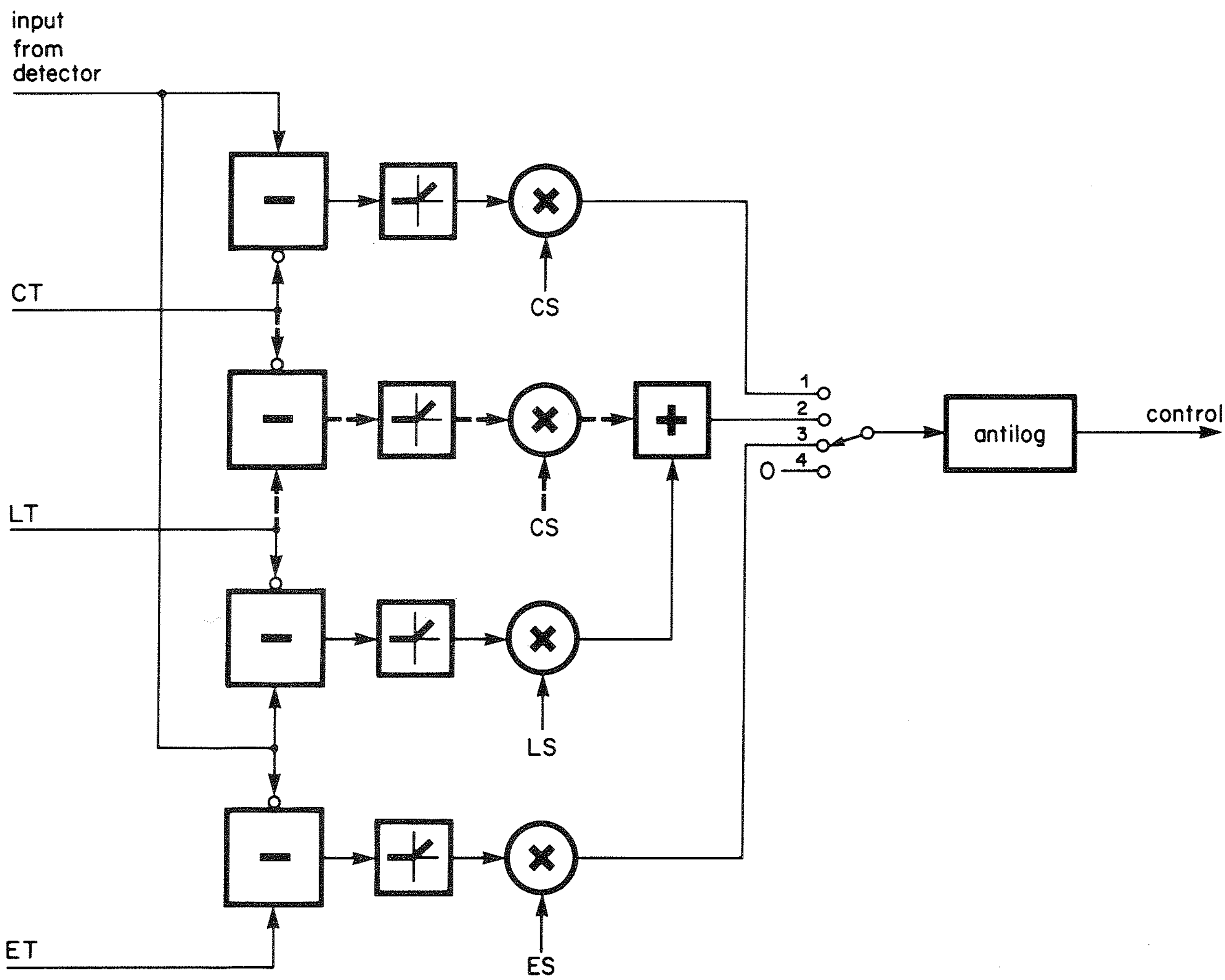

Fig. 7 — Block diagram of method for generating static characteristics.
— — — non real-time computation.

part of the static characteristic, the output selector is placed in position 4. The antilogarithm of zero is unity and so the control signal does not attenuate the audio signal in the direct path. If the compressor threshold is exceeded, output selector position 1 is used and for each decibel increase above the threshold, the output is reduced by *CS* decibels. Fig. 7 shows the complete system, including the correction derived by comparing *CT* and *LT*, which is necessary when a compressor and a limiter are used simultaneously. This correction is calculated only once for a particular DRC specification. It is not part of the necessarily real-time calculations and is indicated by a dashed line.

5. Quantisation effects in the control chain

In the digital processing in the control chain, quantisation errors may be intrusive if insufficient bits are used. At each stage of the processing it is desirable to minimise the number of bits used so that hardware is simplified and computation is reduced. However, the nature and effect of wordlength truncation in the control chain introduces some unfamiliar distortions which will be critically dependent on the way in which the DRC is used. In the following discussion, the effects of truncation in the implementation of the dynamic characteristics is ignored, since this is equivalent to the effects of truncation in digital filters and is adequately covered by a companion Report.[7]

The most critical process in the remainder of the control chain is the calculation of logarithms and anti-logarithms and to some extent the accuracy is determined by the size of look-up table that it is convenient to use. Whereas the static characteristics of an analogue DRC will effect a smooth transition into the region of dynamic range control, the digital implementation has a sharp 'knee' followed by a quantised approximation to the required gain reduction. The nature of the approximation is shown by example in Fig. 9a and is discussed in detail in Sections 5.1. and 5.2. The effect of these errors must be considered for both short and long attack and recovery times.

When the detector signal varies slowly with time, coarse errors in the static characteristic produce gain 'cogging', i.e. the gain changes suddenly between discrete, discernible settings. It is important to note that these static characteristics do not imply steady-state waveform distortion (as they would if they related instantaneous input and output voltages) but simply indicate a law relating gain and steady-state level input level.

Thus it may be expected that if the gain changes are sufficiently small and occur infrequently, a subjectively acceptable result may be obtained.[8]

If short attack and recovery times are used, the rapid changes in the detected signal will impose 'zipper' noise on the gain control signal if insufficient bits are used. It may be difficult to assess the accuracy required for calculations in the control chain, because under these conditions there is a significant amount of modulation distortion for even a perfect DRC and this is of a similar nature to the 'zipper' noise.

The following Sections discuss computational methods by which the performance can be made to approach that of an 'ideal' DRC. Two techniques were used to assess the accuracy required; firstly a computer simulation was made of the quantisation behaviour of the control chain, and secondly an implementation with very high accuracy was constructed and the wordlengths artificially restricted so that the effects could be judged subjectively.

5.1. Calculation of logarithms

In the control chain processing the output of the peak/r.m.s. detector must be expressed on a logarithmic scale. The non-linear filtering action of the detector can produce many more bits than the original 16 bit input signal, and an accurate logarithm of this signal is required, scaled into the range −1 to zero. The amount of storage required for the look-up table can be reduced if the logarithm of a value, x, is expressed

$$\begin{aligned}\log_2(x) &= \log_2(m.2^{-N}) && 0.5 \leqslant m < 1\\ &= -N + \log_2(m) && 0 \leqslant N \leqslant 15\end{aligned}$$

where m,N are the mantissa and exponent in this binary floating point representation of x. The use of base 2 logarithms greatly simplifies this operation; the method is illustrated in Fig. 8 for a 16 bit linear input. By applying N shifts, the linear input can be scaled into a number between 0.5 and 1. The logarithm of the mantissa is obtained from the look-up table indicated as region **c** in Fig. 8. The exponent is simply $-N$, represented by the five most significant bits. The result is shifted four places notionally to the right to give a negative fraction.

$$\text{e.g. } \log_2(0.1875) = \log_2(0.75.2^{-2}) = -2 + (-0.415)$$

representing in binary = 1 1101. 1001 0101
and after scaling* = #ECA8 (= −0.15112)

*# Denotes fractional, hexadecimal two's complement notation.

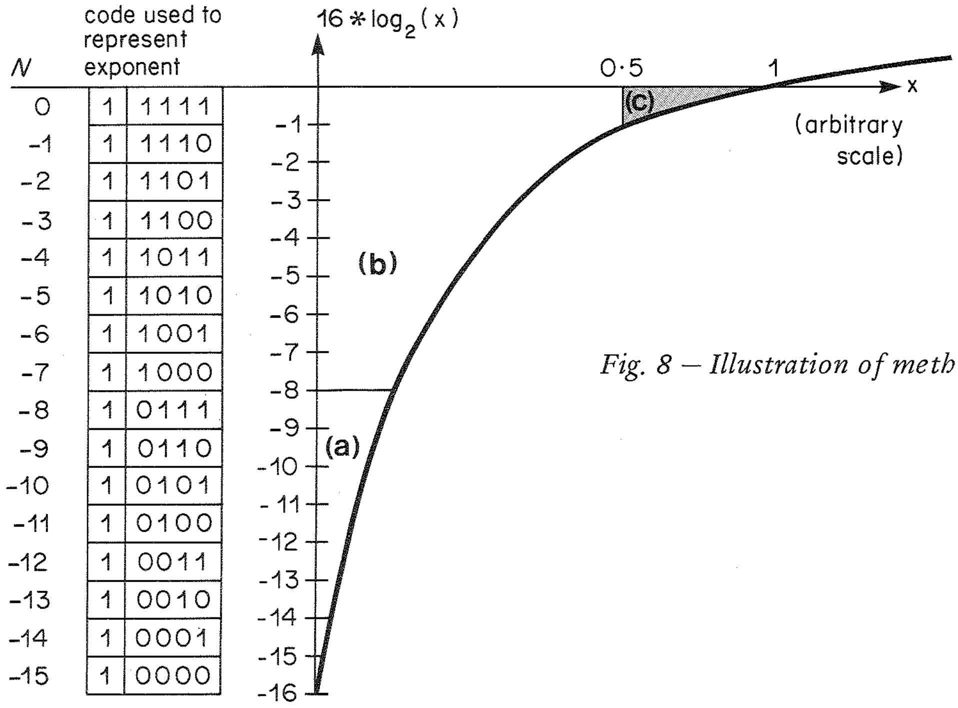

Fig. 8 — Illustration of method of calculation of logarithms.

In this example the logarithm of the mantissa is obtained from a table with 8 bit words. This incurs a quantisation error of 0.00016 since $\log_2$ (0.1875) =–0.15094. However, the technique of calculating the logarithm of mantissa and exponent separately has reduced the number of table entries from 2^{16} to 2^8.

This method of calculation has the useful secondary advantage that the processing load can be reduced if lower accuracy can be tolerated. For example, at its simplest, suppose that shaded area **c** representing the look-up table (e.g. a *PROM*) contains P entries for numbers in the range $0.5 \leqslant x < 1$. If the table size is doubled, then a further P entries may be allocated to the linear input range $0 \leqslant x < 0.5$ in regions **a** and **b**. This permits the accuracy of the calculation to be selected in the following way.

1. No exponent calculation – The look up table alone provides the logarithm, i.e. $2P$ entries of b bits. This gives a resolution in the output of $(b + 1)$ bits including sign bit.

2. Exponent calculation with limited N – The exponent calculation requires that the mantissa is scaled by 2^{-N}, which is an expensive operation in hardware or software. For a 16 bit linear input and $0 \leqslant N \leqslant 7$, then maximum accuracy is maintained in regions **b** and **c** with a resolution of $(b + 5)$ bits while in region a $(b + 2)$ bits are valid.

3. High resolution – With $0 \leqslant N \leqslant 15$, and 24 bit linear inputs, $(b + 5)$ valid output bits can be obtained over the whole input signal range.

The different methods can be used depending on the application. For a limiter with a threshold of –6 dB relative to maximum level, accurate logarithms are required only in region **c** since the control chain is only active when this threshold is exceeded. For lower thresholds this approach may still be acceptable, but in the case of an expander with a threshold of say –30 dB, accurate logarithms will certainly be required in region **b** and possibly region **a** too, since for this case the control chain is active for small input signals.

5.2. Calculation of anti-logarithms

This is the reverse of the procedure for the calculation of logs. An exponent can be derived from the most significant bits and this reduces the size of the look-up table which derives the mantissa. The mantissa is then scaled by the exponent to form the linear output, which can be conveniently achieved by binary shifting if base 2 logarithms are used.

The antilog look-up table contains values corresponding to region **c** in Fig. 8. Again, the accuracy of calculation can be selected by using the same techniques as were described for

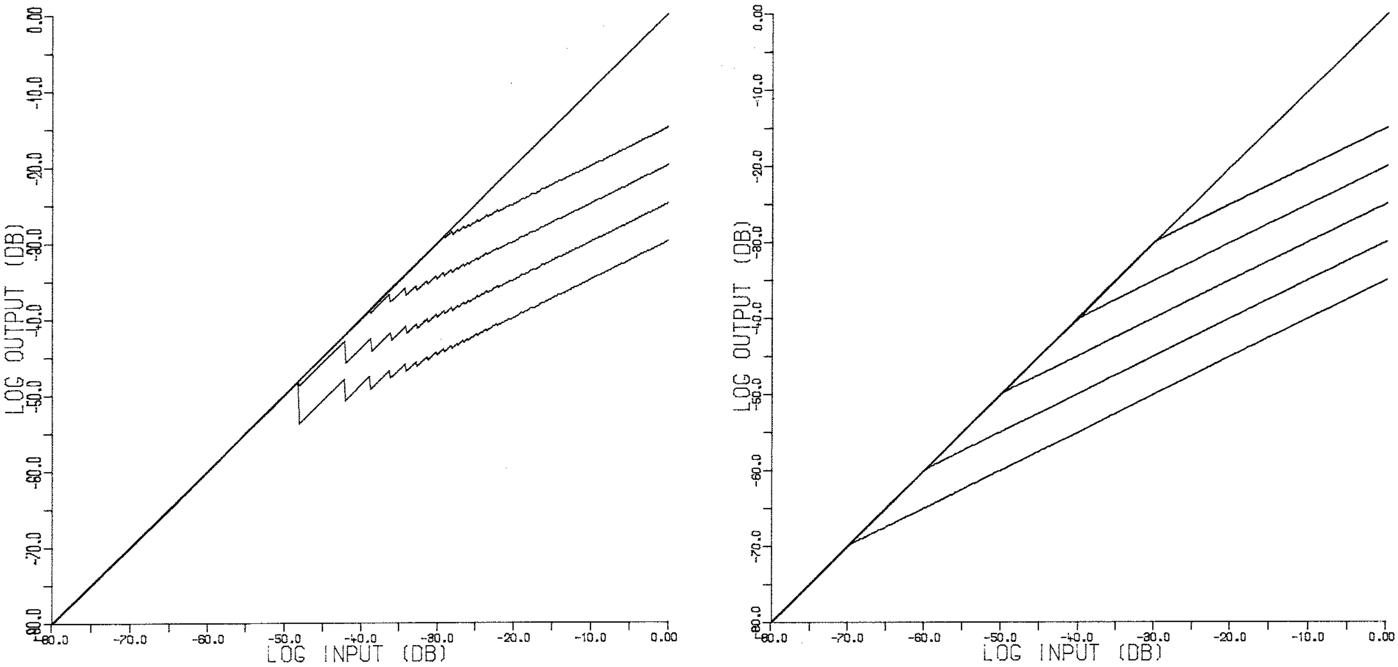

Fig. 9 — Quantisation of the static characteristics.

(a) Direct look-up table approach; (256 x 8) PROM. (b) Exponent/mantissa approach; $0 \leqslant N \leqslant 7$; (256 x 8) PROM.

logarithmic conversion. However, for the hardware that was built and which is described in a companion Report[1], the high resolution method could be achieved with little difficulty and was therefore the method used. Thus the *PROM* look-up table does not contain any entries corresponding to regions **b** and **a**.

5.3. Implementation of log/antilog functions

Since the log. and antilog. calculations contribute the major errors in the control chain, the parameters which have to be specified are the size of the look-up tables, each *(P* x *b)* bits, and the maximum value of the exponent, *N*. In each case, a reduction in these parameters will save hardware or shorten run-times. A Fortran program was written to simulate the effect of variations in these parameters on a family of compressors and the results of this simulation are presented in Fig. 9. In Fig. 9a, a simple look-up method is used, i.e. method 1 in Section 5.1., and as expected, for high thresholds the 'cogs' in the static characteristic are small ($\approx$ 0.05 dB). However, at a threshold of −48 dB, a cog of 6 dB is present which is clearly undesirable. In Fig. 9b, the same look-up table is used but this time a separate exponent calculation is made for $0 \leqslant N \leqslant 7$, i.e. method 2 in Section 5.1. For this case the cogs remain at $\approx$ 0.05 dB for thresholds as low as −48 dB, approximately doubling for each 6 dB lowering of the threshold beyond −48 dB. This seems adequate for compressors and limiters, but expanders may require the high precision calculation, so that the gain adjustments to very low amplitude inputs are not too coarse.

According to the method chosen for log/antilog conversion, the gain control signal will introduce cogging or zipper noise to some extent because of the limited accuracy of the processing. A method of smoothing has been devised which adapts to the dynamic characteristics of the detector and permits the log/antilog processing to be carried out to a lower accurancy than would otherwise be required.* A block diagram representation of such a scheme is shown in Fig. 10. The difference signal across a one sample delay is used to establish whether the detector is in the attack or the recovery mode. A small amount of hysteresis is used to provide a firm boundary to these decisions and according to the result, one of two coefficients, *ATTSM* or *RECSM*, is selected for a first-order low pass filter (shown shaded in Fig. 10). During periods of fast attack, the filter time constant is short, determined by *ATTSM;* and during the recovery period the time constant is long, determined by *RECSM*. It was found experimentally that to give effective smoothing without significantly changing the dynamic characteristics, *ATTSM* and *RECSM* should be

* British patent applied for.

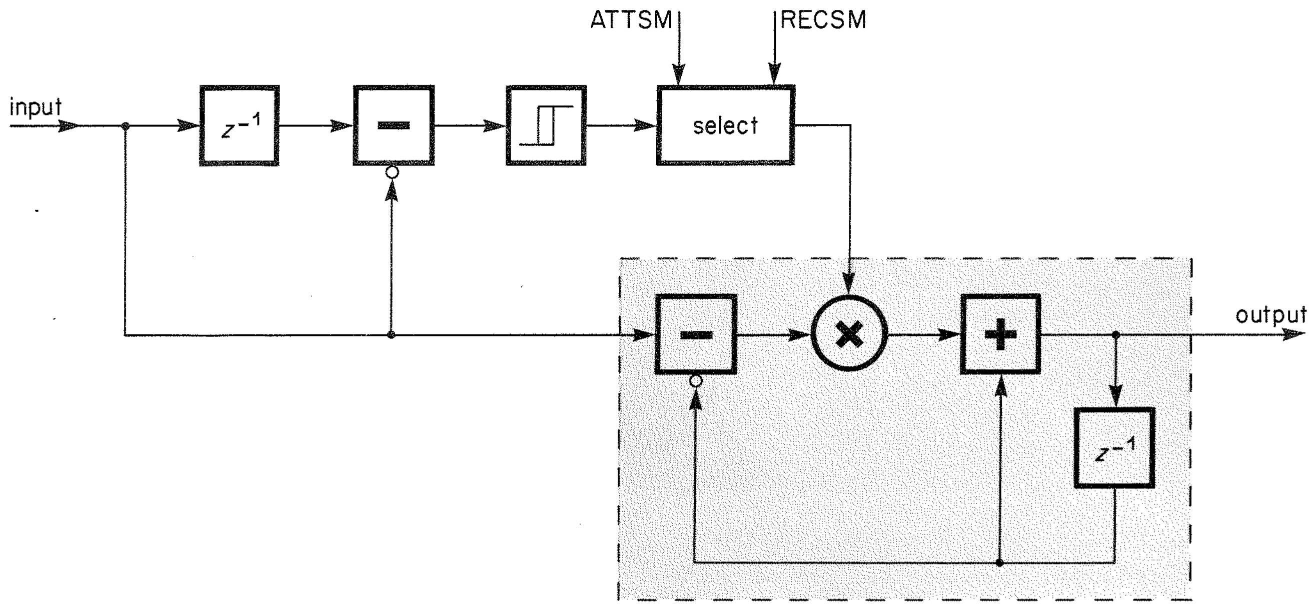

Fig. 10 – Adaptive filtering of the control signal.

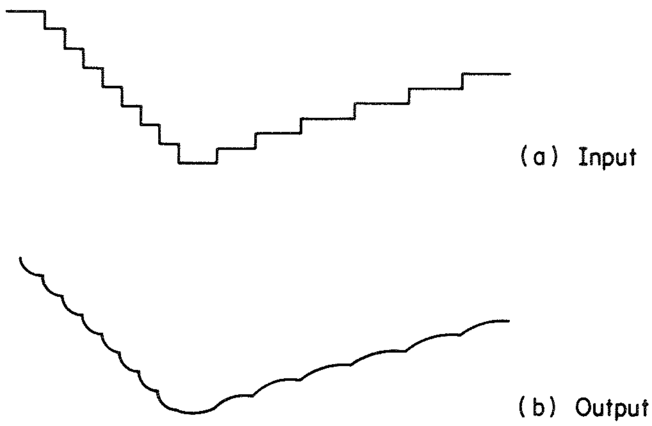

Fig. 11 – Control signal before and after smoothing.

set to give filter time constants one third the attack and recovery time constants, respectively. The effect of this filter on the gain control signal is illustrated in Fig. 11. In informal listening tests it was found that observers could not detect gain cogging or zipper noise for a wide range of attack and recovery specifications, and that good results were obtained even when the 'cog' size was as large as 0.75 dB.

6. The effects of non-linear processes in the control chain

The combined signal processing for the control chain of a digital limiter is illustrated in Fig. 12. Many of the operations are highly non-linear and so it is important to consider the effects that harmonic and intermodulation distortion products might have. In an analogue system these components are removed by a low-pass filter, but in a digital implementation it is possible for these components to alias into the passband of the corresponding digital low-pass filter. This problem is most severe at the detector where the input is the full bandwidth audio signal.

The spectrum of the squared input used for r.m.s. calculation is given by the trignometrical identity,

$$\sin^2 wt = 0.5 - 0.5 \cos 2wt$$

and illustrates that for a sinusoidal input only the second harmonic is generated. This can be safely removed by the linear digital low- pass filter shown in Fig. 4 which typically has a time constant of 50ms and for which a measurement error of < 0.1 dB would result from the aliassing caused by a full amplitude sinusoidal signal at the maximum frequency passed by an anti-alias filter at the input.

When peak detection is used, the spectrum is obtained from the Fourier series expansion of the magnitude of the input,

$$|\sin wt| = \frac{2}{\pi}\left\{1 - \sum_{n=1}^{\infty} \frac{2}{(4n^2-1)} \cos 2nwt\right\}$$

and illustrates that an infinite number of even harmonics are generated from a sinusoidal input. This signal is filtered by the non-linear low-pass filter shown in Fig. 3, and this too will introduce distortion though to a much lesser degree. The second

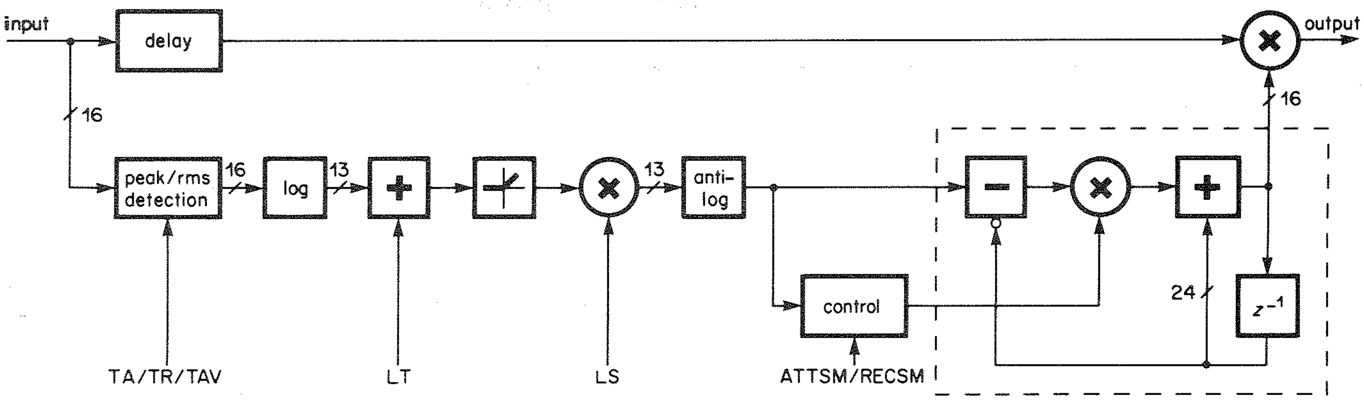

Fig. 12 – Elements of a digital limiter.

harmonic will not cause significant aliassing for the reasons described above in the r.m.s. case; but the 4th harmonic of signal at or near $f_s/4$ would introduce an alias component at z.f., some 21 dB less than the peak value. This cannot be removed by the low-pass filter and would cause up to 0.8 dB measurement error. Higher harmonics would also contribute to the error.

After detection, the control signal is subject to further non-linear processes of log/antilog conversion and adaptive filtering. However, in each case, the sampling rate is much higher than the reduced bandwidth of the control signal. The final stage of adaptive low-pass filtering minimises the in-band distortion products.

These predictions were checked by experiment using a low distortion analogue oscillator and a digital readout of the gain control signal at the output of the adaptive filter. A peak detector with T_a = 300μs, T_r = 100ms and 2:1 compression above a low threshold of –24 dB was programmed using COPAS–2 and a 32 kHz sampling rate. With an 8 kHz, zero programme level input, a worst case measurement error of 0.65 dB was obtained. For a 4 kHz input, the worst case error reduced to 0.1 dB and for all other inputs the error was negligible. The significant errors were confined to only a few Hz each side of 8 kHz and 4 kHz and this was considered a fully acceptable level of performance.

7. An experimental digital dynamic range controller

The techniques described in the previous Sections have been tested by implementing them on COPAS–2*. The architecture of this digital signal processor was designed to be efficient at performing the algorithms for these techniques and Fig. 12 gives the block diagram representation of the computer program that was written for the processor. Although only the limiter section is shown, a full expander/compressor/limiter was implemented as depicted in Fig. 7. The design includes a digital delay of up to 8ms at a 32 kHz sample rate which permits long attack times to be achieved without overshoot. The final gain control element is a multiplier which can be operated using floating-point arithmetic to minimise the effects of roundoff errors. It is common to make gain adjustments to the output of a DRC and this is easily incorporated in this multiplier stage.

The active wordlengths used at various stages of processing are indicated in Fig. 12. Logs and antilogs are calculated using look-up tables of (256x8) bits each with exponent values in the range $0 \leqslant N \leqslant 7$. This gives an accuracy of threshold settings to $\approx$ 0.05 dB and any 'zipper' noise introduced by this processing is effectively concealed by the adaptive filter. The structure and internal 24 bit arithmetic of this filter ensures that no significant roundoff noise is introduced into the smoothed control signal even with very long time constants.

The DRC program has a total of 98 instructions with a maximum run-time of 7.28 μs (corresponding to 52 instructions and a 140 ns cycle). It is therefore practical to provide the full facilities of expansion, compression and limiting with preliminary delay for a single audio channel using less than 25% of the processing available at a 32 kHz sampling rate.

Parameters for the DRC program are transmitted via the *IEEE*-488 interface of the

*This unit was constructed by D.J. Marshall.

COPAS–2 unit. The use of standardised commands for this interface is highly desirable and greatly simplifies its operation.

Typical commands recognised in COPAS–2 are:-

.TC–HHHH HHHH HHHHS	attack, release, averaging times
.E–HHHH HHHH$	expander threshold, slope
.C–HHHH HHHH$	compressor threshold, slope
.L–HHHH HHHH$	limiter threshold, slope
.CL–HHHH$	correction for limiter
.D–HH$	delay in samples (max 255)

Each command begins with a period, followed by either one or two command characters, then a dash (–) indicates that data follows. Each 'H' represents a hexadecimal digit so that, for example, the compressor command uses two, 16 bit coefficients. The command is terminated by the ASCII escape code 'ESC', which is printed as ($) in this example. This control scheme leads to a flexible system for both experimental use and for developed equipment. An 'executive' computer is used to examine a keyboard and a special purpose control panel to generate the appropriate commands. This computer was also used to update a display to show the characteristics of the DRC in operation. An example of this display is shown in Fig. 13, a photograph taken of the display of a desktop computer which was used for the experimental work.

There are many features which are found in analogue DRCs which have not been covered in this Report. Among these are the ability to derive a common gain control for stereo applications, or to use a gain control signal from a different input to achieve special effects. The use of band splitting filters and the separate dynamic range control of each band before re-combination is sometimes required. Many methods have been proposed for the detection circuitry, including automated recovery times and detection based on crest factor measurement. However, all these facilities are extensions or re-arrangements of the basic building blocks described in this Report and though their detailed implementation has been omitted, they could be readily implemented on COPAS–2.

8. Conclusions

This Report has described methods for implementing flexible control of the dynamic range of audio signals using digital processing techniques. Compression, limiting, expanding and noise-gating methods have been proven by using a programmable audio signal processor, COPAS–2, to execute this digital processing. After measures had been applied to reduce the subjective effect of quantisation errors, the audio performance of the digital DRC was much as would be expected from an ideal analogue DRC. The effects of non-linearities in the control chain have been considered and shown to introduce a worst-case measurement error of 0.8 dB and typically < 0.1 dB.

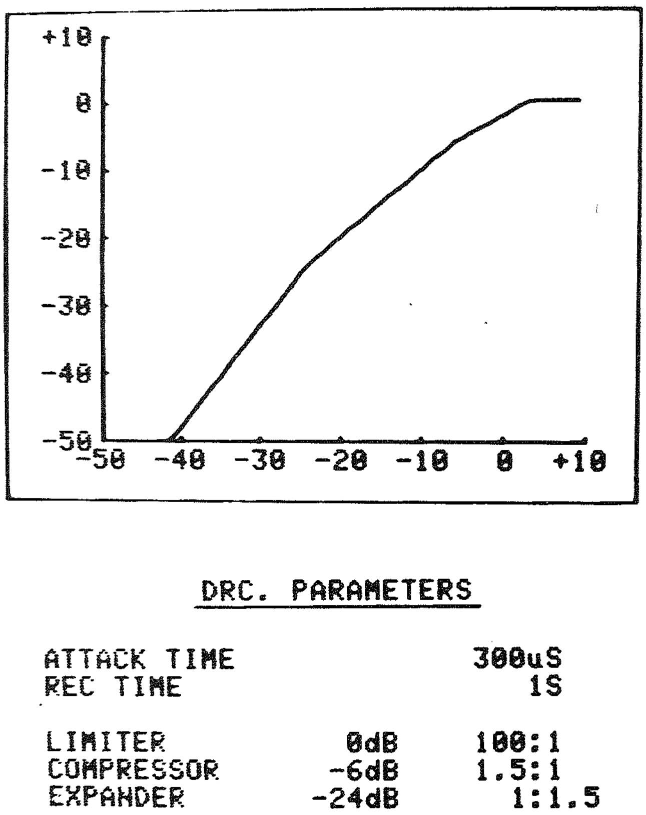

Fig. 13 – Typical controller display for experimental DRC.

The processor incorporates special-purpose circuitry to carry out the log/antilog algorithms described while the filtering operations are well suited to its internal architecture. The complete DRC was programmed to run in 7.28 μs – a figure which indicates that it is practical to do processing of this sort in programmable hardware.

9. Acknowledgement

This work was carried out in collaboration with the Neve Group of Companies.

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