Kevin Cook

kevin137@gmail.com
+34 625 632 421

Summary

Bilingual hardware architect and project manager with a unique physics background and extensive industry experience, including product development work in the industrial computing, satellite television and datacom sectors. Expertise in multi-gigabit circuit design for networking systems, PCB design for manufacturability, large dataset techniques, and development of software for design automation and product validation. Proven ability to collaborate with clients, partners, vendors, and contract manufacturers.

Technical Expertise

Methodologies/Technologies

- Product development from initial concept, to requirements negotiation with clients, to functional prototype, through validation to mass production
- Project management including coordination of mechanical, hardware, software, web, and cloud developers
- Circuit design, schematic capture, and PCB routing with Altium, Zuken, Mentor Graphics, and FOSS tool suites
- Large dataset manipulation, visualization, and inference using the Python/NumPy/Data8/Jupyter stack applied to circuit simulation, design automation, and product validation results
- Automated test development using HTML5+JavaScript, Ruby+Cucumber, LabWindows/CVI, TCP/IP, and custom hardware
- Product validation and characterization using extensive automation, RF techniques, EMC anechoic chambers, BERT, time domain reflectometry, power, thermal, and vibration testing
- Development of HTML5+JavaScript web applications for internal R&D use

Computer Languages	Python+NumPy, R, HTML5+JavaScript, C/C++, Ruby+Cucumber, LabWindows/CVI, Java, Perl, VisualBasic, Access/SQL, XML, Markdown
Applications	Altium, KiCAD, Zuken tools including CADSTAR and SI Verify, Mentor Graphics tools including DxDesigner and PADS Router, LTSpice, Hyperlynx, Polar, SolidWorks, FreeCAD, AutoCAD, SketchUp, TSReader, Excel, FrameMaker, MATLAB/Octave/Simulink
Television / Datacom	On-site certificates in HEVC, HLS/MPEG-DASH, G.984 GPON; Telcordia certificates in TCP/IP, DWDM, SONET/SDH, T1/E1

OS / Platform	Linux, Windows, MacOS, vxWorks, VMware, Vagrant, Docker, EC2
Natural Languages	English (native), Spanish (fluent), German (basic)
Continuing Education	Foundations of Data Science Professional Certificate (BerkeleyX, 2018)

Professional Experience

Aingura IIoT - *Donostia-San Sebastián, Spain*

Hardware Architect (2020-currently)

Leading development of all electronic hardware in Aingura
Developing next generation of products for industrial sensing, edge computing, OT networking.

Ikusi - *Donostia-San Sebastián, Spain*

Project Manager, Multimedia Business Unit (2012-2020)

Managed project to develop customized, cloud-connected television headend
Directed multi-year hardware/software/cloud project for a key customer, coordinating product, features, timelines, and validation. Platform is currently deployed in hundreds of sites across Australia.

Led hardware and mechanical development for new multimedia headend
Developed modular headend architecture including a novel, cost-effective networking system for control based on embedded USB--several current products are based on this platform and its derivatives. Implemented new active thermal system for the platform. Led hardware design of all key PCBAs for the system, integrating new microprocessor, FPGA, DRAM systems, and Ethernet IPcores. Collaborated with PCB fabricators to optimize performance and cost of hardware, with firmware developers to rationalize and modularize devicetree, and mechanical designers to improve EMC.

Directed design of networking subsystem for TV platform
Specified, designed, and implemented streaming-optimized networking system, from hardware to VLAN level, from line card PHYs to backplane to switch fabric ASIC. System based on gigabit Ethernet integrates switching ASIC in custom modular hardware, and forms the backbone of Ikusi's current premium TV headend. Switch module also includes microprocessor and FPGA for headend control. Managed development of custom firmware for switch ASIC by external contractor. Developed validation protocols, and production test stand including bespoke hardware and software written in Ruby.

R&D Technical Staff, Multimedia Business Unit (2007-2012)

Designed hardware for high-density H.264 transcoding module
System based on ASIC with fast multi-channel DDR3 and a PCI-e interface. Characterized and selected ICs for embedded Ethernet subsystem. Simulated signal integrity of PCI-e lanes using Keysight ADS. Miniaturized PCB layout by a factor of two compared to the ASIC reference design. Benchmarked transcoding performance, optimized thermal management system, developed and executed validation protocols, and cost-reduced the design for mass production. Transcoding systems installed in thousands of B2B locations for a major television operator in France.

Developed hardware for network-enabled satellite television transmodulator
Module was first in its class to incorporate Ethernet networking. Simulated signal integrity of system bus using Zuken SI Verify. Improved DFM and cost of design by increasing integration, migrating PCB fabrication to high-volume overseas facilities, and optimizing mechanical design for assembly by robot. Developed and executed validation protocols, assisted production team with jigs and procedures for automation, and adapted hardware platform to new form factors for new products.

Molex Inc. - *Maumelle, Arkansas, USA*

Electrical Engineer, High Performance Adapters Business Unit (2005-2007)

Redesigned 4.25 gigabit/second Fibre Channel active copper cable assembly
New design had updated transmitter IC to reduce EM emissions, exhibited improved manufacturability and durability. Collaborated with contract manufacturer and PCB fabricator to tune characteristic impedance to optimize signal integrity. Characterized the new assembly, which had improved signal quality, bit error rate, and lower overall cost.

Developed 4.25 Gbps production test system including PCBs and FPGA-based pattern generator
Tester required four new printed circuit boards assemblies, three with tightly controlled impedance. Incorporated a customized Xilinx evaluation board programmed to generate test pattern. Coordinated development with mechanical engineer developing the enclosure, performed final assembly and testing, and shipped the tester to Mexico, where it was in heavy use in a production line.

Characterized adapters and cable assemblies
Compliance testing for Fibre Channel, Infiniband, and Ethernet products required time domain reflectometry, eye diagrams, and bit error rate testing. Built custom assemblies and tuned equalizers for special sample requests. Documented results in detailed test reports for distribution to customers.

Tellabs Operations, Inc. - *Naperville, Illinois, USA*

Member of Technical Staff, Hardware Development (2000-2003)

Developed automated test system in LabWindows/CVI
Custom software-controlled instruments, relay switch matrix, and device under test to measure signal quality characteristics and confirm compliance with Telcordia T1/E1 standard. Test system could fully verify 28 T1 ports with no human intervention, saving hundreds of hours per verification cycle.

Designed gigabit passive backplane for optical telecommunications system
Hardware deliverable was production quality from the first prototype, saving tens of thousands of dollars and months of delay by eliminating the need for a second prototype. Design was a key component in product with hundreds of millions of dollars of revenue per year.

Characterized connector and printed circuit board performance using time domain reflectometry
Measured differential and single-ended signal paths, correlated test data to RF simulations, and performed 2.4 gigabit/second bit error rate testing, thoroughly documenting results.

Iowa State University - *Ames, Iowa, USA*

Undergraduate Research Assistant, Physics Department (1998-1999)

Debugged hardware and software for custom VME-based research instrument
Performed low-level testing, including diagnostic routines in C for the VxWorks platform, fault isolation and device programming for the electronics which became the Level I Trigger for the PHENIX experiment at the Relativistic Heavy Ion Collider at Brookhaven National Laboratory.

Education

University of Illinois at Chicago - *Illinois, USA*

Completed 32 credit hours of specialized physics coursework (2003-2004)

Quantum mechanics, thermodynamics, statistical mechanics, electromagnetism, volunteered as an assistant in a thin-film magnetics laboratory, designing and assembling a cryogenic deposition platform.

Iowa State University - *Ames, Iowa, USA*

B.S. in Electrical Engineering (Completed December 1999)

Advanced coursework in the communications curriculum

- Digital communication systems including synchronization, coding, and encryption
- Feedback control theory and digital systems design
- Network programming in C and Java

Senior Design Project: JALTISA (Java Linear Time-Invariant System Analyzer)