byterunner TECHNOLOGIES

# TECHNICAL DATA ON 16550

All addresses are added to the UART's BASE ADDRESS. IE. LCR register, listed here as 3 (011 binary) would be at 3F8+3 = 3FB for comm 1 and 2F8+3 = 2FB for comm 2

## PROGRAMMING TABLE

| A2 | A1 | A0 | READ MODE | WRITE MODE |
|---|---|---|---|---|
| 0 | 0 | 0 | • Receive Holding Register | • Transmit Holding Register |
| 0 | 0 | 0 | N/A | • LSB of Divisor Latch when Enabled |
| 0 | 0 | 1 | N/A | • Interrupt Enable Register |
| 0 | 0 | 1 | N/A | • MSB of Divisor Latch when Enabled |
| 0 | 1 | 0 | • Interrupt Status Register | • FIFO control Register |
| 0 | 1 | 1 | N/A | • Line Control Register |
| 1 | 0 | 0 | N/A | • Modem Control Register |
| 1 | 0 | 1 | • Line Status Register | N/A |
| 1 | 1 | 0 | • Modem Status Register | N/A |
| 1 | 1 | 1 | • Scratchpad Register Read | • Scratchpad Register Write |

## REGISTER BIT MAPS

| A2 | A1 | A0 | REG. | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | RHR | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0 | 0 | 0 | THR | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| 0 | 0 | 1 | IER | 0 | 0 | 0 | 0 | modem status interrupt | receive line status interrupt | transmit holding register interrupt | receive holding register interrupt |
| 0 | 1 | 0 | FCR | RCVR trigger MSB | RCVR trigger LSB | 0 | 0 | DMA mode select | transmit FIFO reset | receiver FIFO reset | FIFO enable |
| 0 | 1 | 0 | ISR | 0/FIFO enabled | 0/FIFO enabled | 0 | 0 | interrupt prior. bit 2 | interrupt prior. bit 1 | interrupt prior. bit 0 | interrupt status |
| 0 | 1 | 1 | LCR | divisor latch enable | set break | set parity | even parity | parity enable | stop bits | word length bit 1 | word length bit 0 |
| 1 | 0 | 0 | MCR | 0 | 0 | 0 | loop back | OP2 | OP1 | RTS | DTR |
| 1 | 0 | 1 | LSR | 0/FIFO error | transmit empty | transmit holding empty | break interrupt | framing error | parity error | overrun error | receive data ready |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | MSR | CD | RI | DSR | CTS | delta CD | delta RI | delta DSR | delta CTS |
| 1 | 1 | 1 | SPR | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |

## 16550 ACCESSIBLE REGISTERS

**- Register Functional Description** (Courtesy of Starteck Semiconductor Inc.)

### TRANSMIT AND RECEIVE HOLDING REGISTER

**T**he serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

**O**n the falling edge of the start bit, the receiver internal counter will start to count 7.5 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

### FIFO INTERRUPT MODE OPERATION

**W**hen the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

a. The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
b. The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
c. The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

### FIFO POLLED MODE OPERATION

**W**hen FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the 16550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled seperately either one or both can be in the polled mode operation by utilizing the Line Status Register.

a. LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
b. LST BIT4-1 will specify which error(s) has occured.
c. LSR BIT-5 will indicate when the transmit FIFO is empty.
d. LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
e. LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The 16550 requires to have two step FIFO enable operation in order to enable receive trigger levels.

### PROGRAMMABLE BAUD RATE GENERATOR

**T**he 16550 contains a programmable Baud Rate Generator that is capable of tracking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^16-1. The output frequency of the Baudout is equal to the 16X of transmission baud rate (Baudout=16 X Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

### INTERRUPT ENABLE REGISTER (IER)

**T**he Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

**IER BIT-0:**
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

**IER BIT-1:**
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

**IER BIT-2:**
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

**IER BIT-3:**
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

**IER BIT 7-4:**
All these bits are set to logic zero.

## INTERRUPT STATUS REGISTER (ISR)

**T**he 16550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized manner. During the read cycle the 16550 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

| P | D3 | D2 | D1 | D0 | SOURCE OF THE INTERRUPT |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | LSR (Receiver Line Status Register) |
| 2 | 0 | 1 | 0 | 0 | RXRDY (Received Data Ready) |
| 2 | 1 | 1 | 0 | 0 | RXRDY (Received Data Timeout) |
| 3 | 0 | 0 | 1 | 0 | TXRDY (Transmitter Holding Register Empty) |
| 4 | 0 | 0 | 0 | 0 | MSR (Modem Status Register) |

## RECEIVE TIME-OUT:

**T**his mode is enabled when the STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)=4 X P (Programmed work length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit

**Example-A:** If user programs the word length=7, and no parity and one stop bit, Time out will be: T=4X7(programmed word length)+12=40 bits. Character time=40/9 [(Programmed word length=7)+(stop bit=1)+(start bit=1)]=4.4 characters.

**Example-B:** If user programs the word length=7, with parity and one stop bit, the time out will be: T=4X7 (programmed word length)+12=40 bits. Character time=40/10 [(programmed word length=7) + (parity=1) + (stop bit=1) + (start bit=1)=4 characters.

**ISR BIT-0:**
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt penting.

**ISR BIT 1-3:**
Logical combination of these bits provides the highest priority interrupt pending.

**ISR BIT 4-7:**
These bits are not used and are set to zero in 16450 mode. BIT 6-7: are set to "1" in 16550 mode.

## FIFO CONTROL REGISTER (FCR)

**T**his register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

**FCR BIT-0:**
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO. This bit should be enabled before setting the FIFO trigger levels.

**FCR BIT-1:**
0=no change.
1=Clears the content of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

**FCR BIT-2:**
0=no change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

**FCR BIT-3:**
0=no change.
1=Changed RXRDY and TXRDY pins from mode "0" to mode "1".

**Transmit operation in mode "0":**
**W**hen 16550 is in 16450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

**Receive operation in mode "0":**
**W**hen 16550 is in 16450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

**Transmit operation in mode "1":**
**W**hen 16550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

**Receive operation in mode "1":**
**W**hen 16550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

**FCR BIT 4-5:**
Not used.

**FCR BIT 6-7:**
These bits are used to set the trigger level for the receiver FIFO interrupt.

| BIT-7 | BIT-6 | FIFO Trigger Level |
|---|---|---|
| 0 | 0 | 01 |
| 0 | 1 | 04 |
| 1 | 0 | 08 |
| 1 | 1 | 14 |

## LINE CONTROL REGISTER (LCR)

**T**he line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

**LCR BIT 1-0:**
These two bits specify the word length to be transmitted or received.

| BIT-1 | BIT-0 | WORD LENGTH |
|---|---|---|
| 0 | 0 | 5 |
| 0 | 1 | 6 |
| 1 | 0 | 7 |
| 1 | 1 | 8 |

**LCR BIT 2:**
The number of stop bits can be specified by this bit.

| BIT-2 | WORD LENGTH | STOP BITS(s) |
|---|---|---|
| 0 | 5,6,7,8 | 1 |
| 1 | 5 | 1.5 |
| 1 | 6,7,8 | 2 |

**LCR BIT 3:**
Parity or no parity can be selected via this bit.

**BIT-3 PARITY**
0 None
1 Parity is both generated on transmission and checked on receive.

**LCR BIT 4:**
If parity (LCR-3) is enabled. LCR BIT 4 selects the even or odd format.

**BIT-4 PARITY**
0 ODD

1 EVEN

**O**dd parity means that the character will always have an odd number of 1's, and even means it will always have an even number of 1's in the binary representation.

**LCR BIT 5:**
Force parity to always 1 or 0. When this bit is set to 1, then parity will always be 0 if LCR-4 is 1 and will be 1 if LCR-4 is 0.

**LCR BIT 6:**
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state) when set to 1.

**LCR BIT 7:**
The internal baud rate counter latch enable (DLAB).

**BIT 7 BAUD LATCH**
0 disabled, normal operation
1 enabled

## MODEM CONTROL REGISTER (MCR)

**T**his register controls the interface with the MODEM or a pherpheral device (RS232).

**MCR BIT 0:**
0 = force DTR (Data Terminal Ready) to high.
1 = force DTR to low.

**MCR BIT 1:**
0 = force RTS (Request to Send) to high.
1 = force RTS to low.

**MCR BIT 2:**
0 = OP1 (Option 1) output to high.
1 = OP1 output to low.

**MCR BIT 3:**
On the IBM computer the OP2 is used to control the board's interrupt tri-state buffer.

0 = OP2 (Option 2) output to high.
1 = OP2 output to low.

**MCR BIT 4:**
0 = Normal operating mode.
1 = enable local loop-back mode (diagnostic).

**L**oopback mode will do the following. The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS, DSR, CD, and RI are disabled. Internally the transmitter output is connected to the receiver input and DTR, RTS, OP1 and OP2 are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts azre still controled by the IER.

**MCR BIT 5-7:**
Not used. Set to 0 internally.

## LINE STATUS REGISTER (LSR)

**T**his register provides the status of data transfer to CPU.

**LSR BIT 0:**
0 = no data in receive holding register or FIFO.
1 = data has been receive and saved in the receive holding register or FIFO.

**LSR BIT 1:**
0 = no overrun erro (normal)
1 = overrun error. A character arived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

**LSR BIT 2:**
0 = no parity error (normal)
1 = parity error. Receive data does not have correct parity information.

**LSR BIT 3:**
0 = no framing error (normal)
1 = framing error received. Received data did not have a valid stop bit.

**LSR BIT 4:**
0 = no break condition (normal)
1 = receiver received a break signal (RX was low for one character time frame).

**LSR BIT 5:**
0 = transmit holding register is full. 16550 will not accept any data for transmission.
1 = transmitter hold register (or FIFO) is empty. CPU can load the next character.

**LSR BIT 6:**
0 = transmitter holding and shift registers are full.
1 = transmit holding register is empty. In FIFO mode this bit is set to one whenever the the transmitter FIFO and transmit shift register are empty.

**LST BIT 7:**
0 = normal
1 = At least one parity error, framing error or break indicator is in the FIFO. Cleared when LSR is read.

### MODEM STATUS REGISTER (MSR)

**T**his register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads the register.

**MSR BIT 0:**
CTS changed state.

**MSR BIT 1:**
DSR changed state.

**MSR BIT 2:**
RI changed state.

**MSR BIT 3:**
CD changed state.

**MSR BIT 4:**
RTS changed state.

**MSR BIT 5:**
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the CTS input.

**MSR BIT 6:**
This bit is equivalent to OP1 in the MCR during loacl loop-back mode. It is the compliment of the RI input.

**MSR BIT 7:**
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD input.

**Note:** Whenever MSR BIT 3-0 is set to logic "!", a MODEM Statius interrupt is generated.

### SCRATCHPAD REGISTER (SR)

**8** bits of information can be stored in this register.

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## BAUD RATE GENERATOR PROGRAMMING TABLE

**A**ll boards will typically have the 1.8432 MHZ crystal. Some Byte Runner boards will also allow selection of the 7.3728 MHZ clock.

| BAUD RATE | 1.8432 MHZ clock | 7.3728 MHZ clock |
|---|---|---|
| 50 | 2304 | 9216 |
| 75 | 1536 | 6144 |
| 110 | 1047 | 4188 |
| 134.5 | 857 | 3428 |
| 150 | 768 | 3072 |
| 300 | 384 | 1536 |
| 600 | 192 | 768 |
| 1200 | 96 | 384 |

| | | |
|---|---|---|
| 2400 | 48 | 192 |
| 3600 | 32 | 128 |
| 4800 | 24 | 96 |
| 7200 | 16 | 64 |
| 9600 | 12 | 48 |
| 19.2K | 6 | 24 |
| 38.4K | 3 | 12 |
| 57.6K | 2 | 8 |
| 115.2K | 1 | 4 |
| 230.4K | not possible | 2 |
| 460.8K | not possible | 1 |

## POWER UP DEFAULTS

IER = 0
ISR = 1
LCR = 0
MCR = 0
LSR = 60 HEX
MSR = BITS 0-3 = 0, BITS 4-7 = inputs
FCR = 0
TX = High
OP1 = High
OP2 = High
RTS = High
DTR = High
RXRDY = High
TXRDY = Low
INT = Low