UNIVERSITY OF CALIFORNIA IRVINE

EECS 31L: Introduction to Digital Logic Laboratory (Spring 2024)

Lab 4: Processor DataPath

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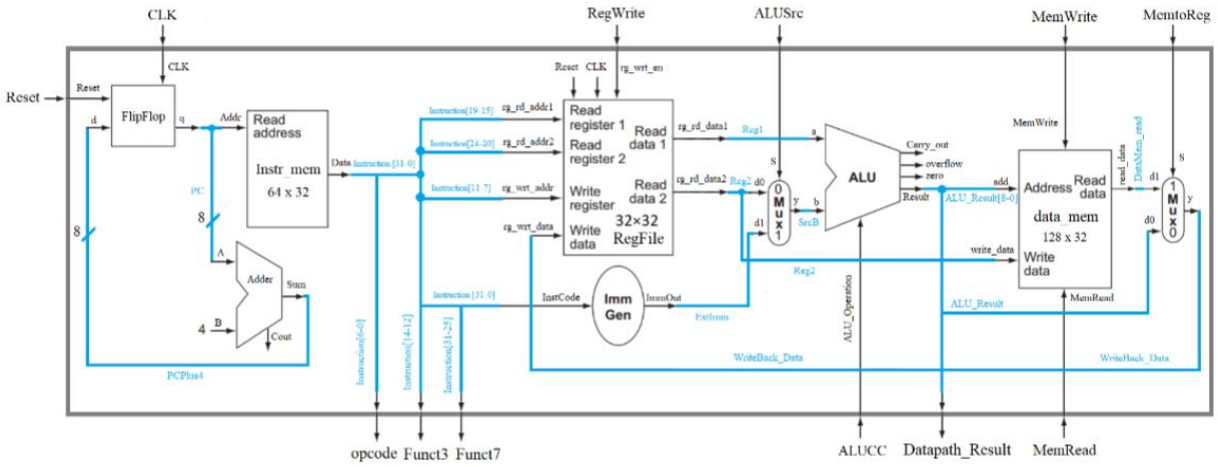
1. Overview



The above is a picture of the Datapath of a single RISC-V single cycle processor. Most of the component blocks have already been made in previous labs. RegFile, FlipFlop, Instr_mem, and ImmGen were all made in Lab 3. The ALU, was made in Lab 2. For Lab 4, I was to make the data_mem, modify the mux I made in Lab 1 to support 32 bits, and connect all these components together according to the above diagram.

2. Hardware Description

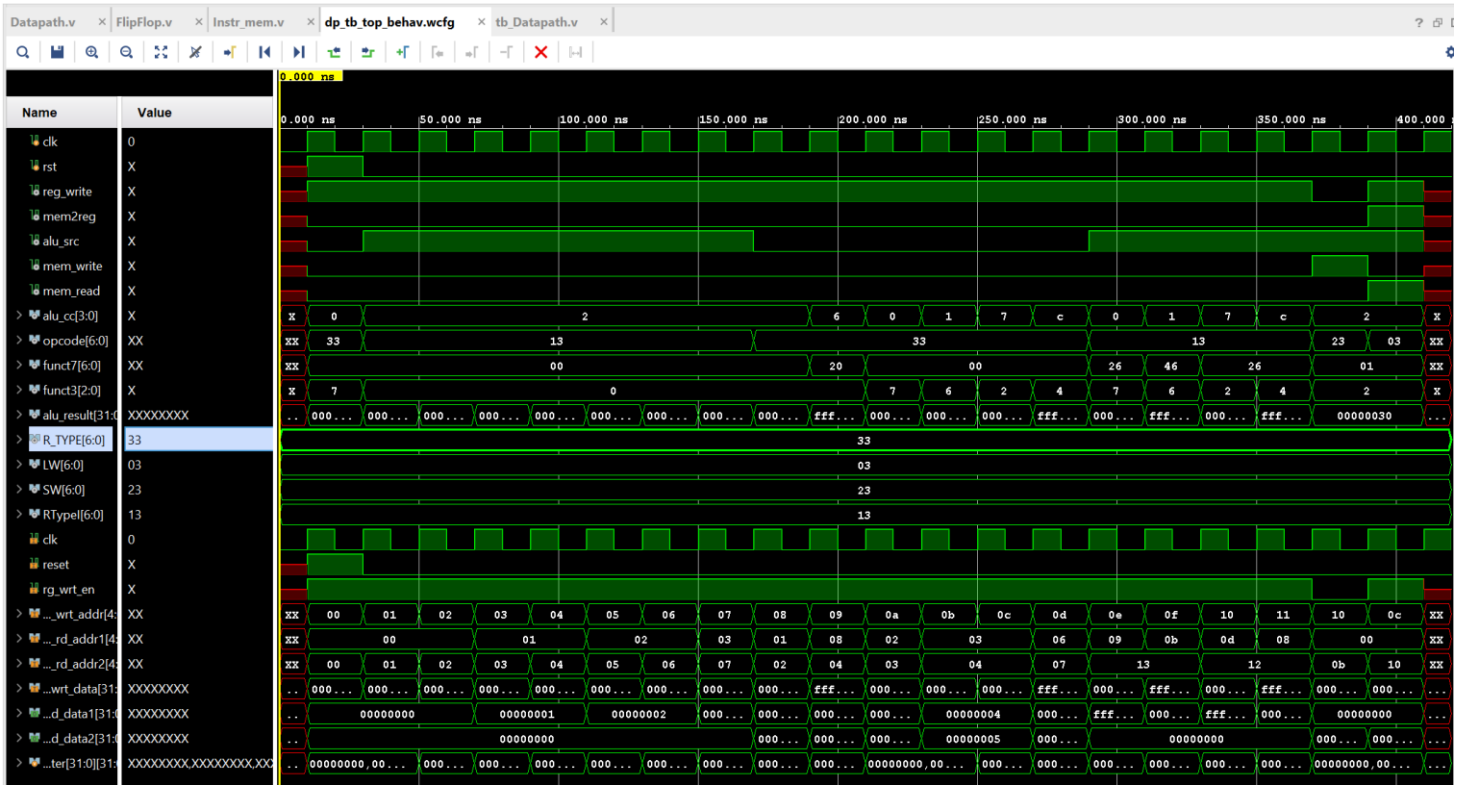
Since I have already explained most of the components in previous labs, I will only focus on explaining the data_mem and the datapath.

Data_mem or Data memory is like Instruction Memory. It stores 128 32-bit elements. Data memory takes in an address and is either able to read the data in that address or write data to that address. The address input is “addr”, the potential data input to be written is “write_data”. Data memory chooses when to write depending on the values of inputs

MemWrite and MemRead. If MemWrite is 1, then DataMem performs the writing function. If MemRead is 1, then DataMem performs the read function. When reading, the data being read is sent to an output called “read_data.”

The Final part of this lab is to make another design module which connects all components mentioned above into a full processor datapath. This datapath has its own inputs and outputs. Its inputs are clk, reset, reg_write, mem2reg, alu_src, mem_write, mem_read, and alu_cc. Reg_write is the enable switch for the register file. Alu_src and mem2reg are the “select” value for the two different muxes. Mem_write and mem_read are MemWrite and MemRead in the Data Memory. Alu_cc is the input that decides which operation the Alu is going to do. The datapath also has its own ouput. These are opcode, funct3, and funct7. Any blue lines are to be wired in my code. These blue wires serve as the different inputs and outputs for all the components that I have created so far. To create this datapath, I wired the correct outputs of one component to the correct inputs of the other according to the diagram.

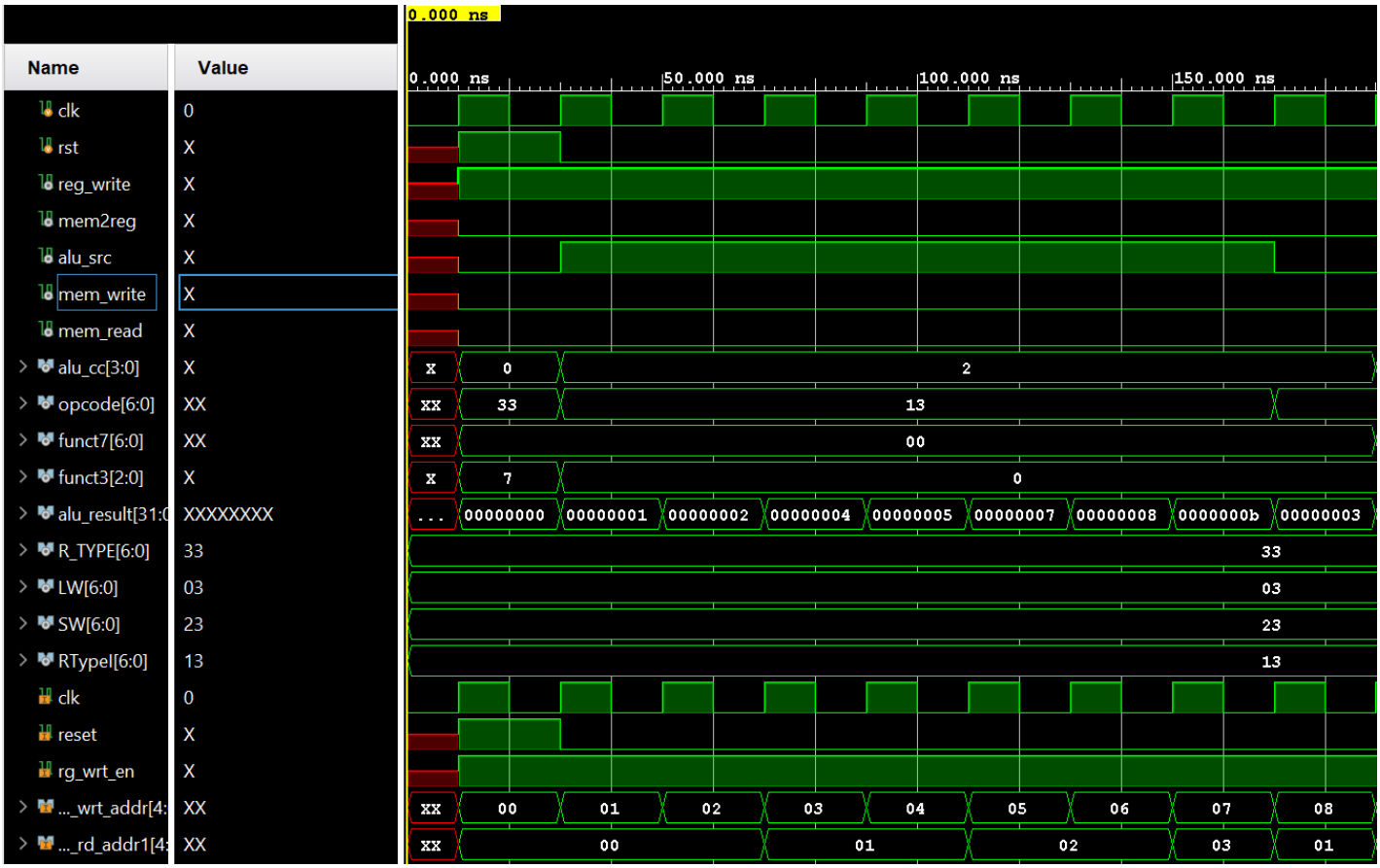
3. Simulation Results



Here are the simulation results for the Datapath testbench. In the Lab instruction manual, they provided me the testbench and the expected waveform result. My own created

waveform matches these results. Specifically, the outputs of opcode, funct7, funct3, and alu_result all match the given waveform.

Waveform from 0ns to 180ns



Waveform from 180ns to 420ns