DSP Architecture Design
Final Project Presentation –
8 * 8 Output Stationary Systolic Array

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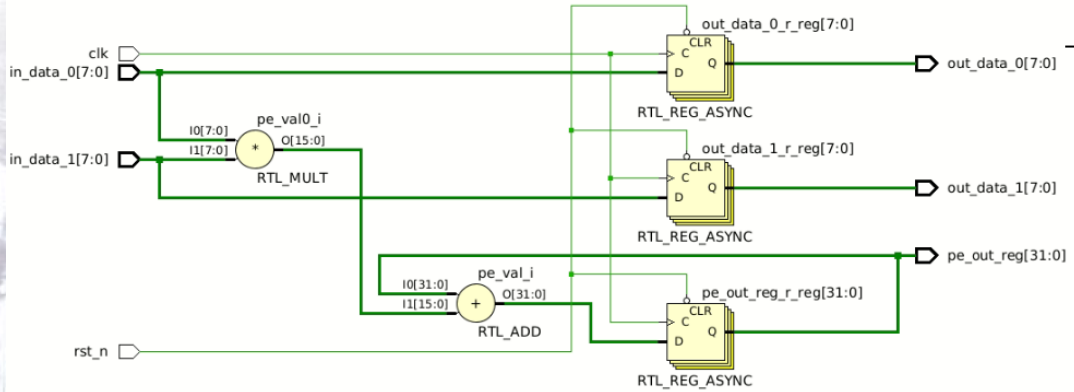
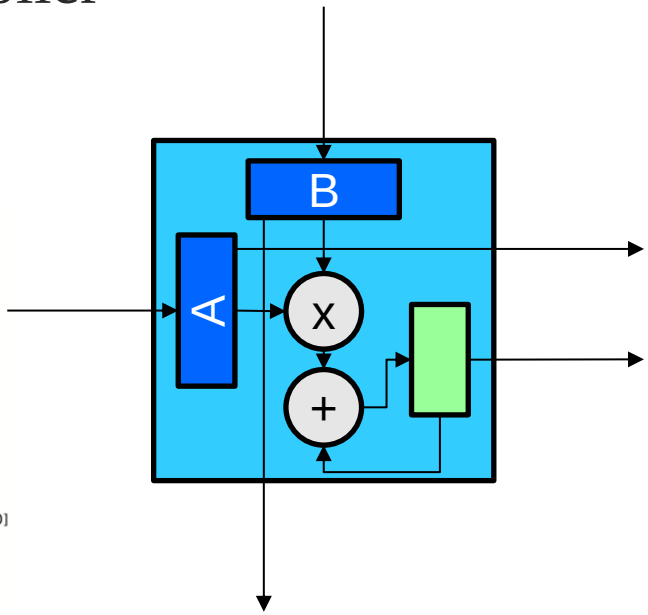
Outline

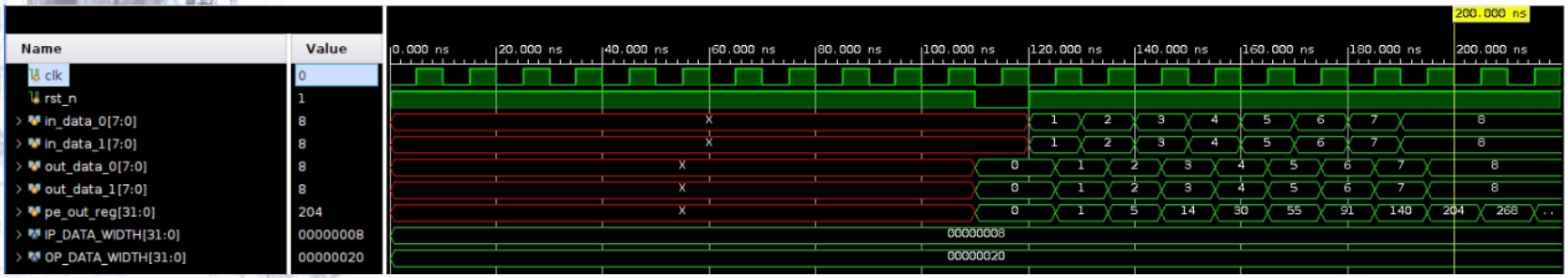
- PE (Processing Element)
- Output Stationary Systolic Array
  - Introduction
  - Simulation Waveform
  - Schematic
  - Utilization & Timing Report

PE (Processing Element)

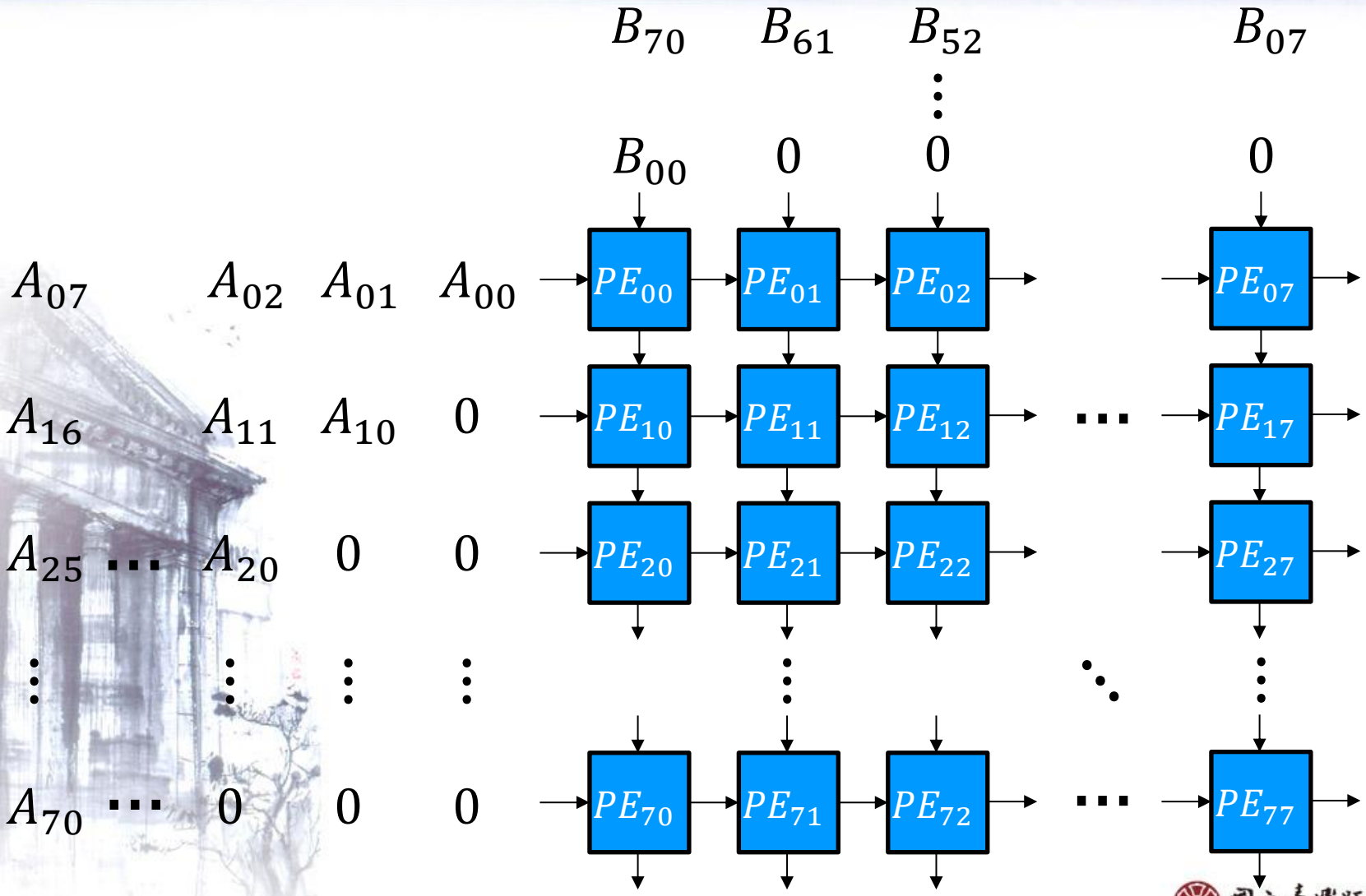
- Composed of one adder and one multiplier
- Operator datatype: uint8
- Output datatype: uint32



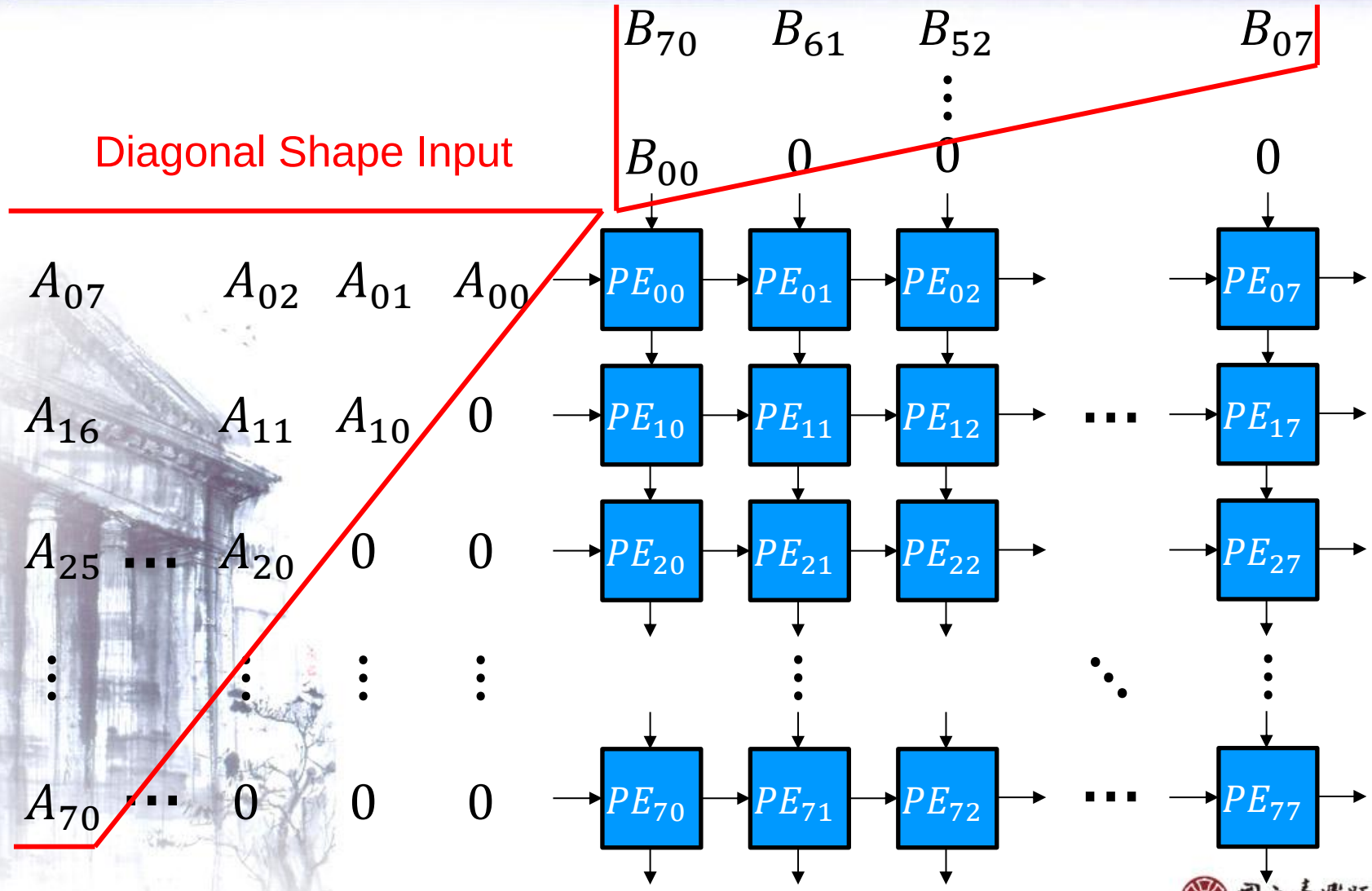




Output Stationary Systolic Array



Output Stationary Systolic Array



Output Stationary Systolic Array

- Simulation Waveform

Output Stationary Systolic Array

- Simulation Result

```
Column        0, Row 0, PASS!
Column        0, Row 1, PASS!
Column        0, Row 2, PASS!
Column        0, Row 3, PASS!
Column        0, Row 4, PASS!
Column        0, Row 5, PASS!
Column        0, Row 6, PASS!
Column        0, Row 7, PASS!
Column        1, Row 0, PASS!
Column        1, Row 1, PASS!
Column        1, Row 2, PASS!
Column        1, Row 3, PASS!
Column        1, Row 4, PASS!
Column        1, Row 5, PASS!
Column        1, Row 6, PASS!
Column        1, Row 7, PASS!
Column        2, Row 0, PASS!
Column        2, Row 1, PASS!
Column        2, Row 2, PASS!
Column        2, Row 3, PASS!
Column        2, Row 4, PASS!
Column        2, Row 5, PASS!
Column        2, Row 6, PASS!
Column        2, Row 7, PASS!
Column        3, Row 0, PASS!
Column        3, Row 1, PASS!
Column        3, Row 2, PASS!
Column        3, Row 3, PASS!
Column        3, Row 4, PASS!
Column        3, Row 5, PASS!
Column        3, Row 6, PASS!
Column        3, Row 7, PASS!
```

```
Column        4, Row 0, PASS!
Column        4, Row 1, PASS!
Column        4, Row 2, PASS!
Column        4, Row 3, PASS!
Column        4, Row 4, PASS!
Column        4, Row 5, PASS!
Column        4, Row 6, PASS!
Column        4, Row 7, PASS!
Column        5, Row 0, PASS!
Column        5, Row 1, PASS!
Column        5, Row 2, PASS!
Column        5, Row 3, PASS!
Column        5, Row 4, PASS!
Column        5, Row 5, PASS!
Column        5, Row 6, PASS!
Column        5, Row 7, PASS!
Column        6, Row 0, PASS!
Column        6, Row 1, PASS!
Column        6, Row 2, PASS!
Column        6, Row 3, PASS!
Column        6, Row 4, PASS!
Column        6, Row 5, PASS!
Column        6, Row 6, PASS!
Column        6, Row 7, PASS!
Column        7, Row 0, PASS!
Column        7, Row 1, PASS!
Column        7, Row 2, PASS!
Column        7, Row 3, PASS!
Column        7, Row 4, PASS!
Column        7, Row 5, PASS!
Column        7, Row 6, PASS!
Column        7, Row 7, PASS!
```

Output Stationary Systolic Array

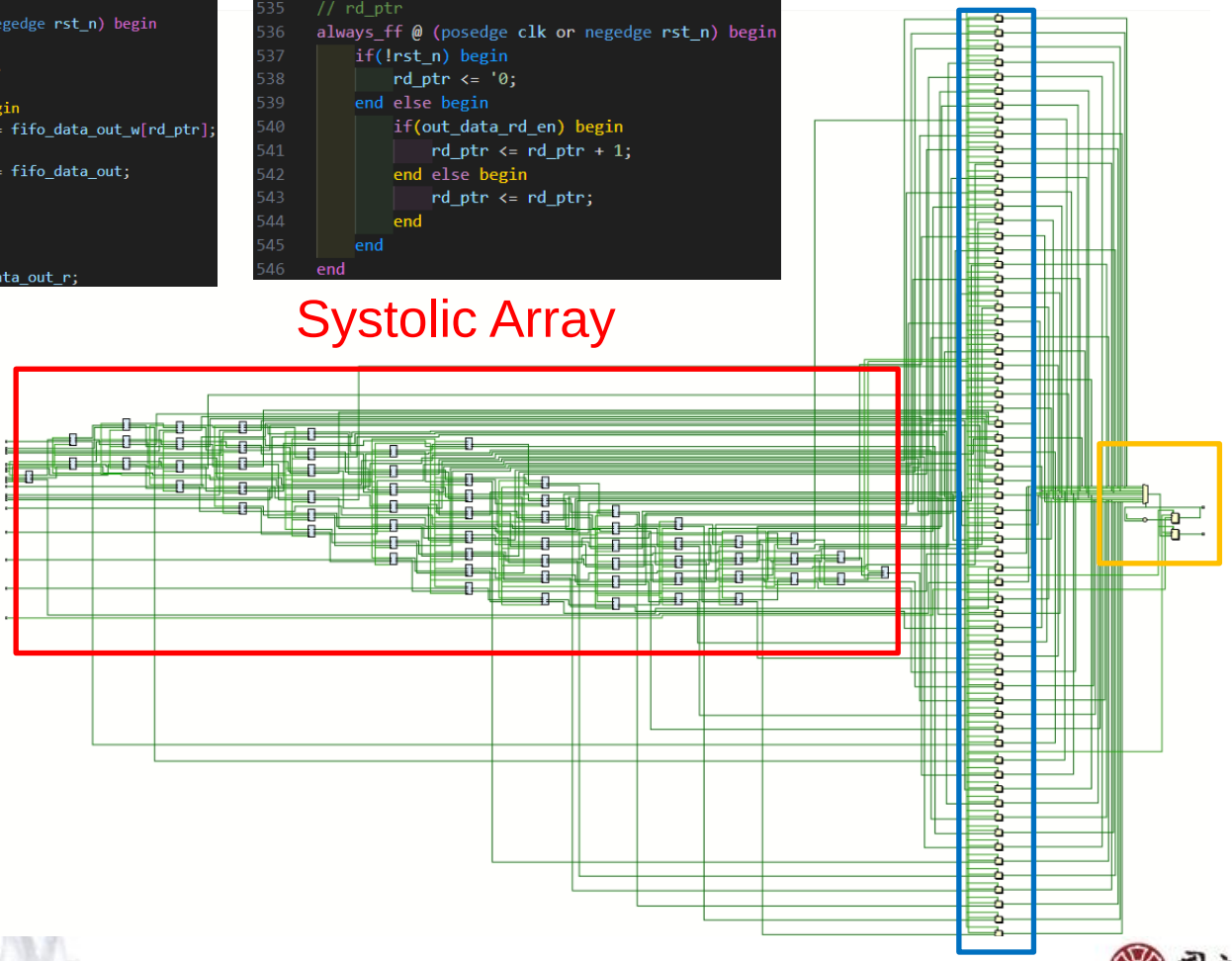
- Schematic

```
520  // fifo_data_out
521  always_ff @ (posedge clk or negedge rst_n) begin
522      if(!rst_n) begin
523          fifo_data_out_r <= '0;
524      end else begin
525          if(out_data_rd_en) begin
526              fifo_data_out_r <= fifo_data_out_w[rd_ptr];
527          end else begin
528              fifo_data_out_r <= fifo_data_out;
529          end
530      end
531  end
532
533  assign fifo_data_out = fifo_data_out_r;
```

```
535  // rd_ptr
536  always_ff @ (posedge clk or negedge rst_n) begin
537      if(!rst_n) begin
538          rd_ptr <= '0;
539      end else begin
540          if(out_data_rd_en) begin
541              rd_ptr <= rd_ptr + 1;
542          end else begin
543              rd_ptr <= rd_ptr;
544          end
545      end
546  end
```

Output Register

Systolic Array



FIFO – like output (rd_ptr & 8 column register)

Output Stationary Systolic Array

- Utilization & Timing Report

Resource	Estimation	Available	Utilization %
LUT	6015	63400	9.49
FF	5251	126800	4.14
IO	390	300	130.00
BUFG	1	32	3.13

FPGA Board: Xilinx Artix-7 XC7A100T
Clock Rate: 100 MHz
Setup Time Slack: 3.518ns

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.518 ns	Worst Hold Slack (WHS):	0.143 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	5123	Total Number of Endpoints:	5123	Total Number of Endpoints:	5252

All user specified timing constraints are met.

Name	Slack ^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	3.518	13	15	PE_00/out_data_1_r_reg[3]/C	PE_10/pe_out_reg_r_reg[31]/D	6.374	3.540	2.834	10.000	clk	clk
Path 2	3.518	13	15	PE_01/out_data_1_r_reg[3]/C	PE_11/pe_out_reg_r_reg[31]/D	6.374	3.540	2.834	10.000	clk	clk
Path 3	3.518	13	15	PE_02/out_data_1_r_reg[3]/C	PE_12/pe_out_reg_r_reg[31]/D	6.374	3.540	2.834	10.000	clk	clk
Path 4	3.518	13	15	PE_03/out_data_1_r_reg[3]/C	PE_13/pe_out_reg_r_reg[31]/D	6.374	3.540	2.834	10.000	clk	clk
Path 5	3.518	13	15	PE_04/out_data_1_r_reg[3]/C	PE_14/pe_out_reg_r_reg[31]/D	6.374	3.540	2.834	10.000	clk	clk
Path 6	3.518	13	15	PE_05/out_data_1_r_reg[3]/C	PE_15/pe_out_reg_r_reg[31]/D	6.374	3.540	2.834	10.000	clk	clk
Path 7	3.518	13	15	PE_06/out_data_1_r_reg[3]/C	PE_16/pe_out_reg_r_reg[31]/D	6.374	3.540	2.834	10.000	clk	clk
Path 8	3.518	13	15	PE_07/out_data_1_r_reg[3]/C	PE_17/pe_out_reg_r_reg[31]/D	6.374	3.540	2.834	10.000	clk	clk
Path 9	3.518	13	15	PE_10/out_data_1_r_reg[3]/C	PE_20/pe_out_reg_r_reg[31]/D	6.374	3.540	2.834	10.000	clk	clk
Path 10	3.518	13	15	PE_11/out_data_1_r_reg[3]/C	PE_21/pe_out_reg_r_reg[31]/D	6.374	3.540	2.834	10.000	clk	clk

Summary

Name	Path 1
Slack	3.518ns
Source	PE_00/out_data_1_r_reg[3]/C (rising edge-triggered cell FDCE clocked by clk {rise@0.000ns fall@5.000ns period=10.000ns})
Destination	PE_10/pe_out_reg_r_reg[31]/D (rising edge-triggered cell FDCE clocked by clk {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	clk
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns (clk rise@10.000ns - clk rise@0.000ns)
Data Path Delay	6.374ns (logic 3.540ns (55.538%) route 2.834ns (44.462%))
Logic Levels	13 (CARRY4=9 LUT4=1 LUT5=1 LUT6=2)
Clock Path Skew	-0.145ns
Clock Uncertainty	0.035ns

Critical Path:
From operator to PE output register
(1 uint8 multiplier + 1 uint32 adder)