Kevin Patel **Mob:-** 91-8105654387
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Work Experience

- **Senior Software Engineer at Yahoo** *(Aug 2010 onwards)*
  - Worked on New Yahoo Mail front-end.
  - Helped in various optimization integrating partner support for New Yahoo Mail.
  - Helped in supporting Multi Language support for the Product.
- **Linux System Administrator of VLSI Lab (250 users)** *(July 07 - July 2010)*
  - Configuring and administering NFS-server, NAS-BOX, two-level automated backup system, license servers, quota system, RAID arrays, etc.
  - Creating and maintaining user accounts, installing different softwares and troubleshooting various issues like network congestion, tool malfunctioning and other anomalies
  - Determining and implementing cost-effective and reliable solutions to many other problems like server upgradation, software procurement, memory and hard-disk management, etc.
  - Training junior system administrators

Awards and Achievements

- **Filed a patent for Yahoo :-** Applied for a patent at Yahoo, which got successfully approved for publishing.
- **Yahoo Best Ethical Hacker Award :-** Won HACKU, an institute level hacking competition organized by Yahoo, in which 250 teams participated.
- **Cultural Special mention by Hostel-12 :-** Awarded Special mention by council members of Hostel-12 for my noteworthy efforts in dance and music

M.Tech. Projects

- **Fault Simulation Acceleration using FPGA based Hardware Emulator** (Intel Project)
  (July 07 - June 09) *(guide:* **Prof. Madhav P. Desai***)*
  - In this approach a given circuit was partitioned into smaller circuits. Each of these partitions were evaluated using a differential algorithm
  - Since the fault simulation of a typical VLSI circuit may need several FPGAs, we implemented a multiboard multihost pipelined architecture and evaluated its performance using a performance model
  - The performance results were also validated by emulating a few ISCAS Benchmark circuits. The performance results for the same were also compared with our industry standard software fault simulator designed by me
- **Exploiting Parallelism & Pipelining in** *A Hardware Intermediate Representation (AHIR)*
  (July 2009 onwards) *(guide:* **Prof. Madhav P. Desai***)*
  - AHIR presents a complete flow which starts with an algorithm specified in a highlevel programming language (such as C) and ends with an RTL description of a circuit that implements the specified algorithm. This flow can be applied to a very large class of C programs
  - Currently the generated RTL description is not able to exploit parallelism. My goal is to exploit inherent parallelism and pipelining of hardware and thereby bring the performance of the generated RTL comparable to the hand-crafted RTL

Important Course Projects

- Designed **32-bit shift and add multiplier** with operating frequency optimization for Virtex-5 FPGA
- Designed **4x4 crossbar switch** with pipelined structure targeting Virtex-5 FPGA
- Design and Layout of **31 Stage Inverter Chain Ring Oscillator** in Magic for low area specification

Hobby Projects

- Designed **Alumni Information Database** using SQL and HTML
- Designed and Administered the **Department Election Website**
- Helped in designing Departmental **Online Quiz system**
- Implemented a fun project **Sir Log Detector** which notifies whenever sir will be logged in

Positions of Responsibility

- **Cultural Councilor of Hostel-12**
  - Efficiently led a **2-tier team of 7 secretaries** to organize all cultural activities in the hostel and economically managed cultural budget of INR 0.1 million
  - Organized over 10 workshops to bring out talent of hostel mates; which increased team participation in Inter Hostel GC tournaments
  - Member of the Institute Cultural Committee, headed by G.S. Cultural, which decides all the cultural activities of the Institute
- **Coordinator of ZOPP workshop** which was attended by more than 60 renowned faculties from elite colleges of the nation
- **PG representative in SARC-Phonathon**; An Alumni relationship development and fund-raising venture managed by students of IIT Bombay
- Volunteered in an international conference IWPSD at IIT Bombay which was attended by approximately 600 participants

Technical Skills

- **Languages:** VHDL, Verilog, Esterel, C, Advanced C++, JAVA, SQL
- **Important Packages:** GNU-Pth, NVIDIA-CUDA, YUI
- **Design Tools:** ModelSim, Xilinx, Spice, magic, MATLAB and various other tools of Cadence, Mentor-Graphics and Synopsys
- **Scripting and Documentation:** Shell, Perl, Python, LaTeX
- **Web-related:** HTML, PHP, Javascript

Extra Curricular Activities & Accolades

- Delivered lectures at institute level on **Linux and Vim** as a part of orientation sessions for juniors
- Worked as a Knowledge Executive in **PT-Education(MBA entrance coaching class)** for 2 months
- Represented Hostel-12 in **Gyrations-09**; inter-hostel dance competition
- Represented the department in 50-meter **swimming**; PG-sports(09)
- Represented Hostel-12 as **lead guitarist** in many cultural events
- Actively volunteered and motivated all the PGs for participating in **PG-Cult Festival**

Hobbies

- Dancing, Playing Guitar, Solving Rubik's Cubes