1061 Advanced VLSI HW2
Multirate Processing of Digital Signal

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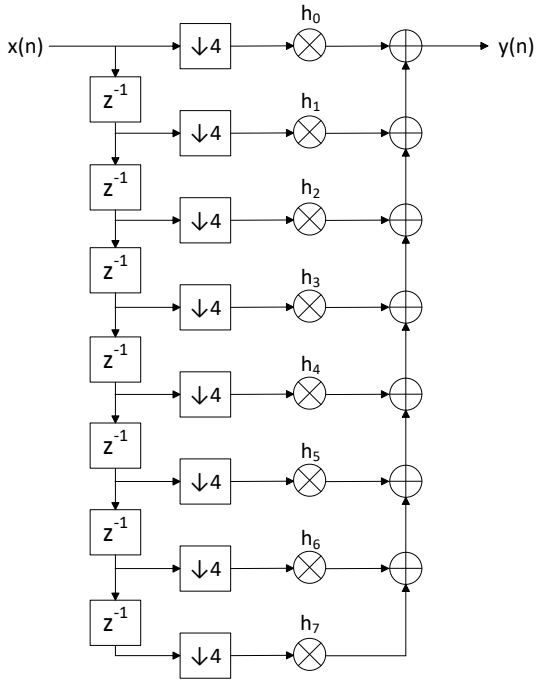
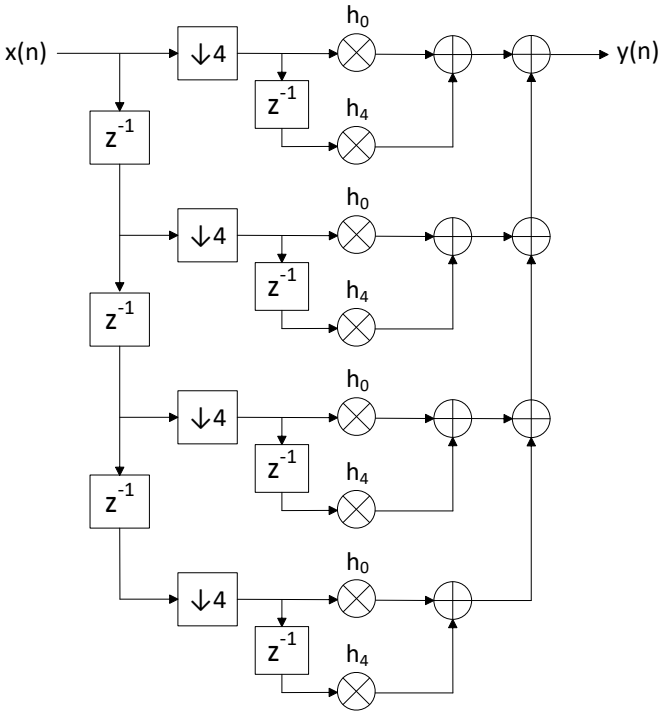
Question 1

I. Plot the RTL design of direct implementation" based on Direct-form 1 structure



II. Plot its equivalent RTL design based on "polyphase structure."



III. Compare these two RTL designs in terms of

A. Total complexity (no. of adders/multipliers/registers, etc.).

Ans:

- Direct form FIR: 7 register + 8 multiplier + 7 adder
- Short length FIR: 7 register + 8 multiplier + 7 adder

According to the analysis above, the total complexity is same with both implementation

(we skipped the down & up sample unit here, since the structure is unclear.)

B. Running clock rate of each adder/multiplier. Suppose that input clock rate of x(n) is 1G sample/sec.

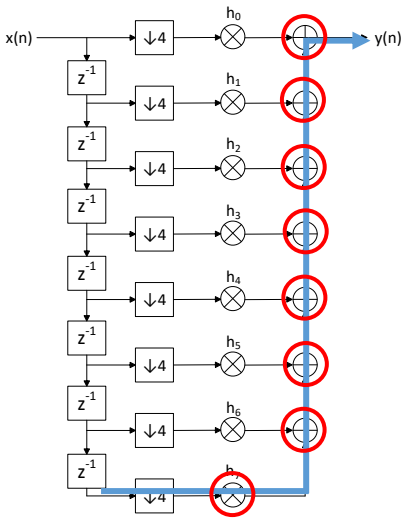
Ans:

- Direct form FIR: multiplier and adder both work after down sample → in 1G/4 = 0.25GHz
- Short length FIR: also in 0.25GHz

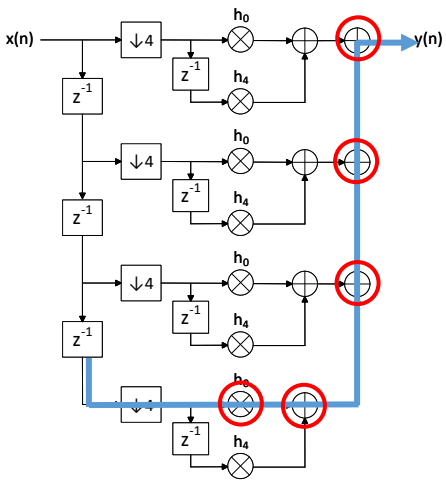
C. Your general comments on these two designs. E.g., comment on the redundant operation of "direct implementation." Why polyphaser design is better? What do you save and gain?

Ans:

The advantage we can take from short length implementation is the shorter critical path. Take a look at the block diagram:



a. Direct form FIR



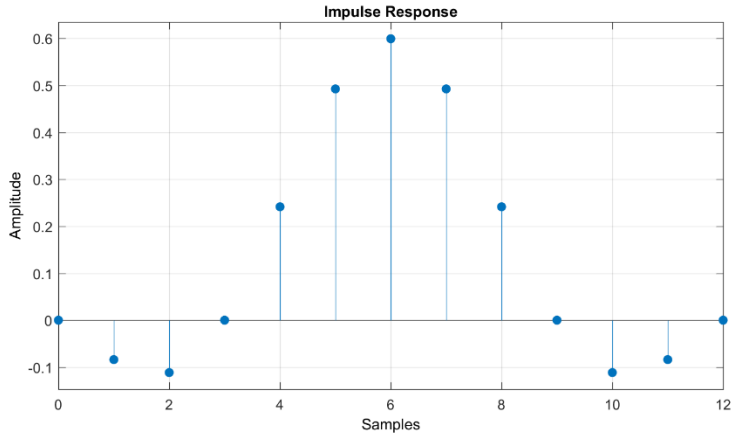
b. Polyphasor design FIR

Fig.a has critical path through 7 adder and 1 multiplier; Fig.b has critical path through 4 adder and 1 multiplier. Obviously, polyphasor design yield shorter critical path.

Question 2

I. Design a Raised-Cosine Filter based on Matlab program specified in (https://www.mathworks.com/help/signal/ref/rcosdesign.html?requested-Domain=www.mathworks.com) Create a normal raised-cosine filter with rolloff 0.25. Specify that this filter span 4 symbols with 3 samples per symbol, as shown on the right figure

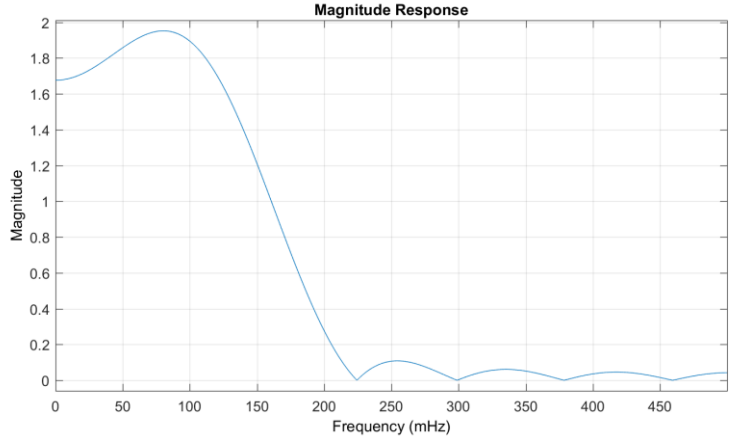
Ans:



II. Plot the frequency response of this raised-cosine filter. What is the value of its excess bandwidth, α? See definition of Excess Bandwidth on p.12 and p.13 of Lec6-2 slide.

Ans:

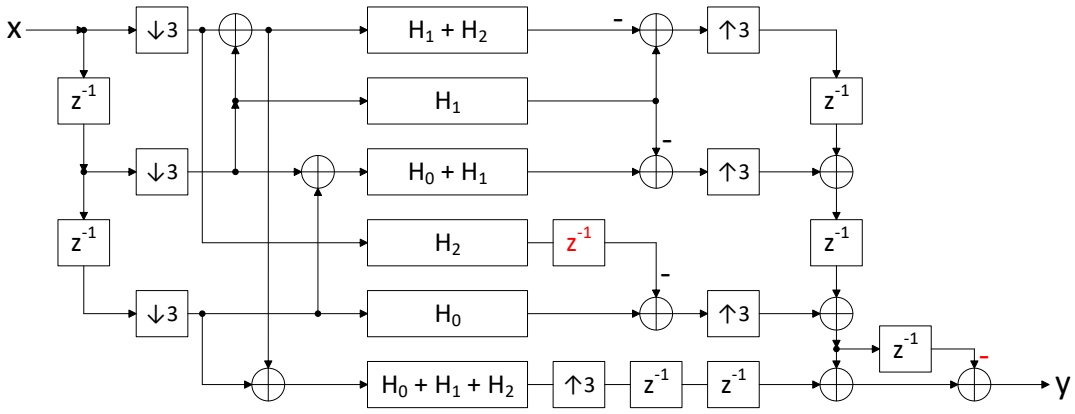
We can figure out from the impulse response pattern of such filter



We can measure the excess bandwidth α = 0.25

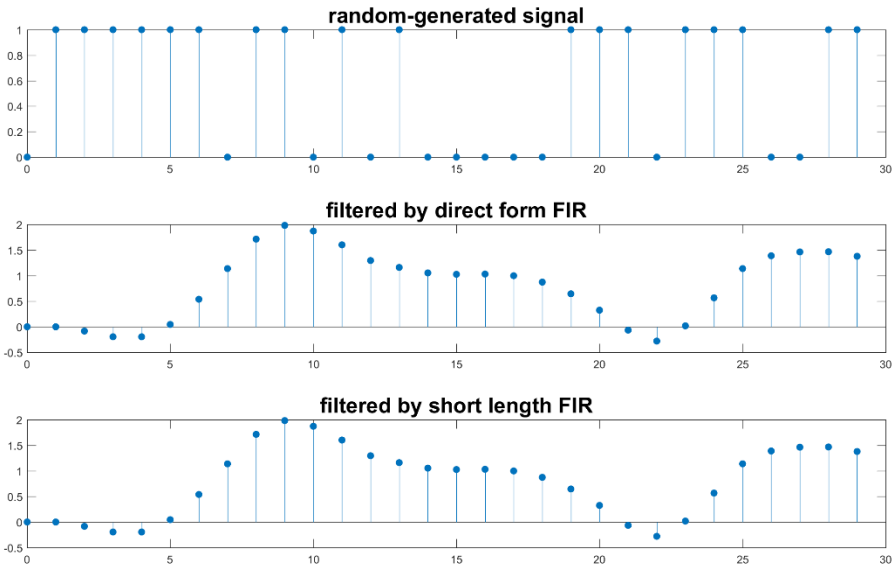
Question 3

I. Validate the RTL design of short-length FIR filter with M = 3 on Lec4.21. Is it correct? Or the design on Lec4.21 needs modification? If so, please check the slide on Lec4.21 and re-design it.



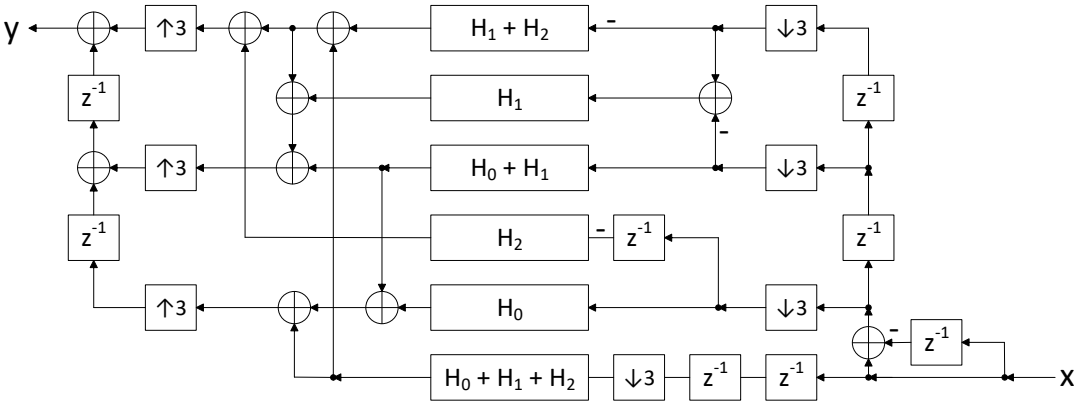
(error in original figure had been modified and marked with red)

II. Verify the RTL design of short-length FIR filter with M = 3 on Lec4.21, by using a filter design with coefficients of the above Raised-co-sine filter. That is, run a Matlab program to verify the RTL design on Lec.4.21, by comparing its filtering results with a normal M=1 (direct im-plementation) FIR filter. Show **the first 30 filtering results** of your Matlab program of both M=3 and M=1 filters.



III. Derive the “transpose architecture” of the correct Lec4.21. Then, re-run the Matlab. Show **the first 30 filtering results** of your Matlab program of both *M=3 (transposed form)* and *M=1 (direct implementation)* filters.

A. Transposed architecture



B. First 30 filtering results (input = random generated binary signal)