Kai-Chieh (Kevin) Hsu

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Research Interests

Signal Processing sparse signal processing, array signal processing and compressed sensing

Machine Learninghealthcare applications, privacy and security issuesVLSI Designlow-power architecture design and ASIC implementation

Education

Princeton UniversityPh.D. in Electrical Engineering

Princeton, NJ

Sept. 2019 - PRESENT

National Taiwan University (NTU)

Taipei, Taiwan

B.S. in Electrical Engineering

Sept. 2014 - Jan. 2019

Achieved 4.19/4.30 overall GPA and 4.19/4.30 major GPA.

• Ranked in top 5% by cumulative GPA

Research Experiences

ECG Real-Time Telemonitoring with Compressed Analysis

NTU, Taiwan

Access IC Lab (Prof. An-Yeu (Andy) Wu, IEEE Fellow)

Aug. 2017 - Mar. 2019

- Edge Classification: Incorporated compressed sensing (CS), task-driven dictionary learning (predictive sparse coding) and PCA to render light-weighted classifier and overcome limited labeled data challenge
- On-Demand Recovery: Design a two-stage algorithm to classify and then reconstruct only problematic signals, utilizing the information from classification stage to speed up the reconstruction algorithm
- Hardware Design and Chip Implementation: Propose a hardware architecture for on-demand recovery to allow hardware sharing between classification and reconstruction algorithms

Direction-of-Arrival (DOA) Estimation

NTU, Taiwan

Group of Electromagnetic Applications (Prof. Jean-Fu Kiang)

Feb. 2017 - Mar. 2019

- Antenna Uncertainty: Utilized special matrix structure with Khatri-Rao subspace-based MUltiple Signal Classification (MUSIC) to improve immunity to uncertainties and detect DOAs with sensors half the number of sources
- More Sources Than Sensors: Proposed a new antenna array structure to increase the detectable number of sources based on fourth-order statistics and compressive sensing approach
- Mixed Carrier Frequency (CF) Known and Unknown Sources: Proposed a two-step algorithm to first estimate DOA of known sources and then joint estimate the DOA and CF of unknown sources
- Near Sea Surface Environment: Consider the influence of multipath propagation (coherent signal) and sea clutter (backscattered signal from the sea surface)

Publications

Accepted

[6] Joint Estimation of DOA and Frequency From A Mixture of Frequency Known and Unknown Sources with Orthogonal Coprime Arrays |

Jan. 2019

K.-C. Hsu and J.-F. Kiang

K.-C. Hsu and J.-F. Kiang

Sensors, 19(2), 335

[5] Low-Complexity Compressed Analysis in Eigenspace with Limited Labeled Data for Real-Time Electrocardiography Telemonitoring

Anaheim, CA Nov. 2018

K.-C. Hsu, B.-H. Cho, C.-Y. Chou and A.-Y. (Andy) Wu

IEEE Global Conference on Signal and Information Processing (GlobalSIP)

[4] Joint Estimation of DOA and Carrier Frequency Based on Coprime Arrays

Toyama, Japan Aug. 2018

Progress In Electromagnetics Research Symposium (PIER S)

[3] DOA Estimation With Triply Primed Arrays Based on Fourth-Order Statistics | 🖾

Boston, MA

July 2018

K.-C. Hsu and J.-F. Kiang *IEEE AP-S Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*

[2] DOA Estimation Using Triply Primed Arrays Based on Fourth-Order Statistics

K.-C. Hsu and J.-F. Kiang

Mar. 2018

Progress In Electromagnetics Research M, Vol. 67, pp. 55-64

[1] DOA Estimation of Quasi-Stationary Signals Using a Partly-Calibrated Uniform Linear Array with Fewer Sensors Than Sources

K.-C. Hsu and J.-F. Kiang

Progress In Electromagnetics Research M, Vol. 63, pp. 185-193

Under Review

• C.-Y. Chou, **K.-C. Hsu**, B.-H. Cho, K.-C. Chen and A.-Y. (Andy) Wu, "Low-Complexity On-demand Reconstruction for Compressively Sensed Problematic Signals," submitted to *IEEE Trans. Signal Process.*, Apr. 2019.

Honors & Awards.

3rd Prize in Integrated Circuit Design Contest

Ministry of Education, Taiwan

• Out of about 300 teams

July 201

2nd Prize in Taiwan Creative Electromagnetic Implementation Competition

High-speed RF and mm-Wave Tech. Center, Taiwan

• Under the supervision of Prof. Tzong-Lin Wu, IEEE Fellow

 Implemented an electromagnetic structure longer than 2.5 m with only stationery and achieved -7.8 dB insertion loss at 3 GHz | △

Aug. 2017

June 2018

Jan. 2018

8th place in Data Structure and Programming Contest

Cadence, Taiwan

· Out of about 250 students

Mar. 2017

Digital IC Design Certificate

National Chip Implementation Center, Taiwan

• Familiar with Verilog, logic synthesis, simulation, STA and cell library

Nov. 2018

Graduate Representative in NTUEE graduate ceremony
Given to top ten students of four years

Dept. of EE, NTU, Taiwan

Professor Chun-Hsiung Chen Scholarship

Electromagnetic Industry-Academia Consortium, Taiwan

• Rewarded outstanding performances in electromagnetic fields

Jan. 2018

Presidential Awards $\times 2$

Dept. of EE, NTU, Taiwan

• Given to top ten students of that semester

second semester of 2014 and 2016

Selected Course Projects

Survey of Dictionary Learning | 🕒

Mathematical Principles of Machine Learning

team project June 2018

- Contribution: served as the **project speaker** and surveyed predictive dictionary learning and sparse coding optimization
- · Studied generalization bound of reconstructive and predictive dictionary learning
- · Studied optimization algorithm of dictionary learning, including MOD, ODL, K-SVD and TDD
- Studied sparse coding optimization algorithm, including sub-gradient descent, ISTA and FISTA

An Analysis of Deep Neural Networks in Hardware Perspective \mid \triangle

Advanced Integrated Circuit Design

Python, team project Jan. 2018

- Contribution: served as the **leader** to distribute work and surveyed the structure of residual net, Inception v4 and Xception
- Reviewed many state-of-the-art very deep CNNs, including AlexNet, VGG net, Inception, ResNet and Xception
 Analyzed with estimation accuracy and resource consumption and provided insight of hardware-friendly designs
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Different Handover Policies in Different Environments |

Intro. to Wireless and Mobile Networking

Matlab, team project June 2017

- $\bullet \ \ \ \ \text{Contribution: served as the } \textbf{project speaker}, conducted simulations and analyzed results$
- · Proposed four different handover policies and compared performances among different environments
- Provide two different channel models and different mobility pattern of mobile stations

Pipelined MIPS CPU |

Verilog, team project

Computer Architecture

June 2017

NTU, Taiwan

• Contribution: served as the **leader** to distribute work, design whole structure and implement basic function of CPU

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- Implemented a pipelined MIPS CPU with support of multiplication and division and overcame data hazard and branch hazard
- Implemented a synthesizable pipelined MIPS CPU overcoming data hazard, load-use hazard and branch hazard
 Advanced with branch prediction, L2 cache and support of multiply and divide instructions

Working Experiences

Research Assistant

Access IC Lab (Prof. An-Yeu (Andy) Wu, IEEE Fellow) Feb. 2018 - Dec. 2018

Teaching Assistant NTU, Taiwan

Digital System Design Feb. 2018 - June 2018