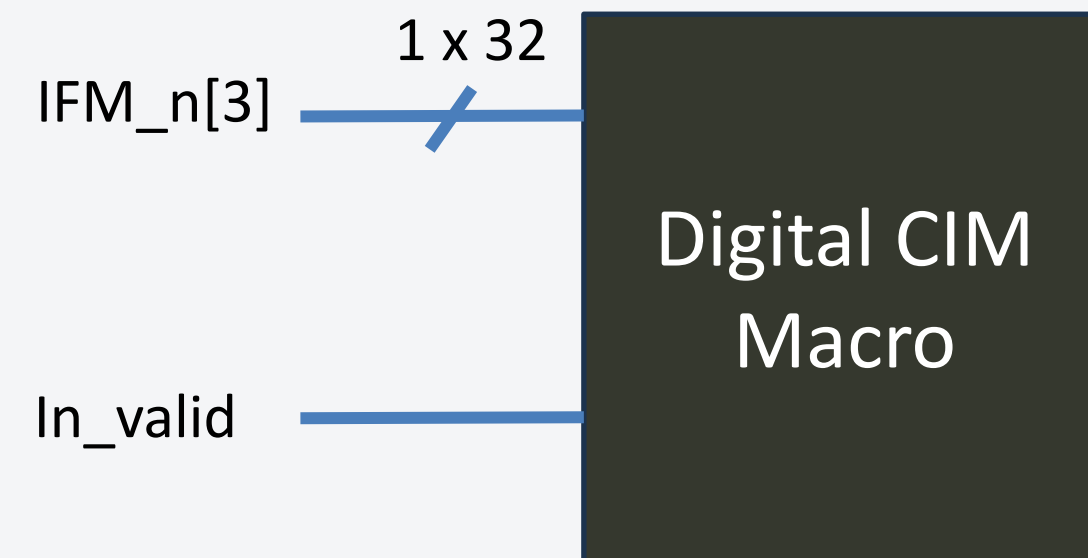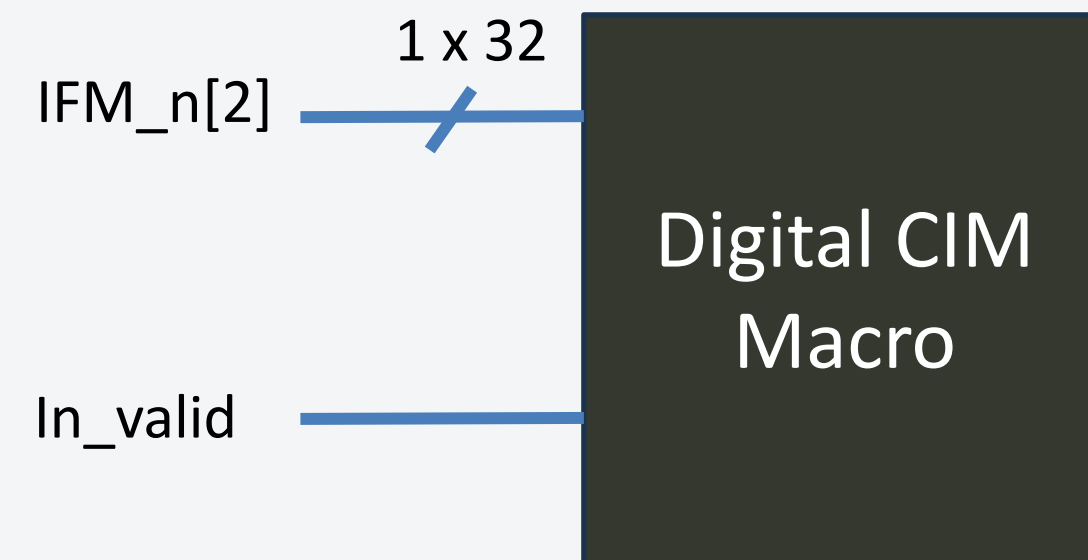# Serial Input

Clock period   : 449 ps
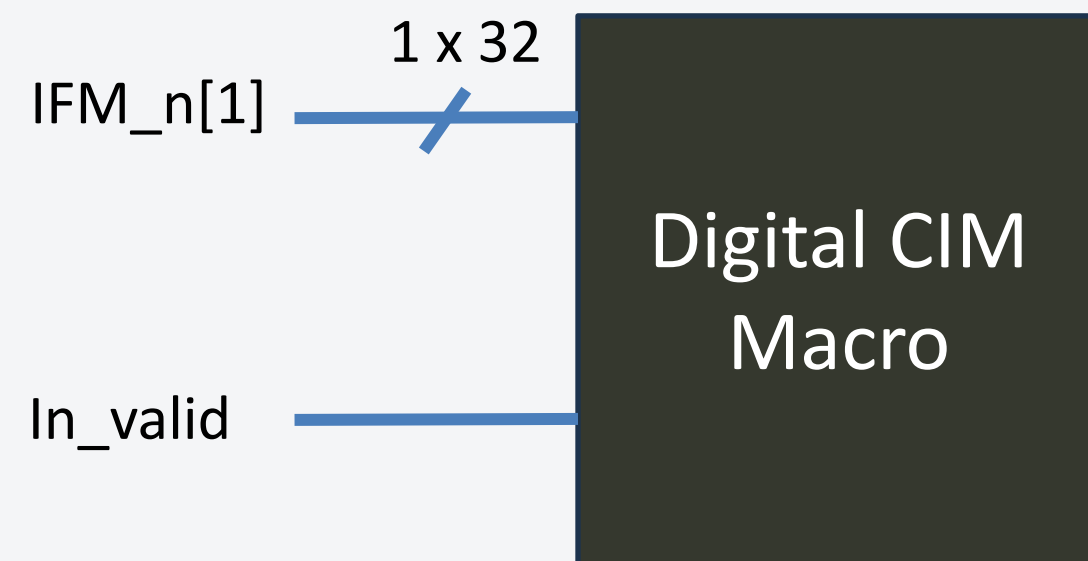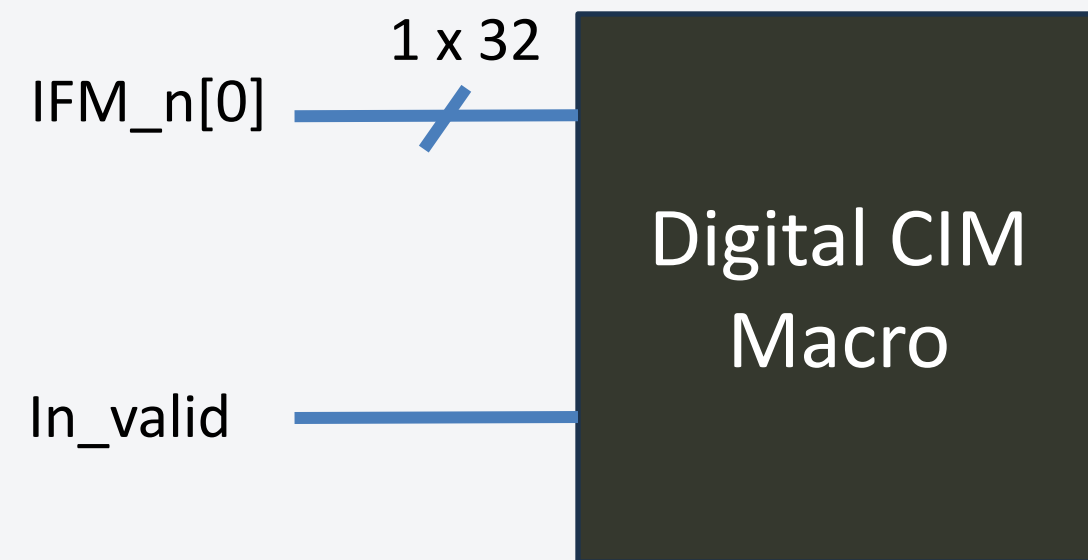
Throughputs   : 0.709 GOPS

Power efficiency : 3.5 TOPS/W

Area efficiency   : 6.376 E-13 TOPS/mm2

Serial Input Pattern

IFM_n[0] — 1 x 32 — Digital CIM Macro
In_valid — Digital CIM Macro

IFM_n[2] — 1 x 32 — Digital CIM Macro
In_valid — Digital CIM Macro

IFM_n[1] — 1 x 32 — Digital CIM Macro
In_valid — Digital CIM Macro

IFM_n[3] — 1 x 32 — Digital CIM Macro
In_valid — Digital CIM Macro

System Structure Graph
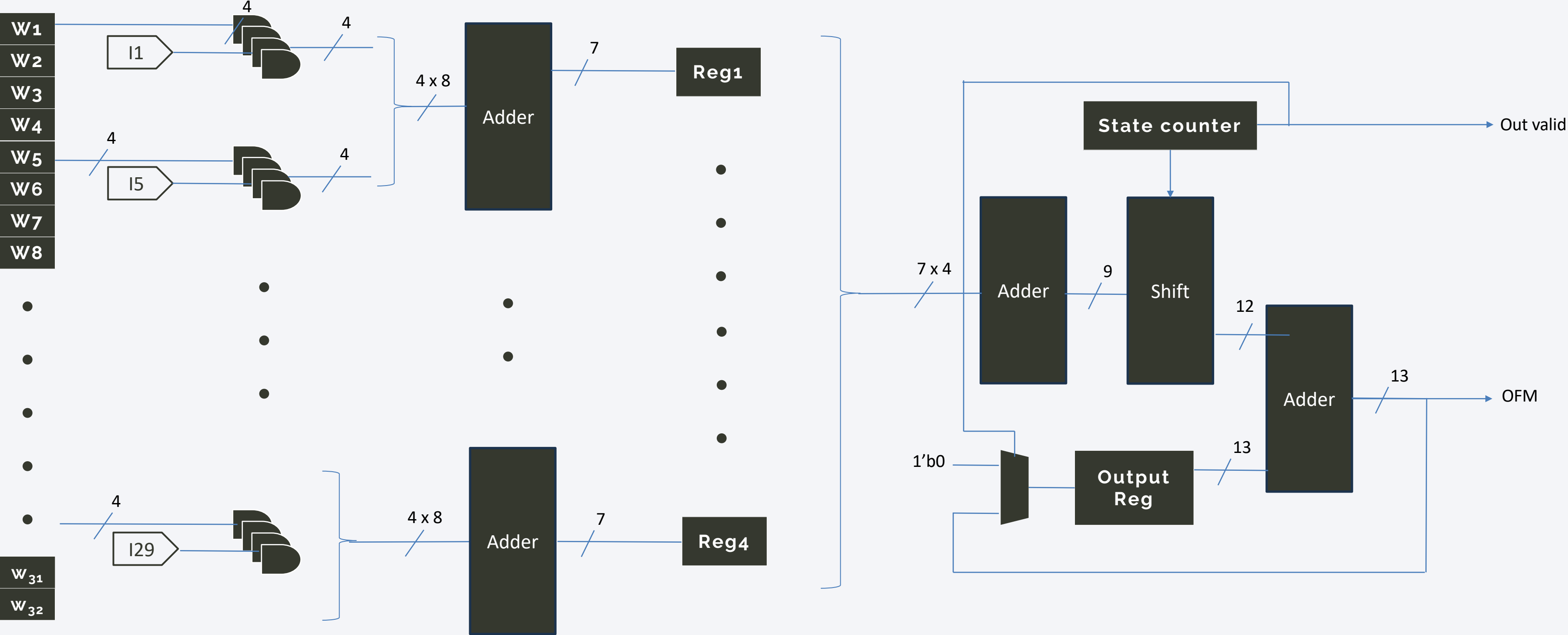
Design trade-off

No pipeline with CG :

Total cell area: 1938.790081

Total Power   4.105e-05

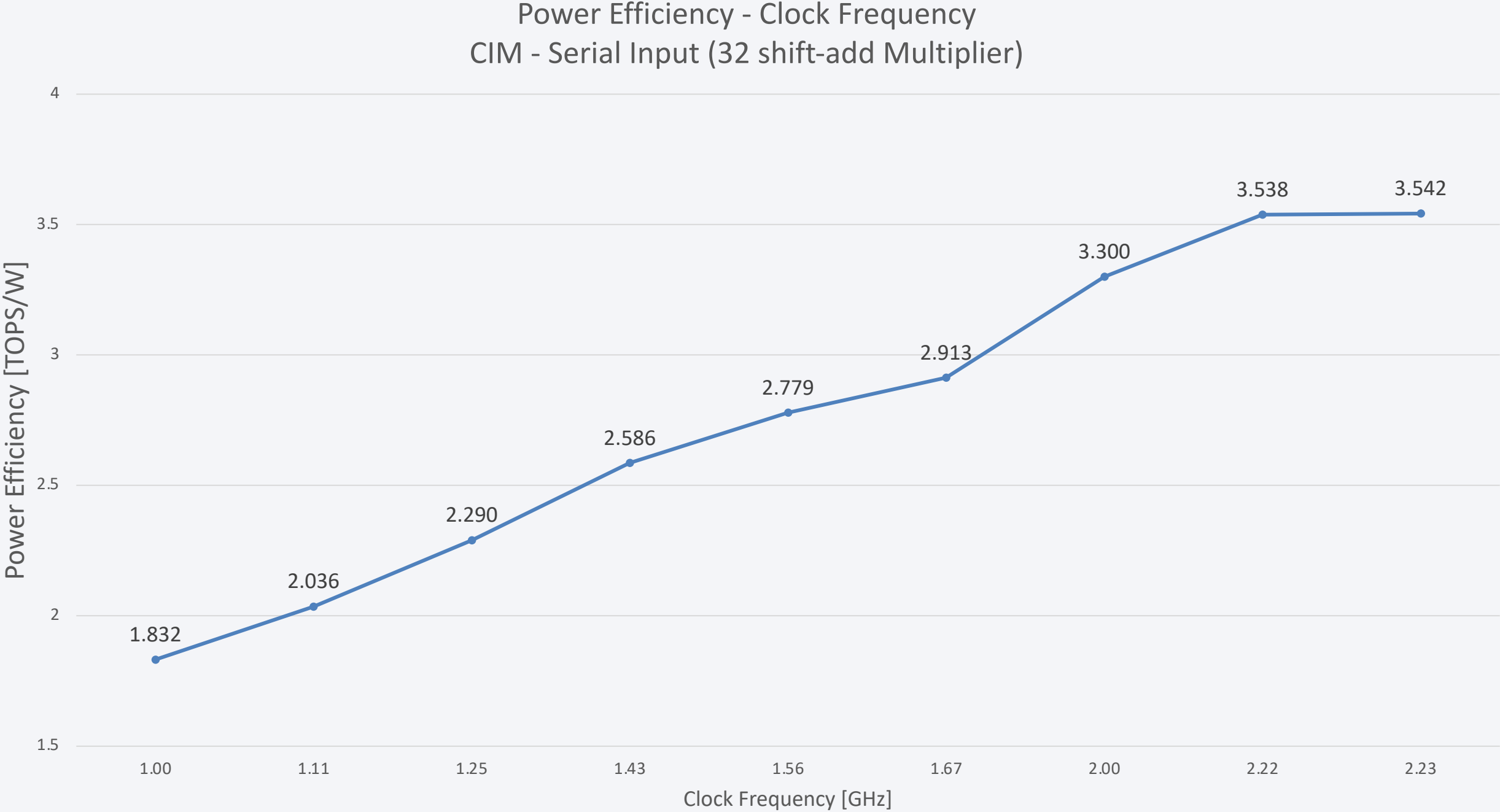No pipeline without CG:

Total cell area: 1937.623681

Total Power   4.995e-05

```verilog
// CG
ICGx3_ASAP7_75t_R CG_U1(
    .CLK(clk),
    .ENA(0),
    .SE(in_valid),
    .GCLK(clk_gate_IN1)
);
```

```verilog
always @(posedge clk) begin
    if (in_valid) begin
        /*
        ...
        ...
        */
    end
end
```

```verilog
always @(posedge clk_gate_IN1) begin
    /*
    ...
    ...
    */
end
```

Design trade-off

Power Efficiency - Clock Frequency
CIM - Serial Input (32 shift-add Multiplier)

Design trade-off

Area Efficiency - Clock Frequency
CIM - Serial Input (32 shift-add Multiplier)