Metal Oxide Field Effect Transistor

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Pre-lab Field Effect Transistor

Problem 1:Metal Oxide Semiconductor Field Effect Transistors

Question 1

The difference is that an Enhancement MOSFET does not exist from source to drain; therefore, no current flows at zero gate voltage. Whereas Depletion MOSFET has one. In an Enhancement MOSFET ,when positive voltage is applied to the gate, it will induce a channel by flowing minority carriers (electrons) from P-type bulk into the concentrated layer. Whereas a Depletion MOSFET, the channel will have positive charge induced in it – this results in the depletion of majority carriers (electrons) and hence reduction in conductivity.

Question 2

Difference between an NMOS and a PMOS transistor is that for a NMOS transistor, the current flowing in the channel Is due to the electrons whereas the flow of holes causes the current flow in a PMOS transistor.

Problem 2:MOSFET as an Amplifier

$$V_{GS} + I_{DS} \times R_S = 5V \tag{1}$$

$$I_{DS} = k \times (V_{GS} - V_{th})$$

$k = 0.5\ V_{th} = 1V\ R_S = 6^3$

$$I_{DS} = \frac{5V - 2V}{6^3}$$

$I_{DS} = 0.5mA$

$$V_{DS} + 2 \times I_{DS} \times R_S = 10V \tag{2}$$

$\therefore V_{DS} = 4V$

Question 2

For the MOSFET to operate in the saturation region:

$$V_{DS} > V_{GS} - V_{th} \tag{3}$$

Since the above operation holds($4 > 1$)the MOSFET operates in the saturation region

Problem 3:MOSFET as Switch

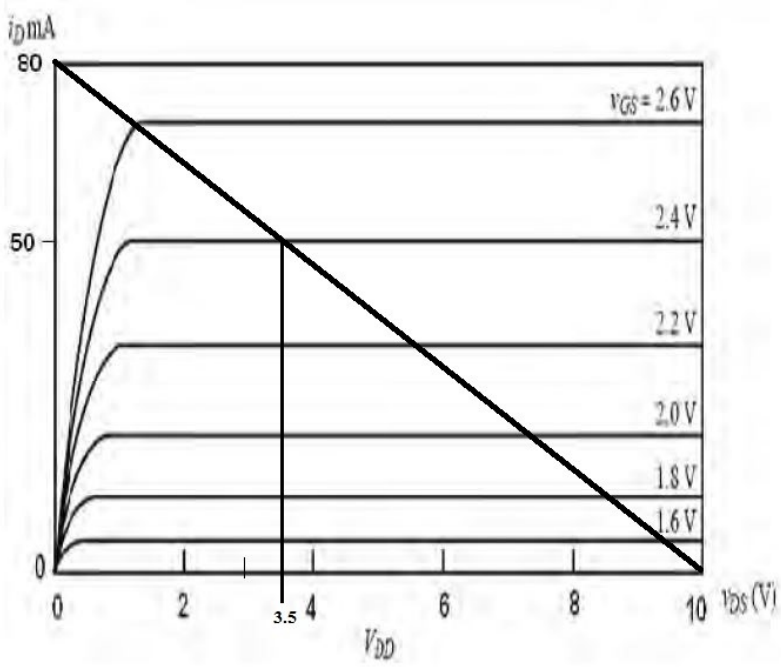


Figure 1: The graph shows the characteristics of the MOSFET as a switch

From the graph above the operating point of both inputs are as follows, when : $V_{GS} = 0$ $I_D = 0$ $V_{DS} = 10$ **and** $V_{GS} = 2.4V$ $I_D = 50mA$ $V_{DS} = 3.5V$

Pre-lab CMOS Inverters and Logic Gates

Problem 1:Voltage Transfer Characteristic of a CMOS inverter

Question 1

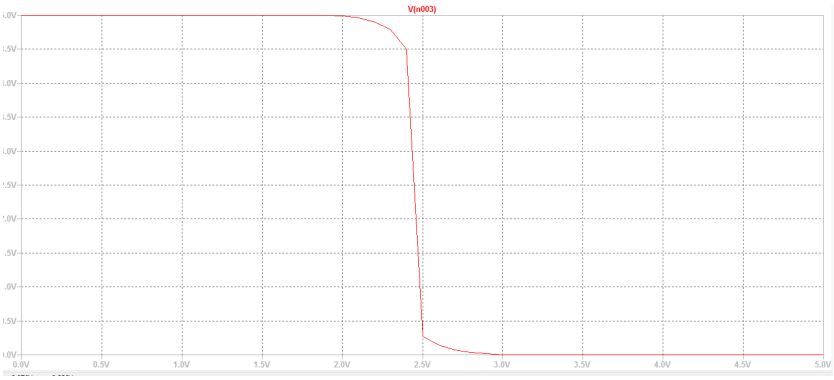


Figure 2: The graph shows V_{out} against V_{in},where $V_{OH} = V_{DD} = 5V V_{OL} = 0V, V_{th} = 2.4V$,$N_{ML} = 2.24V, N_{MH} = 2.42V$.

Question 2

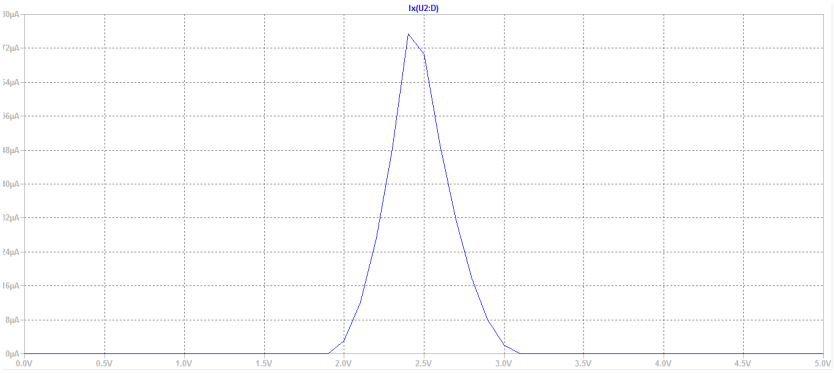


Figure 3: The graph shows the current flowing through the input as a function of the input voltage.

Question 3

The current reaches a maximum of 2.42 V.Which is approximately the theoretical value $V_{th} = \frac{V_{DD}}{2}$.The inverter is switching between states so none of the transistors is turned off so current flows through the two of them.

Problem 2:CMOS Inverter with Capacitive Load

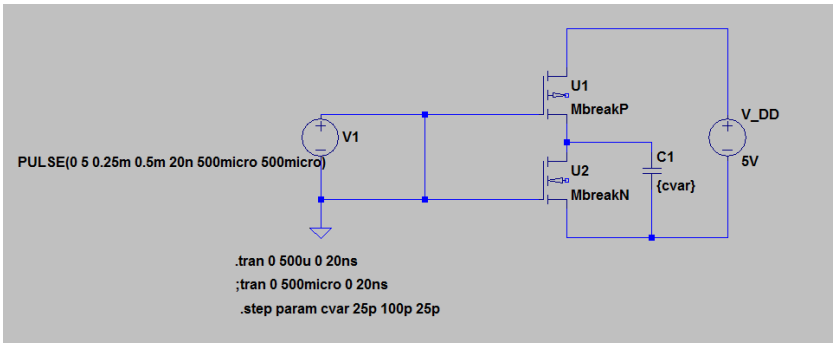


Figure 4: The figure shows the implemented circuit.

Question 1

Table 1: The table shows the different t_{PHL} for the different capacitors

C/pF	25	50	75	100
t_{PHL}/ns	31.3	53.8	76.2	98.0
t_{PLH}/ns	45.3	80.7	115.826	150.9

Question 2

$$P_D = f \times C \times V_{DD}^2 \tag{4}$$

$f = 1kHZ$
$VDD = 5V$

C varies from 25 pF to 100pF.

Table 2: The table shows the the dynamic power dissipation of the CMOS inverter for the different load capacitors.

C/pF	25	50	75	100
Power/μW	0.625	1.25	1.875	2.5

Problem 3:Propagation Delay of an Inverter Stage

Question 1

$$t_d = \frac{1}{2NF} \tag{5}$$

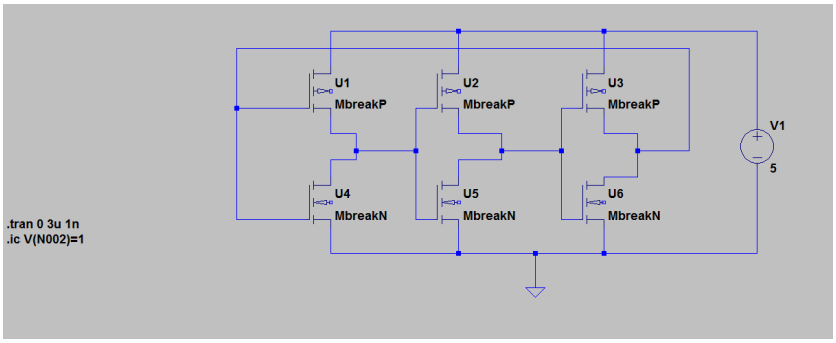


Figure 5: The figure shows the implemented circuit.

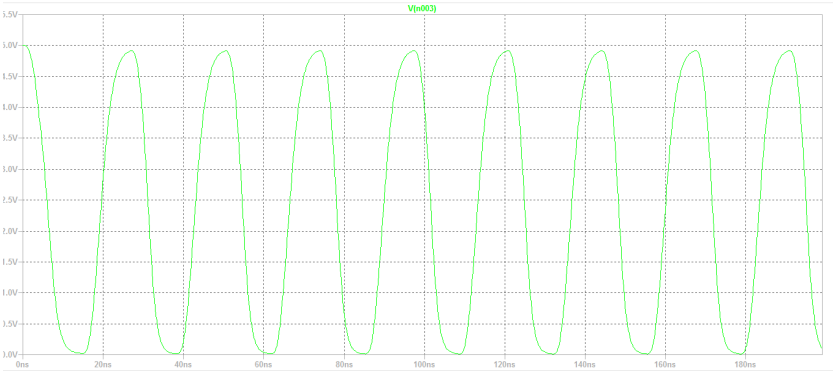


Figure 6: The graph shows the oscillation frequency is 7.029 MHz.The propagation delay using the formula is 2.37 ns.Where $V_{DD} = 3V$

Where N=3 (number of stages)and F is the oscillation frequency.

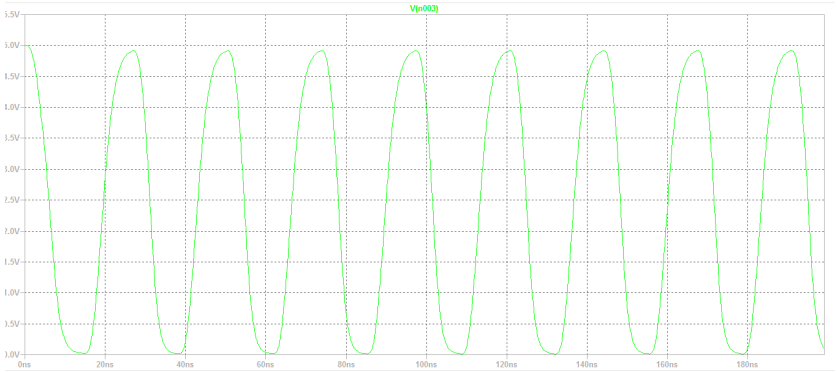


Figure 7: The graph shows the oscillation frequency is 42.86 MHz.The propagation delay using the formula is 3.89 ns.Where $V_{DD} = 5V$

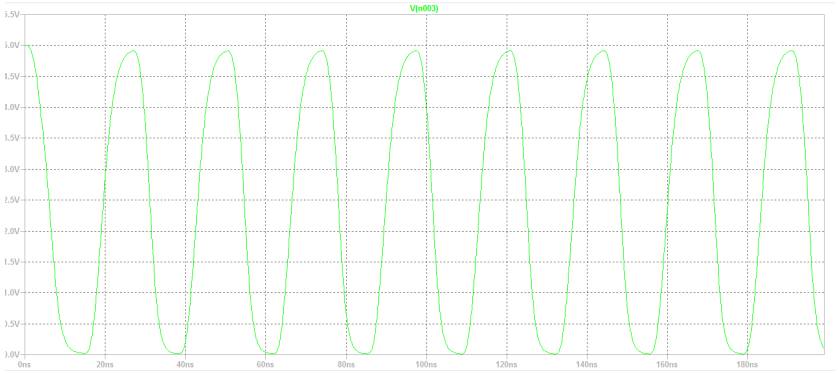


Figure 8: The graph shows the oscillation frequency is 95.04 MHz.The propagation delay using the formula is 1.75 ns.Where $V_{DD} = 7V$

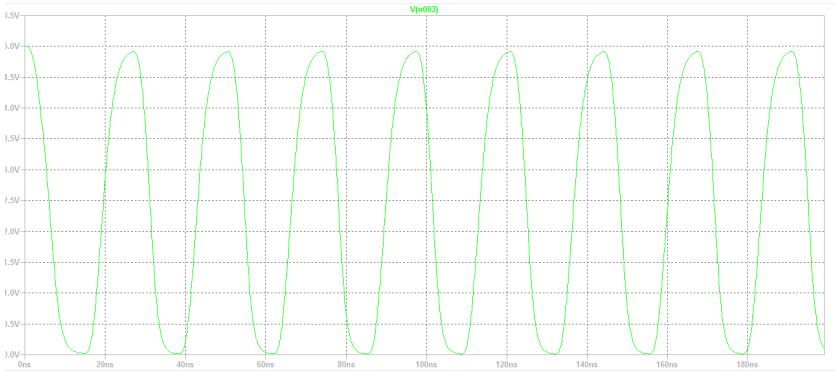


Figure 9: The graph shows the oscillation frequency is 211.5 MHz.The propagation delay using the formula is 0.79 ns.Where $V_{DD} = 10V$

Question 2

To calculate the dynamic power dissipation per inverter stage we use the formula below :

$$P_D = f \times C \times V_{DD}^2 \tag{6}$$

Table 3: The table shows the results.

P_D/mW	V_{DD}/V	f/MHz
6.32	3	7.029
10.7	5	42.86
46.5	7	95.04
211.5	10	211.5

Where f is the oscillation frequency.C is the capacitance and V_{DD} is the power supply.From the data sheet we use 10 pF for the capacitance.V_{DD} and f will vary.

Question 3

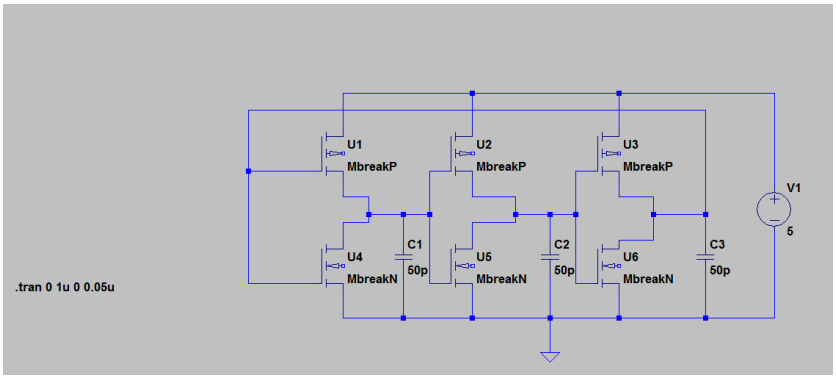


Figure 10: The figure shows the implemented circuit.

Question 4

When there is a capacitive load at the output of each inverter, there is an increase in the input capacitance,which produces a large propagation delay and a smaller oscillation frequency .

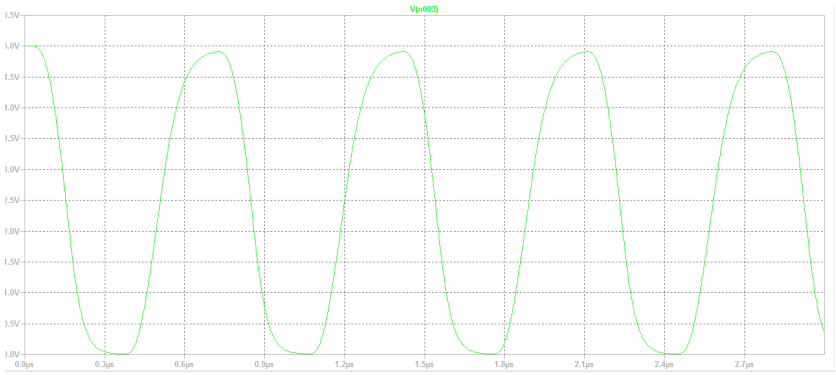


Figure 11: The graph shows that the oscillation frequency is 1.416 MHz and the propagation delay using the formula is 117.02 ns.

Question 5

From the power dissipation formula we $P_D = f \times C \times V_{DD}^2$we can see that the power dissipation is directly proportional to the capacitive times the square of the power supply.Therefore an increase in the product of the load capacitance and the square of the power supply will be an increase in the power dissipation.The same applies for the decrease in the product.

Problem 4:Logical Gate

Table 4: Table shows truth table of and XOR with two inputs

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

$$p \oplus q = (p \vee q) \wedge \neg(p \wedge q) \tag{7}$$

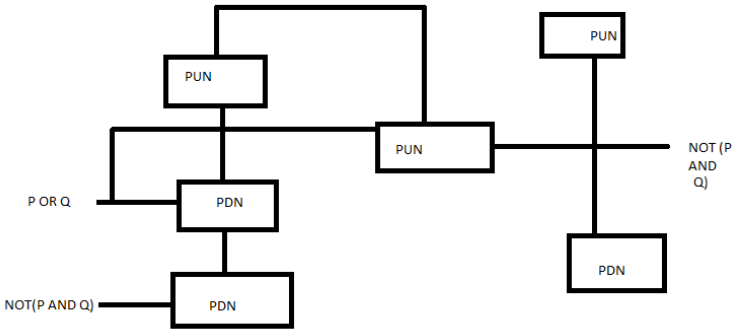


Figure 12: The figure shows the circuit of the equation above.

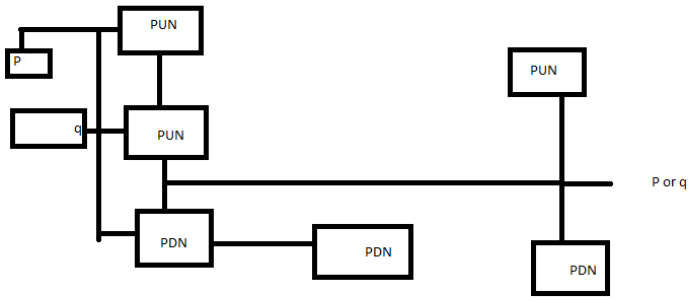


Figure 13: The figure shows the circuit of $p \vee q$.

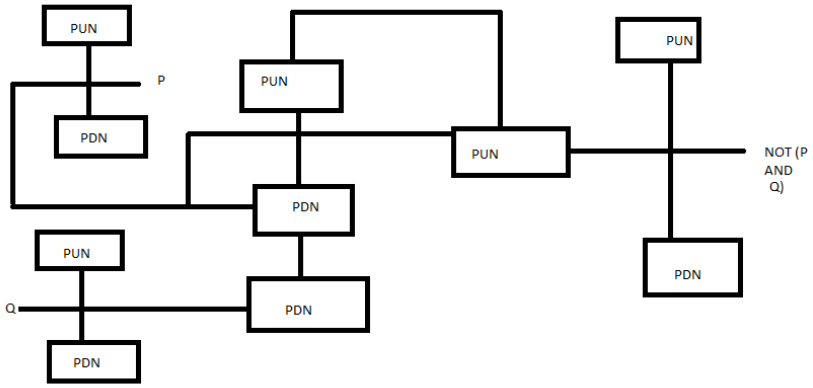


Figure 14: The figure shows the circuit of $p \vee q$.

Execution

Problem 1:Current/Voltage Characteristic of a MOSFET

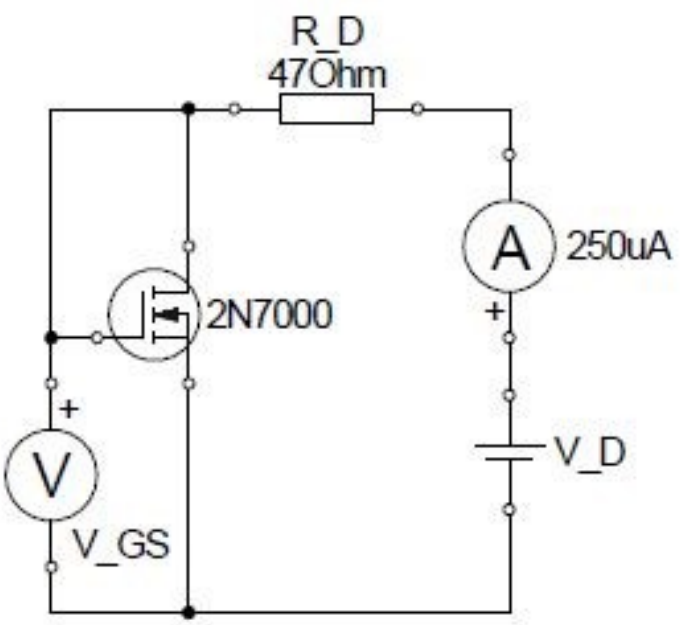


Figure 15: The figure shows the implemented circuit.

$Uth = UGS = UDS$

When $I_D = 250\mu A$ $Uth = UGS = UDS$.The recorded values for Uth and ID is : $Uth = 2.004 VID = 250.5\mu A$

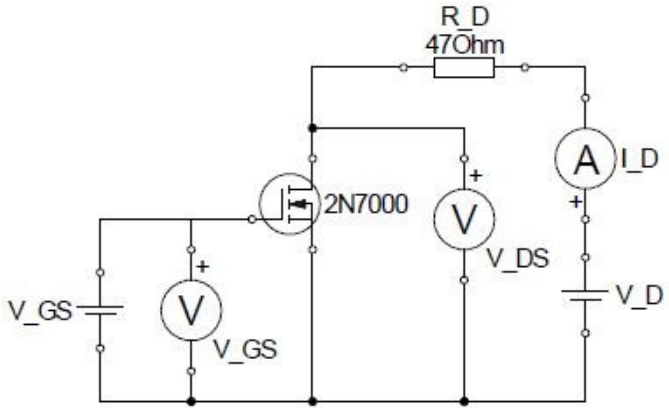


Figure 16: The figure shows the implemented circuit to measure the transfer characteristics, the following circuit was used.

Table 5: The table shows the gate source scanned from 0 to 3 V,while the drain source is constant at 5 V.

V_{GS}	I_D/mA
0	0
1	0
2	0.497
2.1	1.56
2.2	39.9
2.3	41.6
2.4	44.2
2.5	47.5
2.6	49.7
2.7	51.7
2.8	54.5
2.9	56.4
3	58.5

Table 6: The table shows $V_{GS} = 2.2V$

V_{DS}	I_D/mA
0	0
0.093	1.5
0.154	1.73
0.206	1.83
0.411	1.95
0.501	1.97
1	2.03
1.51	2.07
2.022	2.37
2.507	2.58
3.009	2.49
3.506	2.41
3.989	2.5

Table 7: The table shows $V_{GS} = 2.4V$

V_{DS}	I_D/mA
0.1	5.86
0.4	6.49
1	9.6
1.5	13.39
2	17.23
2.5	21.7
3	25.2
3.5	28.7
4	32.15

Table 8: The table shows $V_{GS} = 2.6V$

V_{DS}/V	I_D/mA
0	0
0.2	20.3
0.6	13.6
1.1	14.3
1.5	17.79
2	21.15
2.5	25.22
3	29.1
3.5	32.39
4	36.06

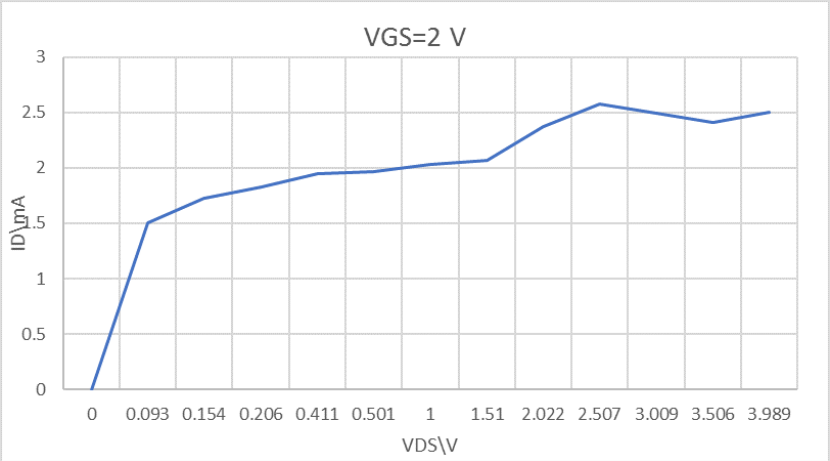


Figure 17: The graph shows the transfer characteristics.

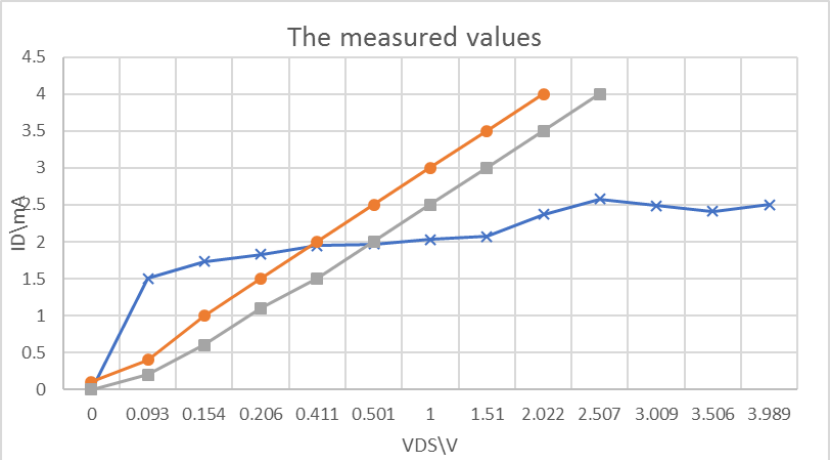


Figure 18: The graph shows the transfer characteristics when $V_{GS} = 2.2V$ which has the marker$\times$,$V_{GS} = 2.4V$ which has the marker$\cdot$ and$V_{GS} = 2.6V$ which has the marker$\boxdot$

Table 9: The table shows the values from the data sheet for the $V_{DS} = V_{GS} - V_{th}$.

V_{DS}/V	I_D/mA
0.038	0.16
0.163	1.23
1.3164	10.43
0.5684	22.9

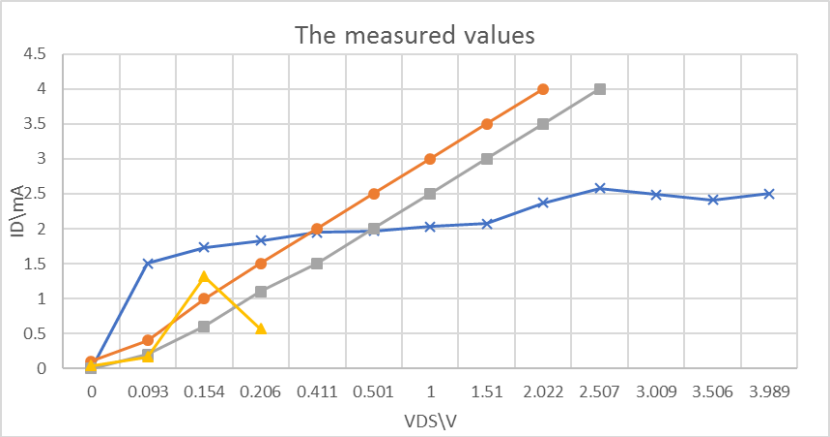
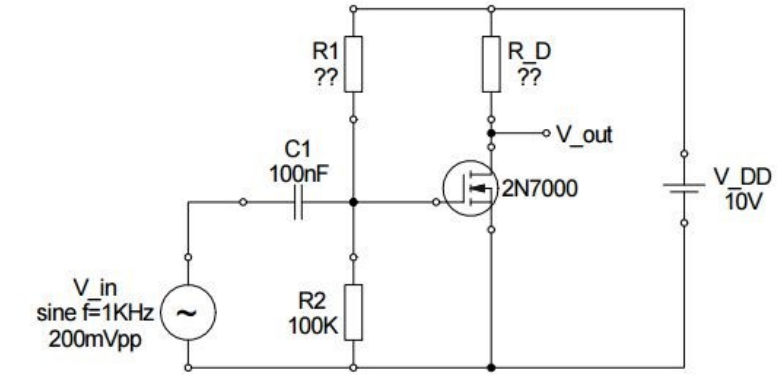


Figure 19: The graph shows the addition of the $V_{DS} = V_{GS} - V_{th}$ line denoted as ▲

Problem 2:MOSFET as Amplifier



$V_{GS} = 2.7V$, $V_{DS} = 5V$, $k = 72.2mA/V^2$, U_{th} = use measured value!

Figure 20: The figure shows the implemented circuit.

From the circuit we know that:

$$R_D = \frac{V_{DD} - V_{DS}}{I_D} \tag{8}$$

$V_{DD} = 10V$
$V_{DS} = 5V$
$I_{DS} = k(V_{GS} - V_{th})^2$
$k = 72.2mA/V$
$V_{GS} = 2.7V$
$V_{th} = 2V$
$\therefore R_D = 141.3\Omega$

$$V_{R_2} = \frac{V_{DD} \times R_2}{R_1 + R_2} \tag{9}$$

From the circuit we see that $V_{GS} = V_{R_2}$:

$$V_{GS} = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

$\therefore R_1 = 270.4\Omega$

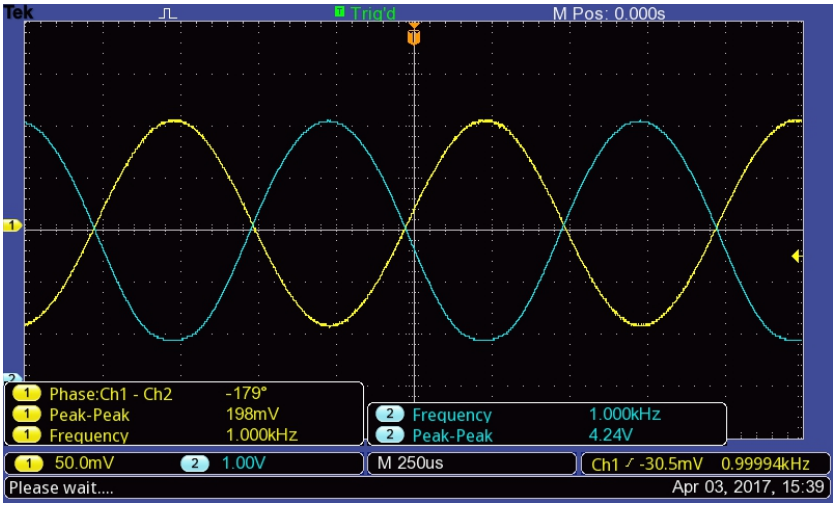


Figure 21: A graph shows the results of the experiment.

Question 1

The transistor operates in the saturation mode during amplification because it satisfies the requirements in the saturation mode with are : $V_{GS} \geqslant V_{th}$ **and** $V_{DS} \geqslant V_{GS} - V_{th}$**.The first equation is** $2.7 > 2$ **and the second is** $5 > 0.7$**.**

Question 2

$$V_{GS(inst)} = 2.7V + V_{in}$$

From the circuit we see that $V_{out} = V_{DS}$ **so using the previous equation.** $V_{DD} = I_D \times R_D + V_{out}$

In determine the largest possible input for no clipping to observed.$V_{out} = V_{in} - U_{th} \quad V_{DD} = I_D R_D + V_{in} - U_{th}$

We know that $I_D = k(V_{GS(inst)} - U_{th})^2$

By equating the equations we get:

$$V_{DD} = R_D(k(2.7V + V_{in} - U_{th})^2) + V_{in} - U_{th}$$

$\therefore V_{in} = 243.2mV$

Question 3

The theoretical voltage gain is $VDS = \frac{Vout}{Vin}$. $V_{GS(max)} = V_{GS(inst)}$ $V_{in} = V_{GS(AC)}$

Let $V_{GS(AC)} = V_{GS(ACmax)}$**.** $V_{GS(ACmax)} = -V_{GS(ACmin)}$

$$VGS(max) = V_{GS} + V_{GS(AC)}$$

$$VGS(min) = V_{GS} - V_{GS(AC)}$$

$$I_{D(max)} = k(V_{GS} + V_{GS(ACmax)} - U_{th})^2$$

$$I_{D(min)} = k(V_{GS} + V_{GS(ACmax)} - U_{th})^2$$

$V_{outmin} = V_{DD} - I_{Dmax}R_D$ **in order to obtain a small** V_{outmin} V_D **should be large due to the minus sign.The opposite applies for** V_{outmax}

$$V_{outmin} = VDD - k(V_{GS} + V_{GS(AC)} - Uth)^2RD$$

$$V_{outmax} = VDD - k(V_{GS} - V_{GS(AC)} - Uth)^2RD$$

$$V_{out} = V_{outmax} - V_{outmin}$$

$$\therefore Gain = \frac{VDD - k(V_{GS} - V_{GS(AC)} - Uth)^2R_D - V_{DD} - k(V_{GS} + V_{GS(AC)} - U_{th})^2R_D}{V_{in}}$$

Question 4

Table 10: The table compares the theoretical gain and the real gain we can see that there is a large deviation in the two results.

	Theoretical	Real
Gain	28571.47	21.41

Question 5

From the hard copy we see that the phase difference is $-179°$**.This could be due to the influence of the capacitor.**

Problem 3:Design a Multiplexer

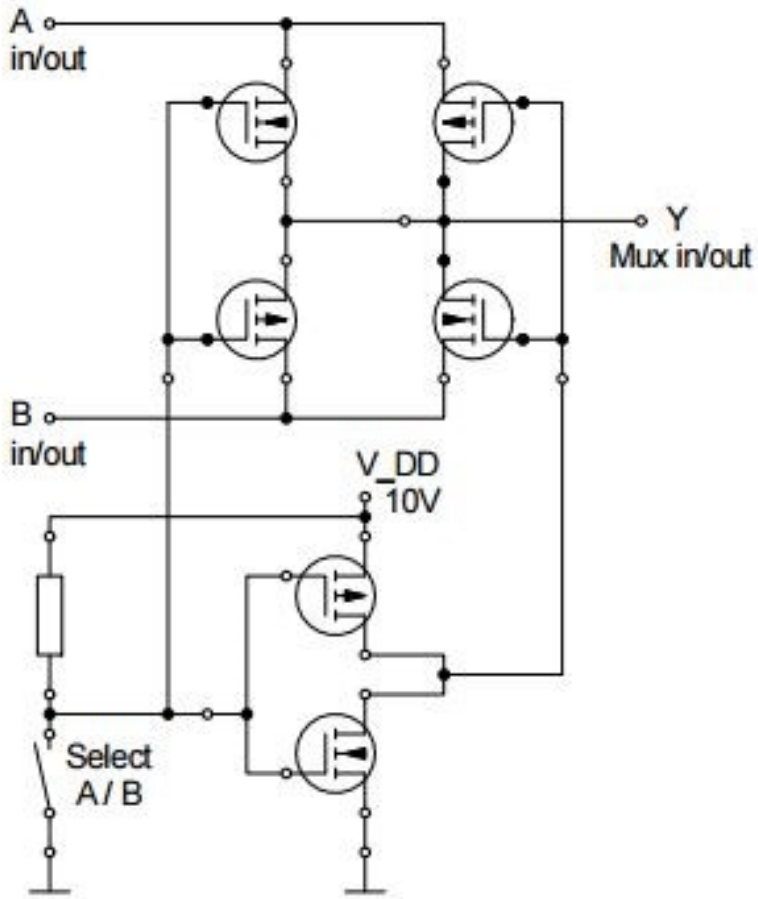


Figure 22: The figure shows the implemented circuit.

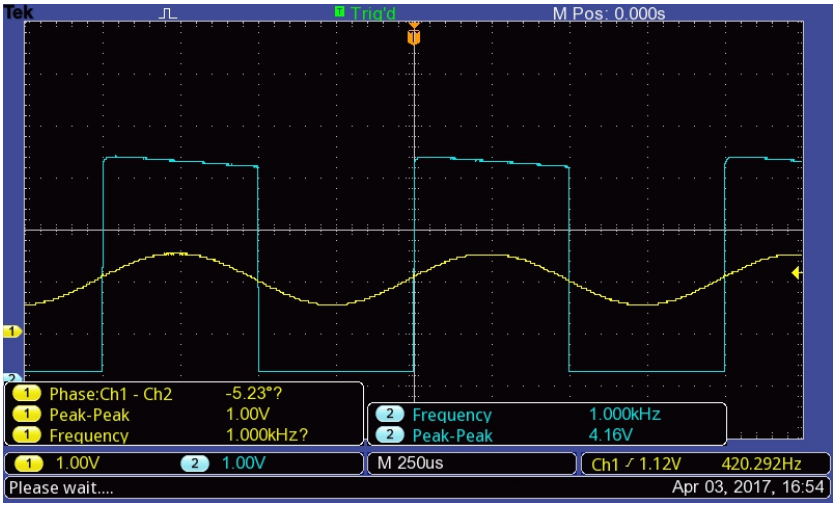


Figure 23: A graph shows the results of the experiment.The rectangular pulse occurs when there is a A/B low and the other when there is a A/B high

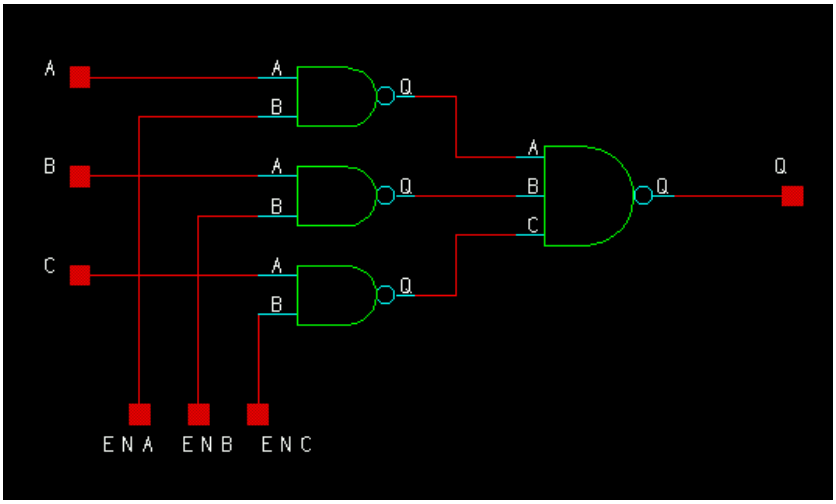


Figure 24: The figure shows a 3-1 multiplexer

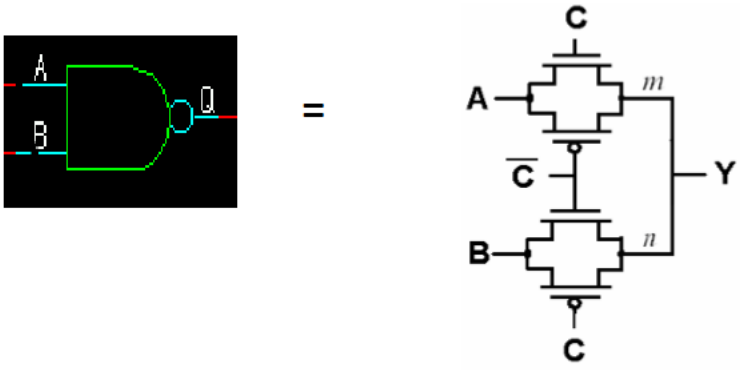


Figure 25: The diagram equates the components.Where all Cs represents the ground on the circuit on the right.

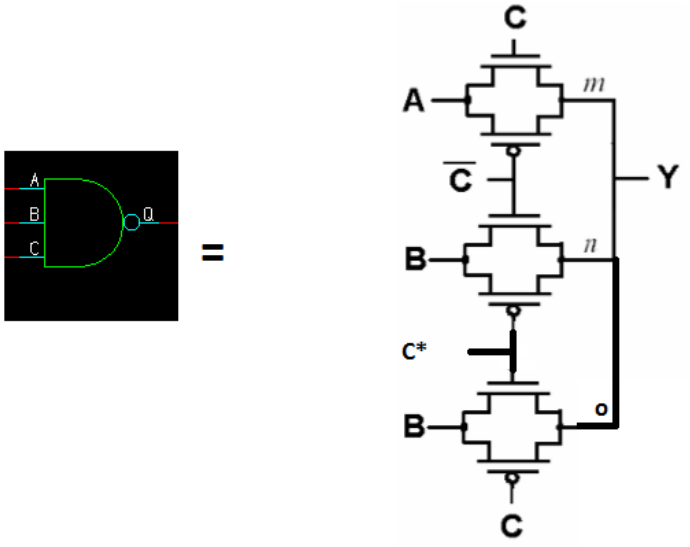


Figure 26: The diagram equate the components.Where all Cs represents the ground on the circuit on the right.

Conclusion

In this experiment we see that there are some large deviation from the real value and the theoretical values.In this experiment we saw how to design a Multiplexer.In this experiment we did not obtain any significant errors.One of the errors where in Problem 1 since the transistor was heating up.

References

Adv.EE Lab-Electronics Lab Manual
http://www.edaboard.com/thread209324.html
https://en.wikipedia.org/wiki/Exclusive_or