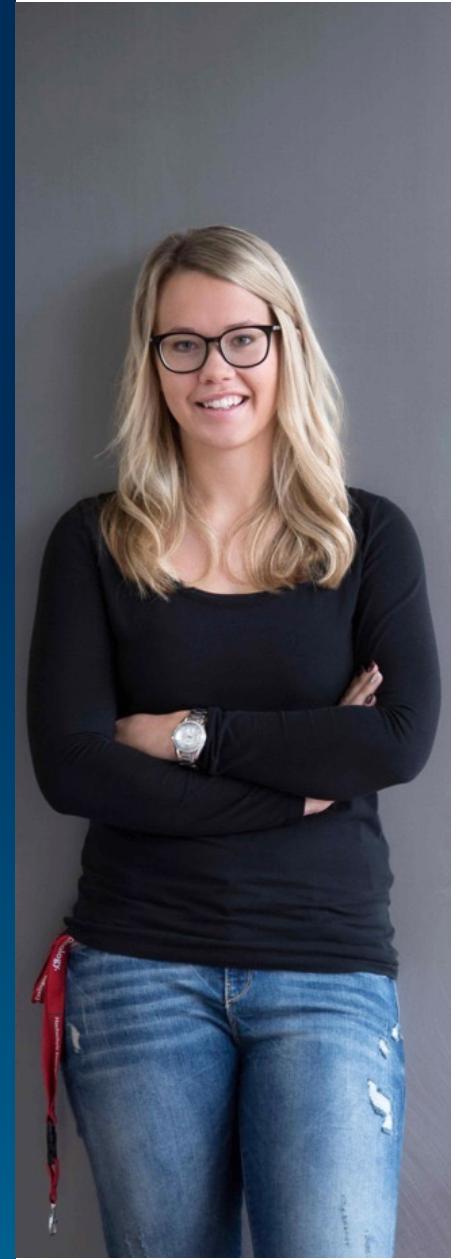


LECTURE COMPUTER ARCHITECTURE  
**INTRODUCTION**

RAINER KELLER





## CONTENT

- 1 Moore's law and ICs
- 2 IT market – and Embedded Market
- 3 Programming embedded systems
- 4 Bus and CPU architectures
- 5 Instruction execution

## REMINDER: INTERNATIONAL SYSTEM OF UNITS (SI)

Reminding of mind-boggling numbers & scales:

- pico =  $10^{-12}$  Current CMOS structures: 3nm (Gate length)  
DNA's diameter: 2,5nm (Hair: 50.000nm!)
- nano =  $10^{-9}$  IB-Networks achieve latency of  $<1\mu\text{s}$ !
- micro =  $10^{-6}$  The human eye blink takes  $\sim 300$  ms.
- milli =  $10^{-3}$  The physical moving of a hard-disk's head takes on the order of 8ms!
- Kilo =  $10^3$  Microprocessors operate at 3 GHz
- Mega =  $10^6$  clock cycle frequency.  
In turn, one cycle only takes  $\sim 0,3 \cdot 10^{-9}$ s
- Giga =  $10^9$  During that time light travels only 10cm!
- Tera =  $10^{12}$  Hard-disks now feature 22 TB of storage  
Put thousands together one gets PB
- Peta =  $10^{15}$  storage (problem: finding, retrieving)

## GOALS FOR TODAY

- Understand the aim of lecture Computer Architecture
- Developments in IC/CPU design
- Know the market of Embedded Systems
- Understand basic CPU architectures and designs

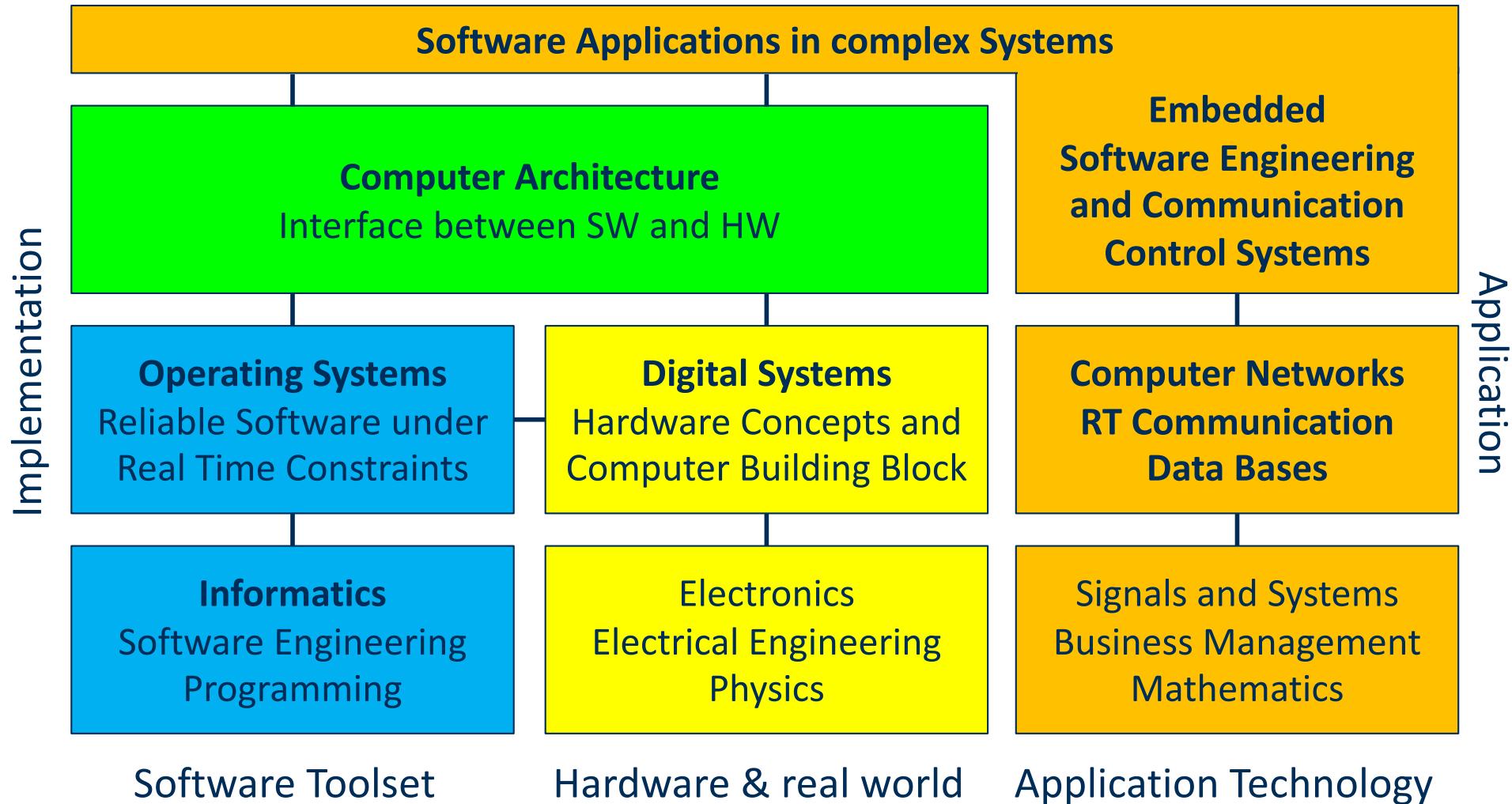
# COMPUTER ARCHITECTURE

Computers come in all shapes and sizes...



Some even make headlines:

Where we are located in our Curriculum:



Please re-evaluate the corresponding lecture's scripts (like Digitaltechnik)

# Moore's Law, Intel and other CPUs

# IC TECHNOLOGY DRIVER

## Over time: many advancements in the Manufacturing technologies

### Major Process Technology Innovations Are Piling Up



Source: IC Insights

Computer Architecture, Profs R. Keller, J. Friedrich, W. Zimmermann

Publication regarding SiGe and III-V Channels:  
**"SiGe and Ge Epitaxy: Channels to a Higher Mobility"**

High-k Material with better insulation than SiO<sub>2</sub>

Other Materials than Silicon: Germanium

And Copper with lower resistance for wires/vias

This we will revisit later

Manufacturers had / have to adapt with a lot of new technology in the last few years.  
New Fabs cost Billions of USD.

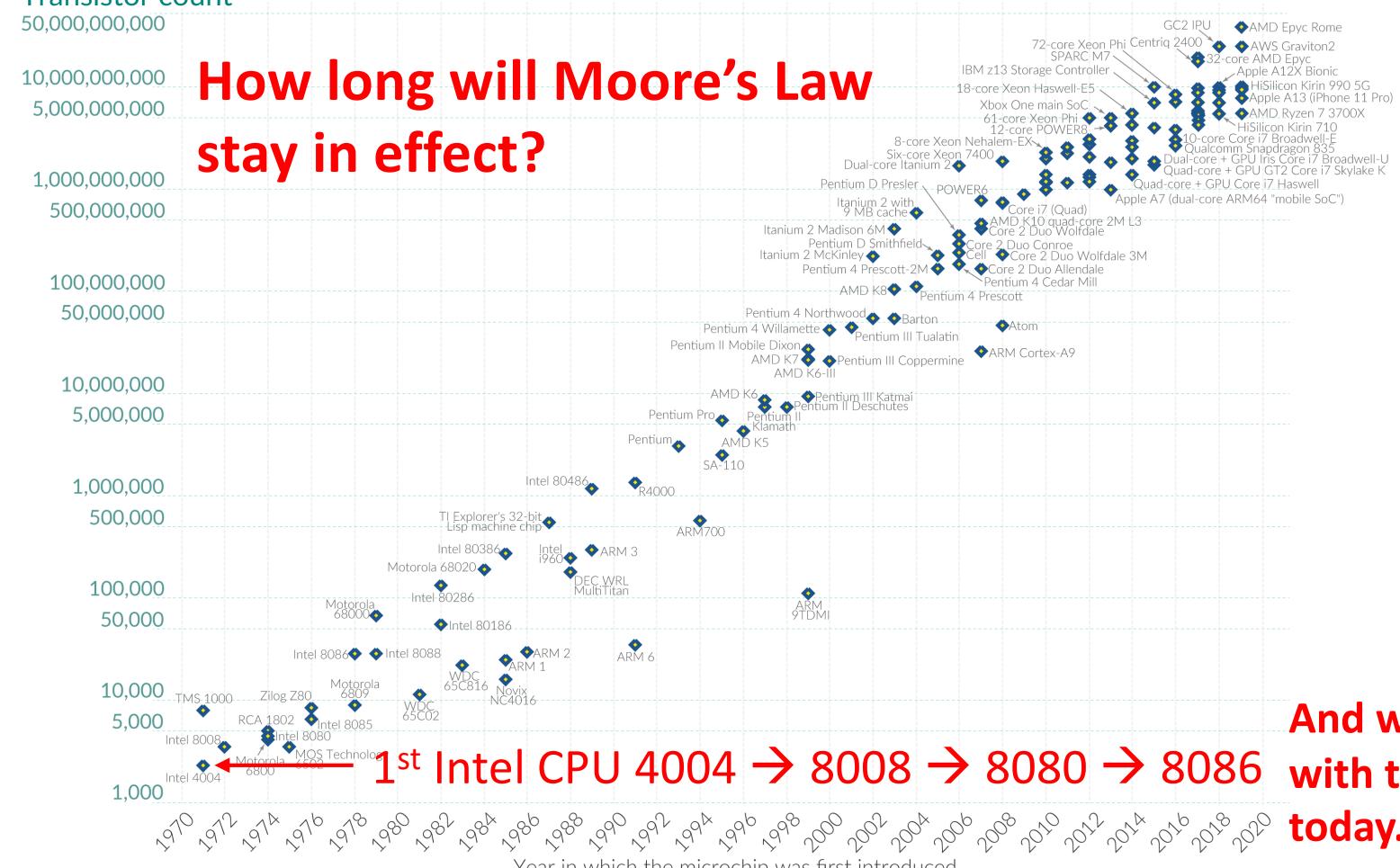
# HISTORY: MOORE'S LAW 1/2

Moore's Law: "Number of transistors per chip-area doubles every 12 (to 18) months". In effect since 1965...

Moore's Law: The number of transistors on microchips doubles every two years

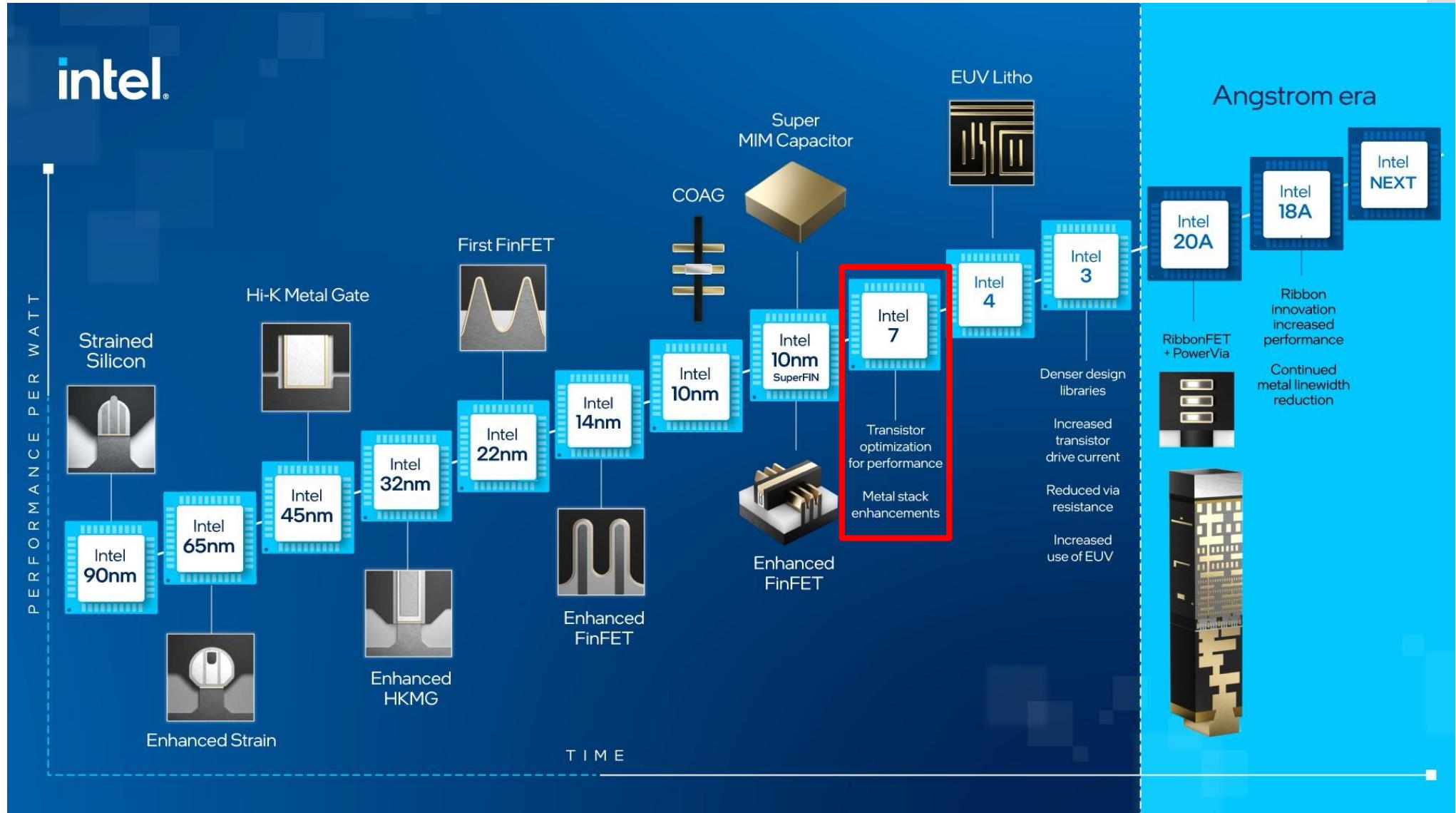
Our World  
in Data

Transistor count



## HISTORY: MOORE'S LAW 2/2

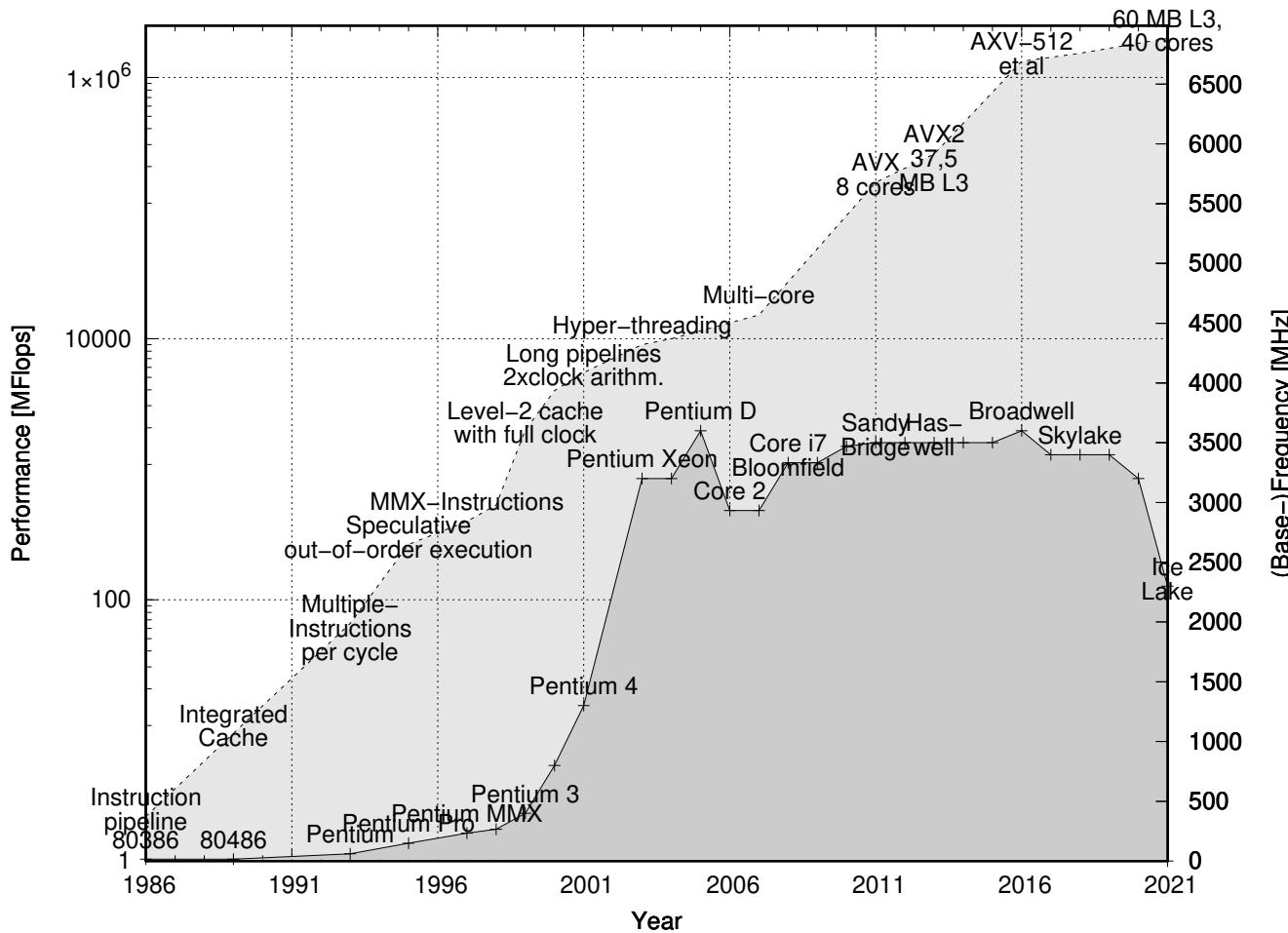
Nice overview from Dr. Ann Kelleher (Exec.-VP Techn. Devel.), Intel (2022):



[Link to interview with Dr. Ann Kelleher \(Dec. 2023\) on opening Fab 34 in Ireland](#)

# DEVELOPMENT OF (MICRO) PROCESSORS

When we talk about development of “processors”, we often mean “micro processors”, i.e. Intel x86-64, mainly for Desktops, Laptops and Server. Their development was/is *extraordinary*:



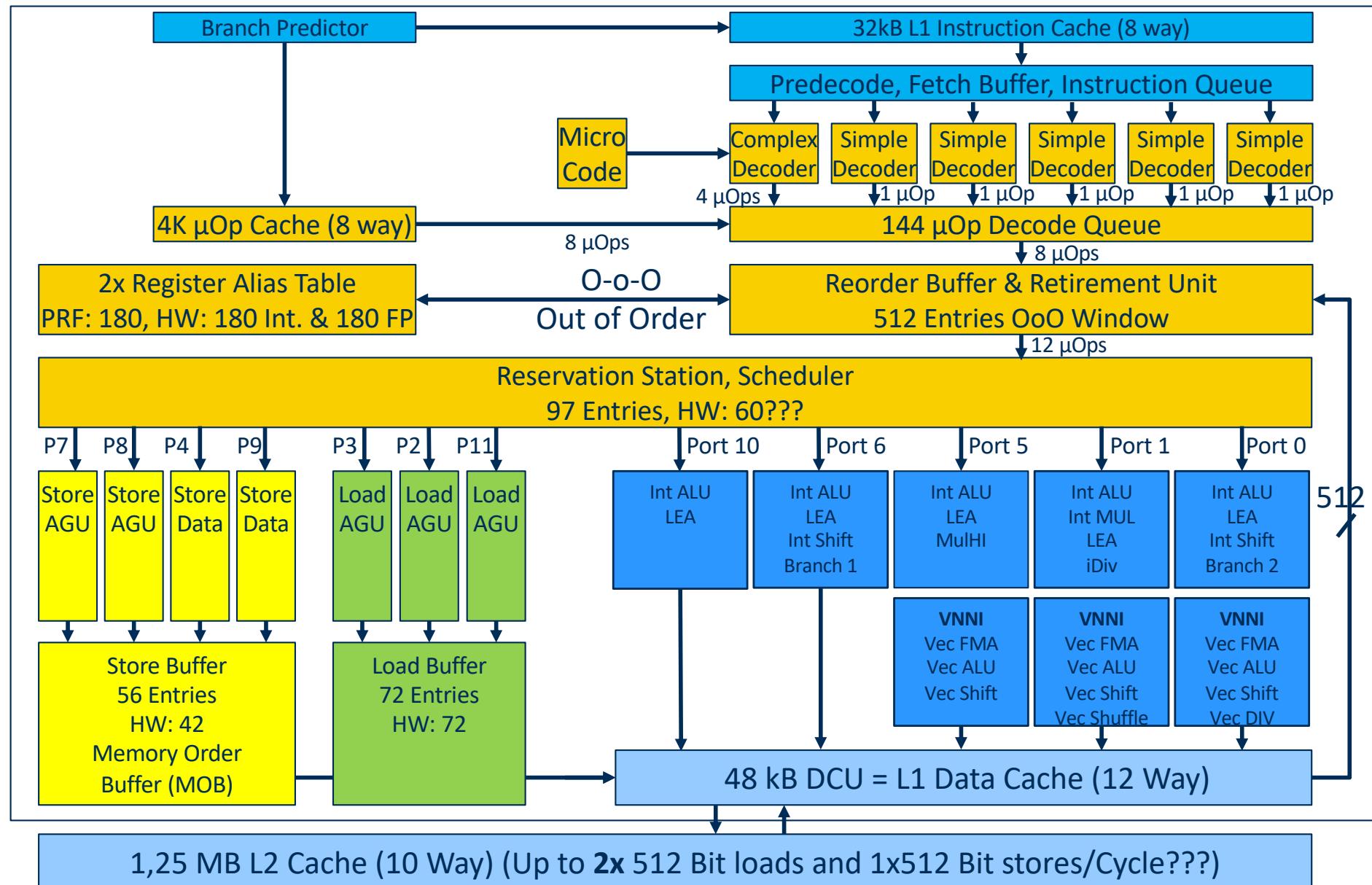
Source: Myself

What stands out?

- Exponential growth of performance (here MFLOPs)
- Core frequency does not grow... (again, this is **base-frequency**)
- Performance is achieved mainly through many cores (& caches)!
- While “in the old days”, one just had to wait one year to get twice the performance, now one really **must work** (optimize, reprogram)!  
*H. Sutter: „The free lunch is over!“*

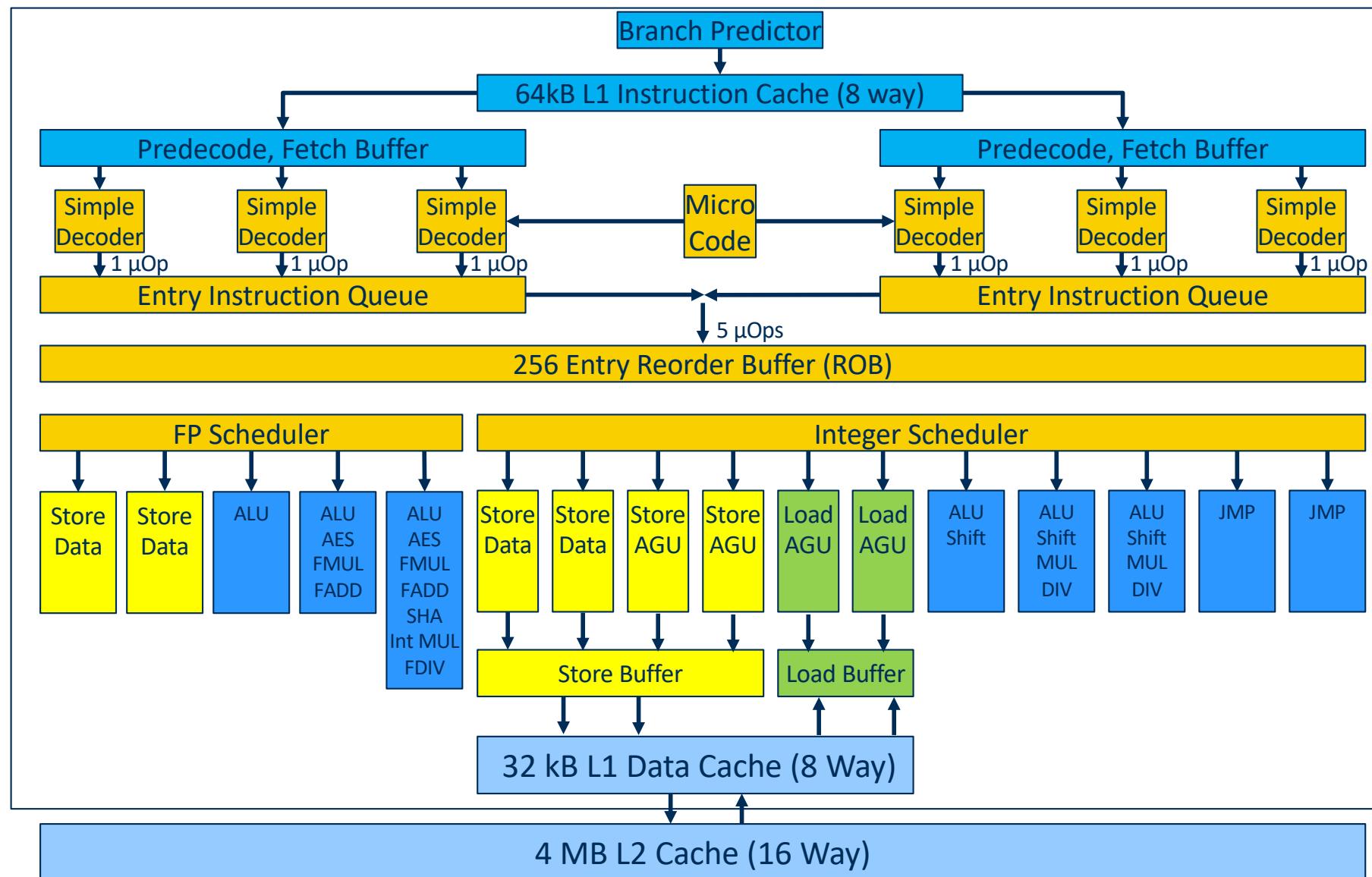
# INTEL ALDER LAKE & RAPTOR LAKE MICROARCH. (2023)

P-Cores: Golden Cove are an extension of the Willow Cove architecture (~19% faster):



# INTEL ALDER LAKE & RAPTOR LAKE MICROARCH. (2023)

E-Cores: Gracemont are meant to be power-efficient (and **small** in size!)



## OTHER (MICRO) PROCESSORS

When we talk about development of “processors”, we often mean “micro processors”, i.e. Intel x86-64, mainly for Desktops, Laptops and Server.

Which other processors/manufacturers do You know?

IBM Mainframe zSeries



IBM Power processors (Servers & Printers)



ARM **Arm** (now NVIDIA) is in virtually every mobile phone!

NEC SX **Vector** processors:



- 1 instruction processes up to 256 operands
- Impressive architecture of SX-9:  
16 CPUs on one main board, each  
feature 256 GB/s memory bandwidth!



MIPS Architecture used in DSL Routers



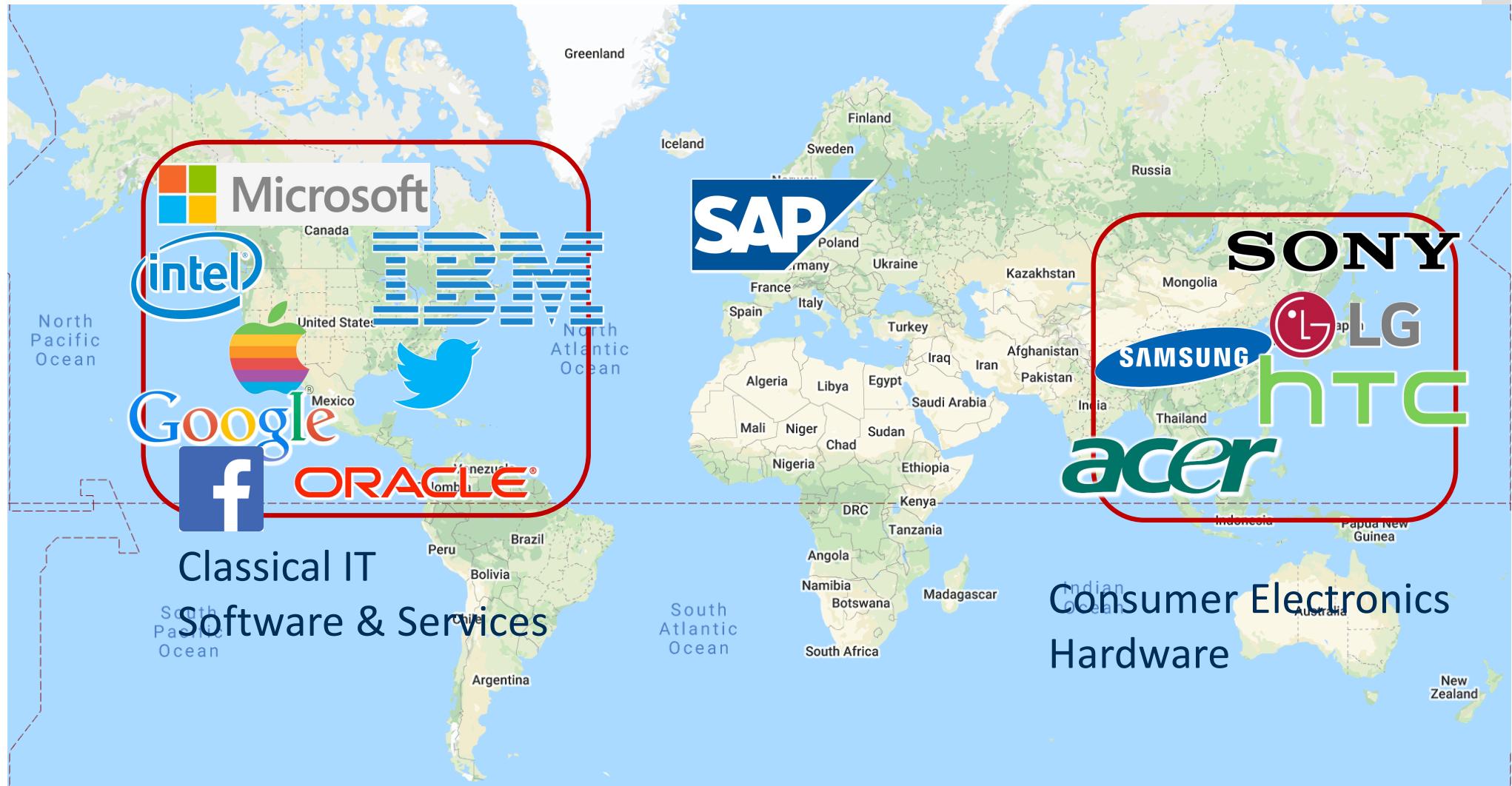
SPARC Architecture (Oracle & Fujitsu)

RISC-V Architecture: **the Alternative™** ...



# IT World Champions

# IT WORLD CHAMPIONS...



Something missing here???

# EMBEDDED IT CHAMPIONS!



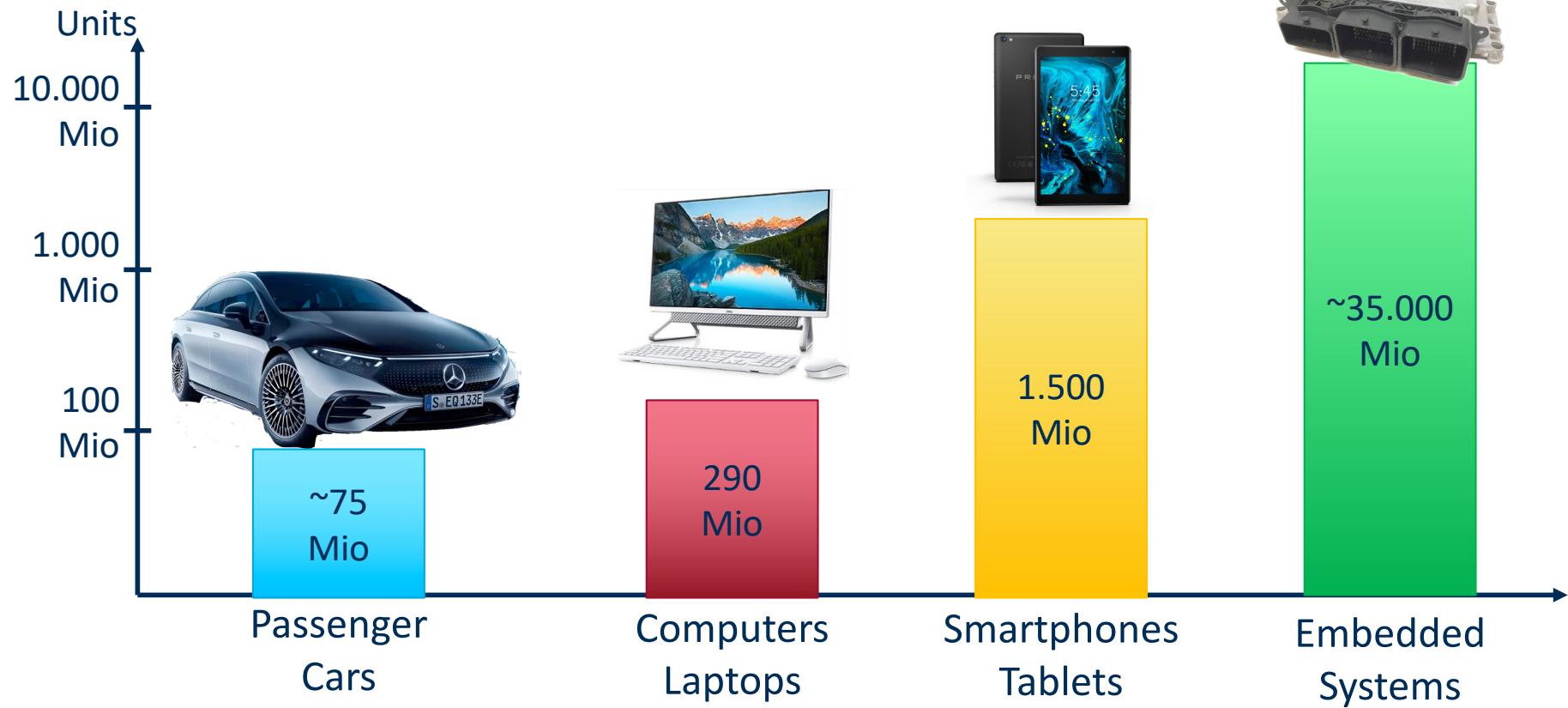
The currently only producer of EUV lithography machines is ASML.

## PROCESSOR MARKETS

Number-wise, what are the most sold processors worldwide?

Intel x86-64?  
IBM Power?  
ARM Cortex?  
AMD Ryzen?

None of the above! Let's compare world-wide units/year:



Source: all data for 2023, Statista, IC insights

MORE TO COME...

Internet of Things (IoT):  
interconnected, -acting computers everywhere, with multiple sensors

Wearables  
“pervasive computing”



Smart Home (think smart building/fab)



Automated Driving, Mobility

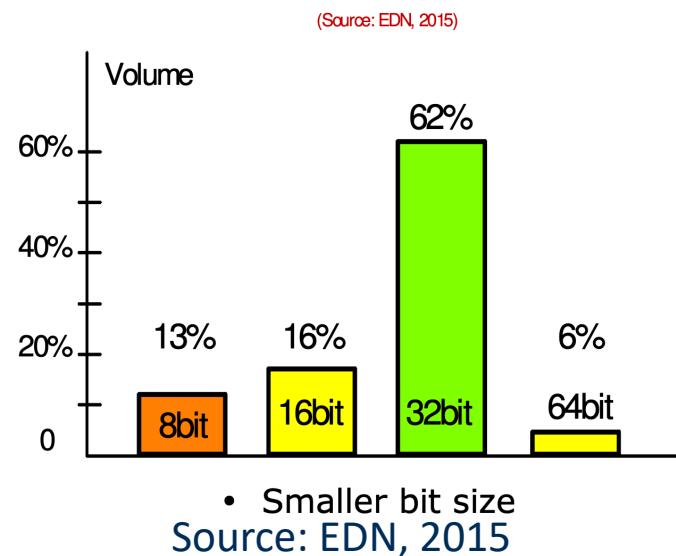


# EMBEDDED SYSTEMS

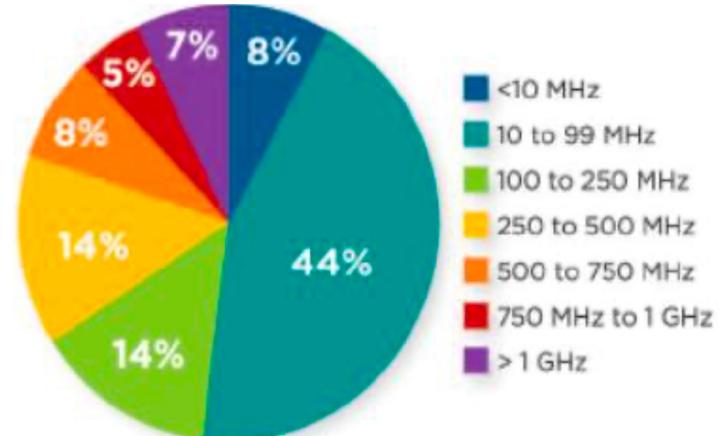
What is special in Embedded Systems?

- **Reliability and Safety!!!** → Buggy System may kill people
- **Real Time requirements** → Must run in sync with external events
- **Resource Constraints** → Computing speed & memory size limited

Embedded CPUs market share:



CPU clock speed:



Your washing machine don't need 64 bit...

# EMBEDDED SYSTEMS MARKET

Market expected to grow from \$207.3 Billion in 2020 to \$267.3 in 2025!  
 IC / Hardware companies:

Company	Note	Revenue/Bio.	Employee	HQ
Intel	Known for x86-64 bought Mobileye	<b>~8% of \$77.87</b>	110600	St. Clara, CA
Altera (bought by Intel 2015)	FPGAs	<b>Price: \$16bio</b>		San Jose, CA
Xilinx (bought by AMD 2020)	Invented FPGAs	<b>Price: \$35bio</b>		San Jose, CA
Qualcomm	4G, 5G, SoC (e.g. Snapdragon)	\$25.53	41000	San Diego, CA
<b>NXP</b>	Spin-off by Philips	\$8.61	29000	<b>Eindhoven</b>
Freescale (merged into NXP)	Out of Motorola 2004	<b>Price: \$43bio</b>		Austin, TX
<b>STMicroelectronics</b>	Merger: Italian&French companies	\$10.22	46000	<b>Geneva</b>
<b>Bosch</b>	IoT since 2011, Chip plant in 2021	...	...	<b>Gerlingen</b>
Analog Devices	DSPs, Power Management	\$5.79	15300	Wilmington
Infineon	Spin-off by Siemens	\$8.57	46000	<b>Dresden</b>
<b>Microchip Technologies</b>	Spin-off by General Instruments	\$5.70	14000	Chandler, AZ
Atmel (bought by Micro... 2014)	AVR, improved Intel 8051, ARM	<b>Price: \$3,6bio</b>	5200	San Jose, CA

# Programming

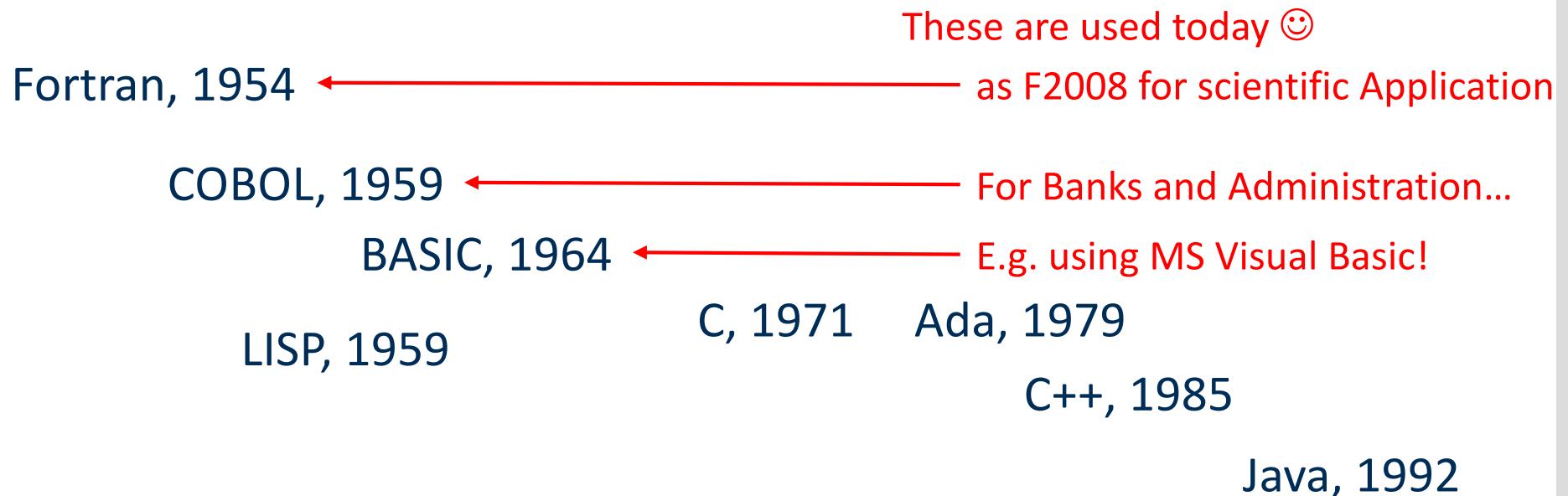
# PROGRAMMING LANGUAGES

Computer programming languages allow humans to communicate the machine, what exactly to do!

Before, one had to do that in “machine language”:

- First and foremost: plug cables (see ENIAC)
- Then via coding of the hexadecimal instructions
- Finally Assembler with human-readable mnemonics

Only then the High-level languages were developed:



Observation of general usage of programming languages:

Language	Typical Usage	TIOBE	IEEE
Python	Prototyping, Numerical Analysis, AI, Testing	15.6%	1
C	General Purpose, Kernels	11.2%	4
C++	General Purpose, Object Oriented	10.7%	3
Java	Business Applications, Portable SW	8.9%	2
C#	General Purpose, <b>not</b> portable	7.5%	6
JavaScript	Web Clients and servers	3.4%	5
SQL	Database query and definition language	1.9%	7
Go	General Purpose, Automated Scripts,	1.6%	8
Scratch	Basic language to learn programming	1.5%	??
Assembly	Low-level, hardware optimized kernels	1.4%	22

Sources (as of March 2024): First time, Python overtook C!

<https://www.tiobe.com/tiobe-index/>

<https://spectrum.ieee.org/top-programming-languages-2021>

Other popular languages: Ruby (Old), PHP, **Rust**, Swift, R, Shell...

# HARDWARE & SOFTWARE STACK

Any computer, large or small

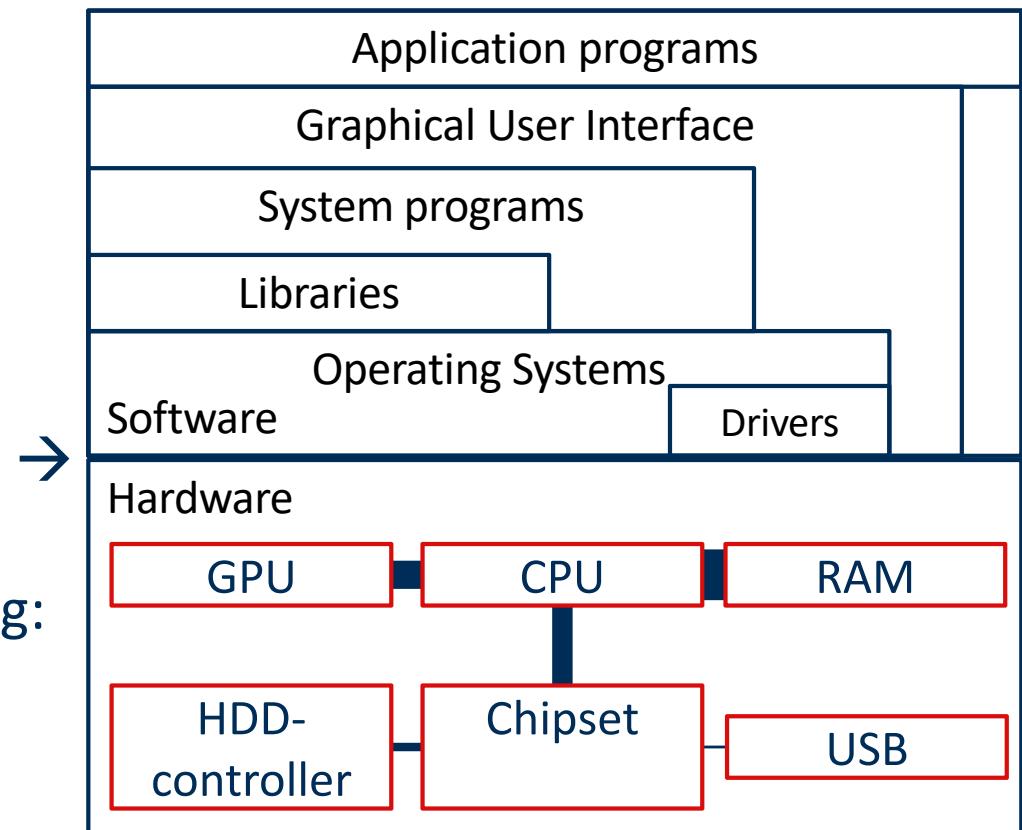


basically have the same  
Hardware setup & Software stack

Sometimes, there is a "Hardware Abstraction Layer" (HAL)

Architectural differences regarding:

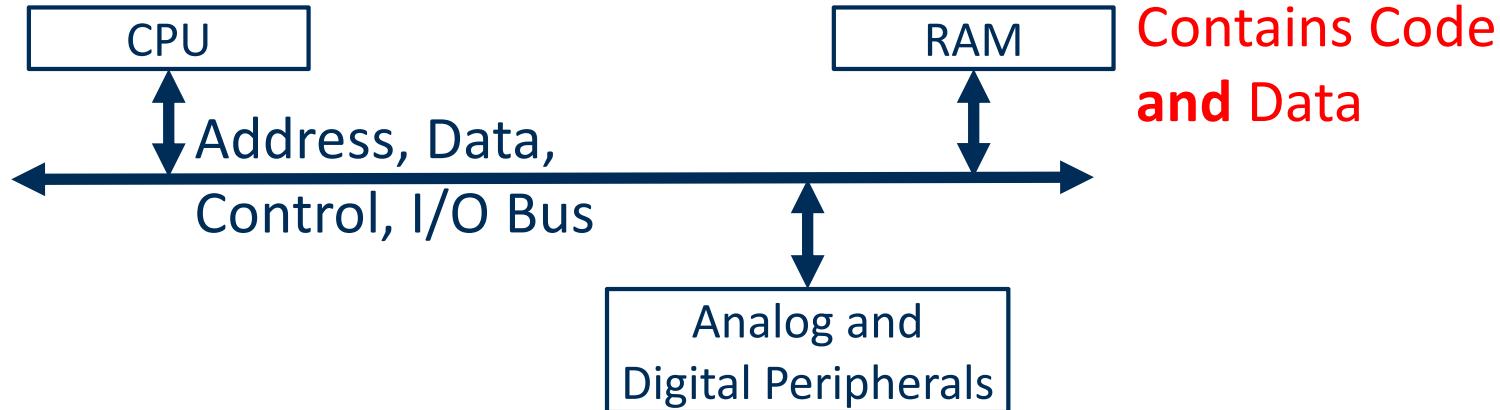
- UI? GUI? Even a GPU?
- What kind of I/O? Sensors?
- CPU → RAM



# Bus Architectures

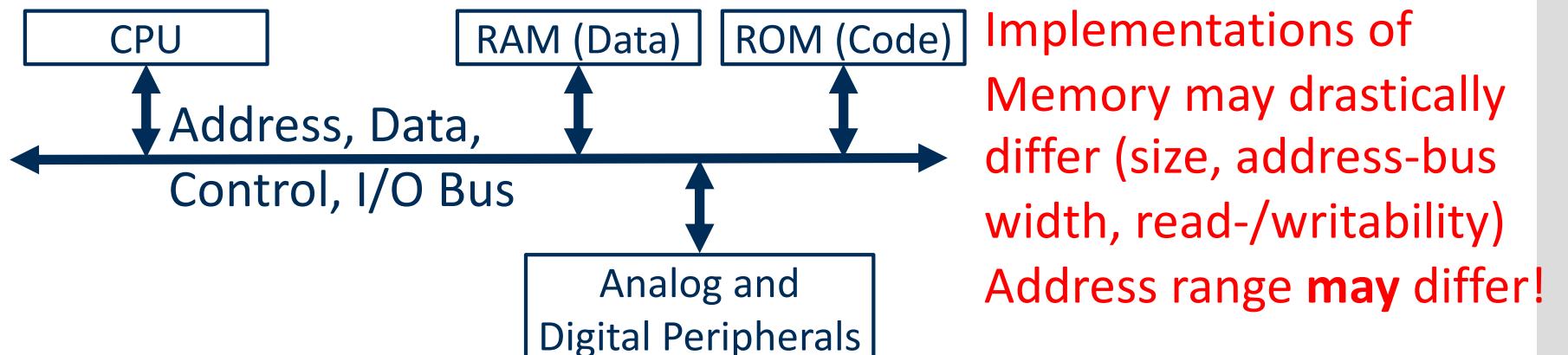
# HARDWARE SETUP WITH REGARD TO RAM

Von-Neumann Architecture:



Contains Code and Data

Harvard Architecture:



Implementations of Memory may drastically differ (size, address-bus width, read-/writability)  
Address range **may** differ!

What are up-/downsides of the Harvard Architecture?

What does the programmer have to take into account?

Which one is more common?

# BUS ARCHITECTURES

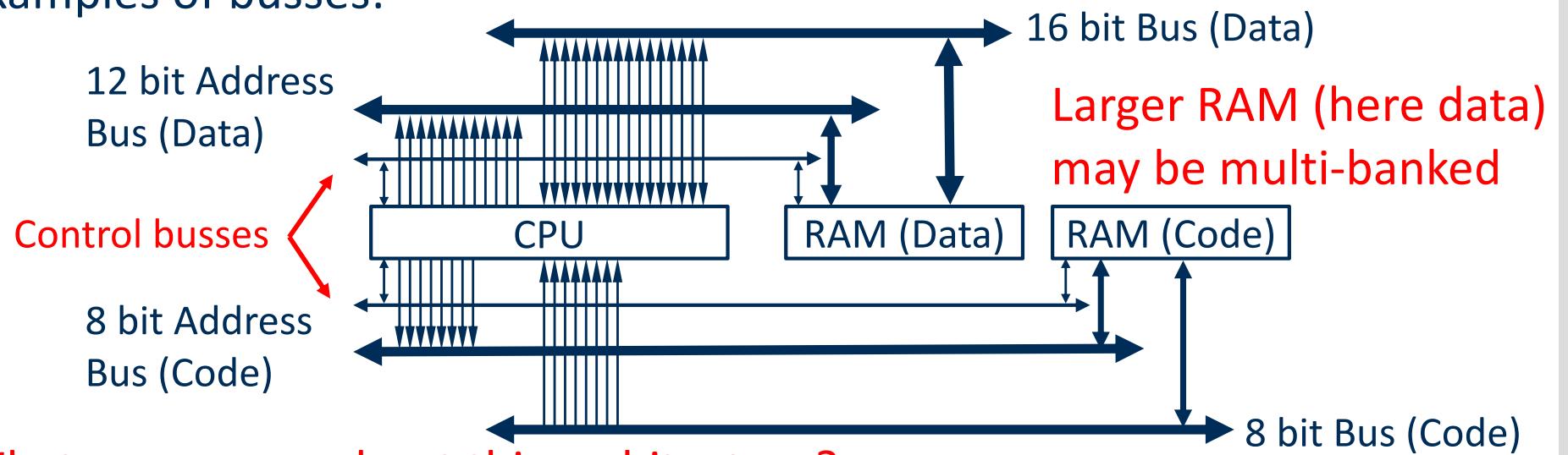
The definition of a computer bus:

A computer bus is a communication system that transfers data between components inside or between computers.

Busses may be:

- Serial (1-wire) or parallel; for control/power, more wires are required
- Uni- or bidirectional,
- Single-point or allowing multiple access points.

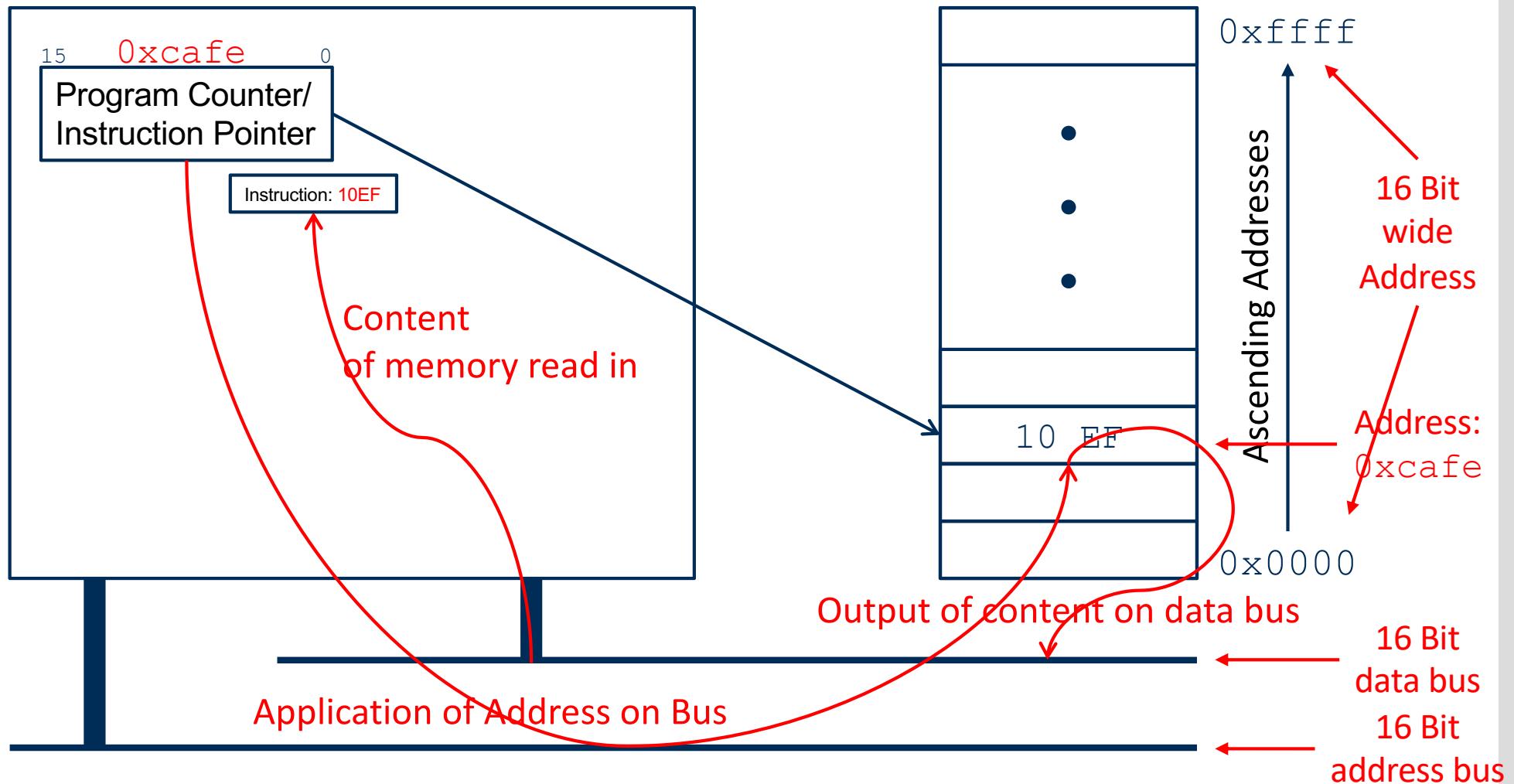
Examples of busses:



What can we say about this architecture?  
How wide are the control busses?

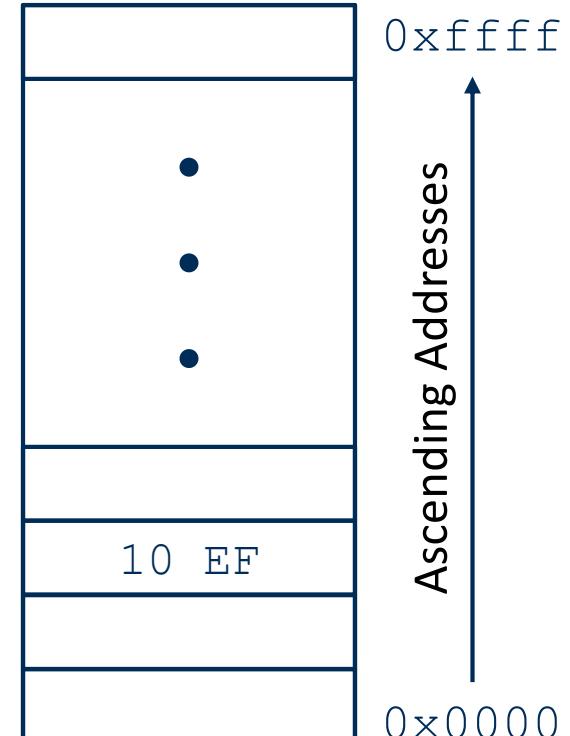
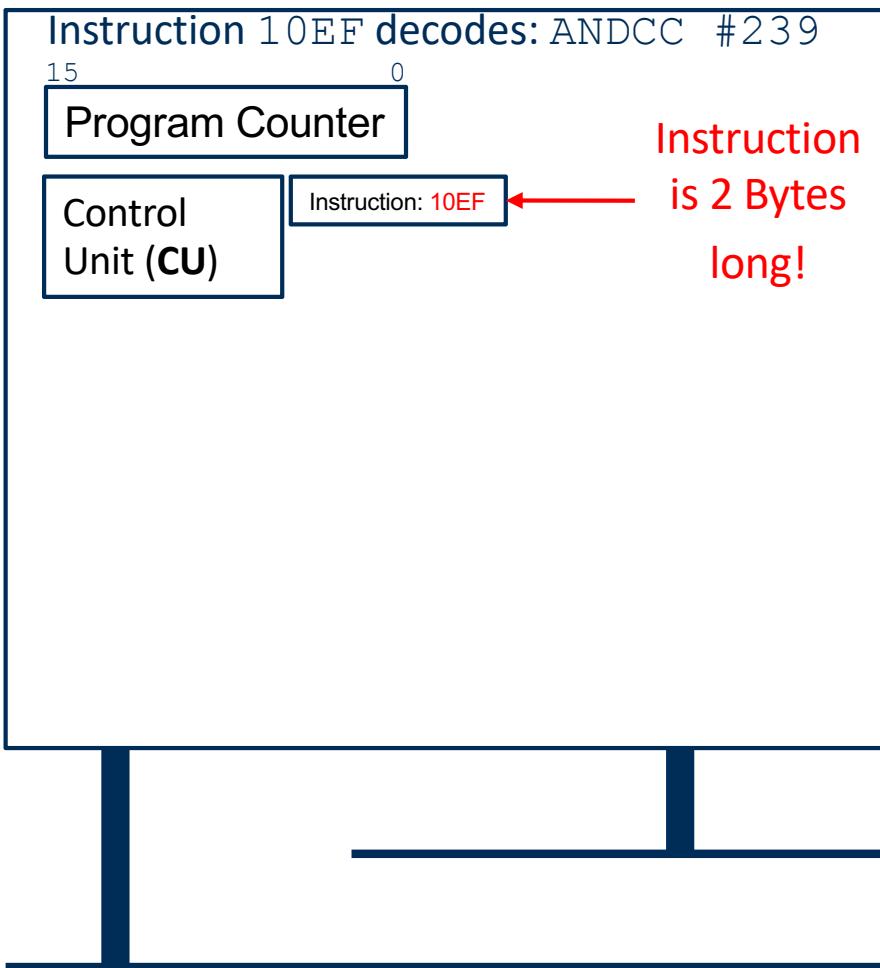
# REPETITION MICROPROCESSORS 1/6

Simple CPU execution in phases: Phase 1 Instruction Fetch



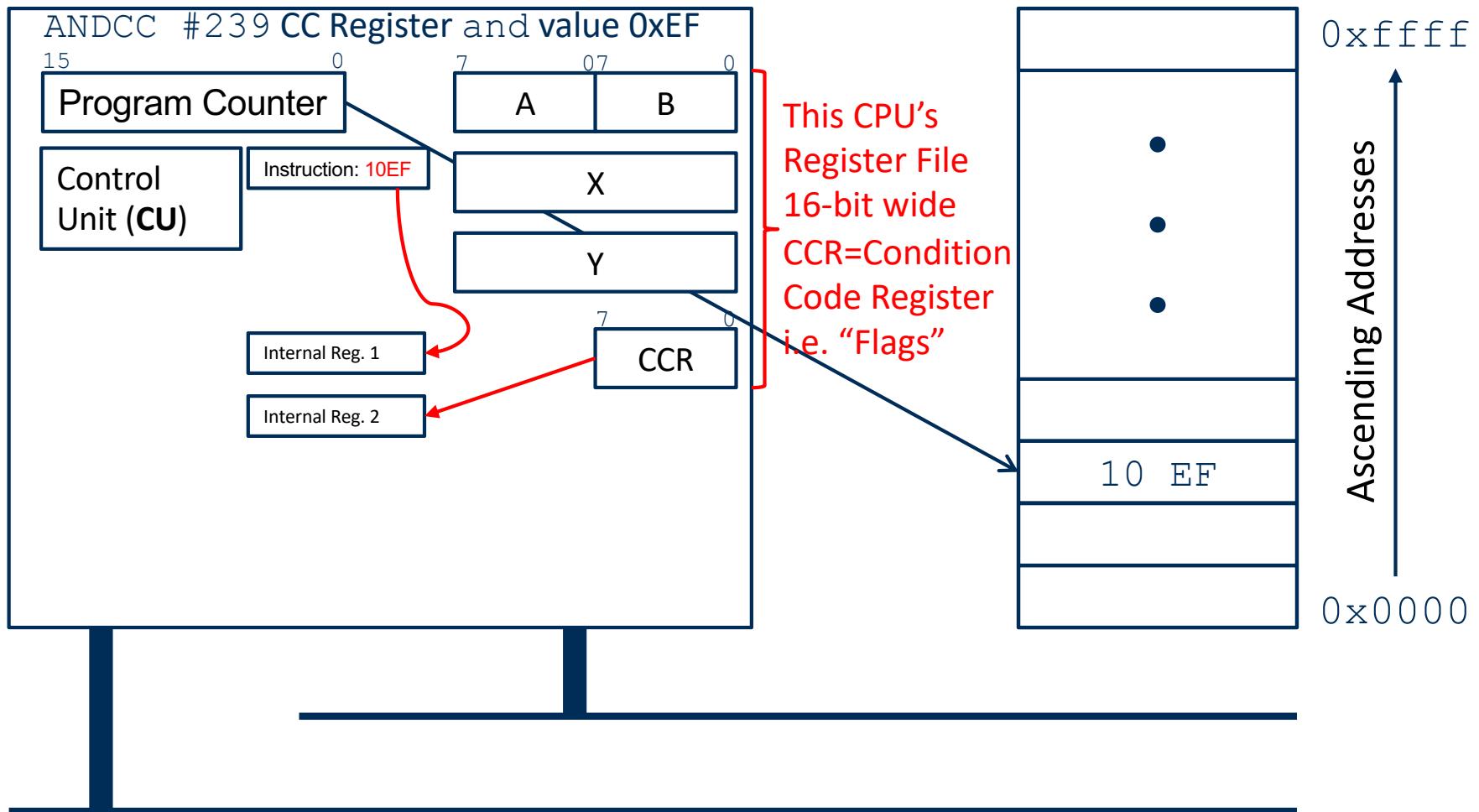
# REPETITION MICROPROCESSORS 2/6

## CPU Phase 2: Instruction Decode



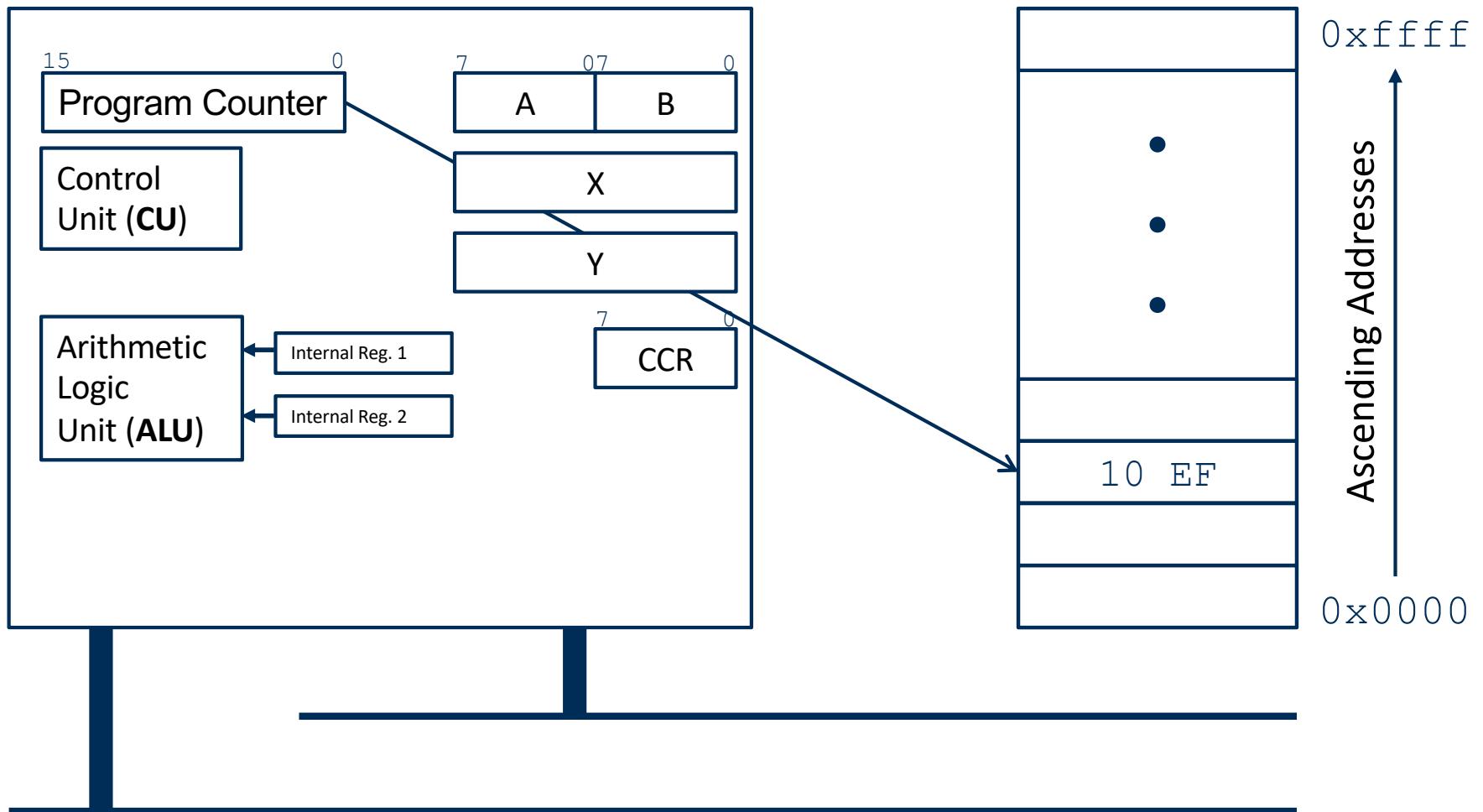
# REPETITION MICROPROCESSORS 3/6

## CPU Phase 3: Fetch Operands



# REPETITION MICROPROCESSORS 4/6

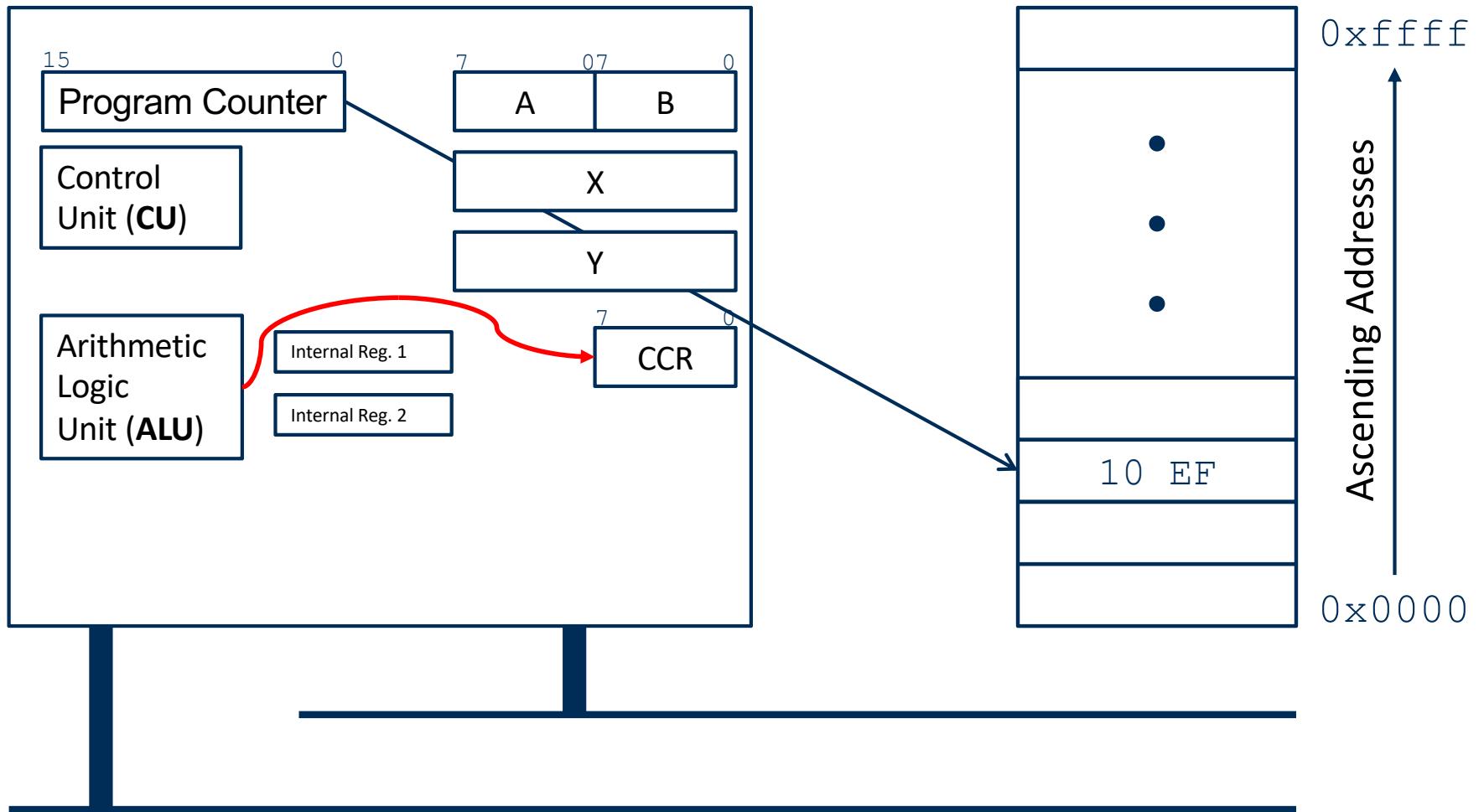
## CPU Phase 4: Instruction Execute



ALU computes the result of the instruction ANDCC #239

# REPETITION MICROPROCESSORS 5/6

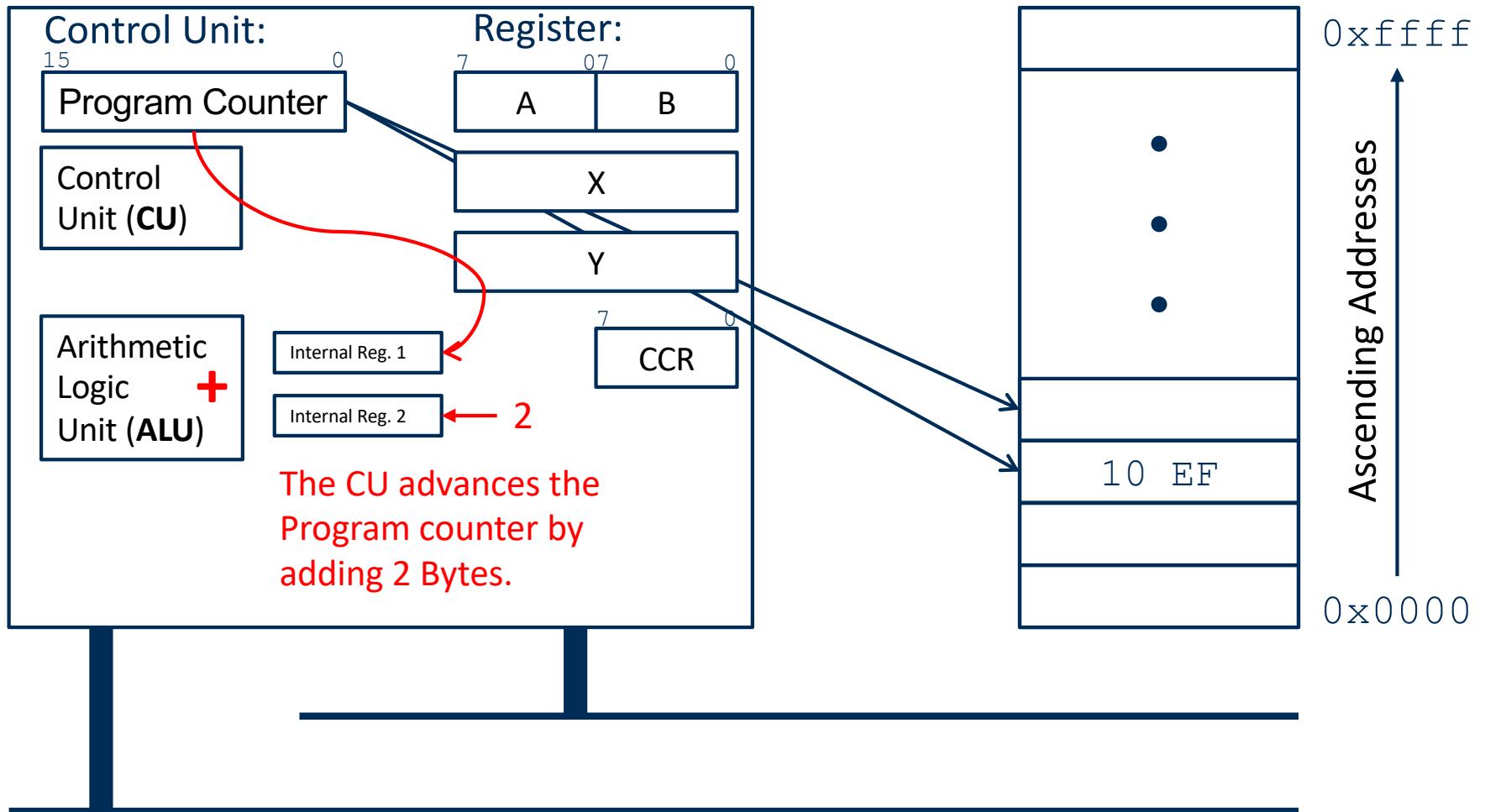
## CPU Phase 5: Write Back



In the last phase, the resulting value is written back – here to the FLAGS register CCR.

# REPETITION MICROPROCESSORS 6/6

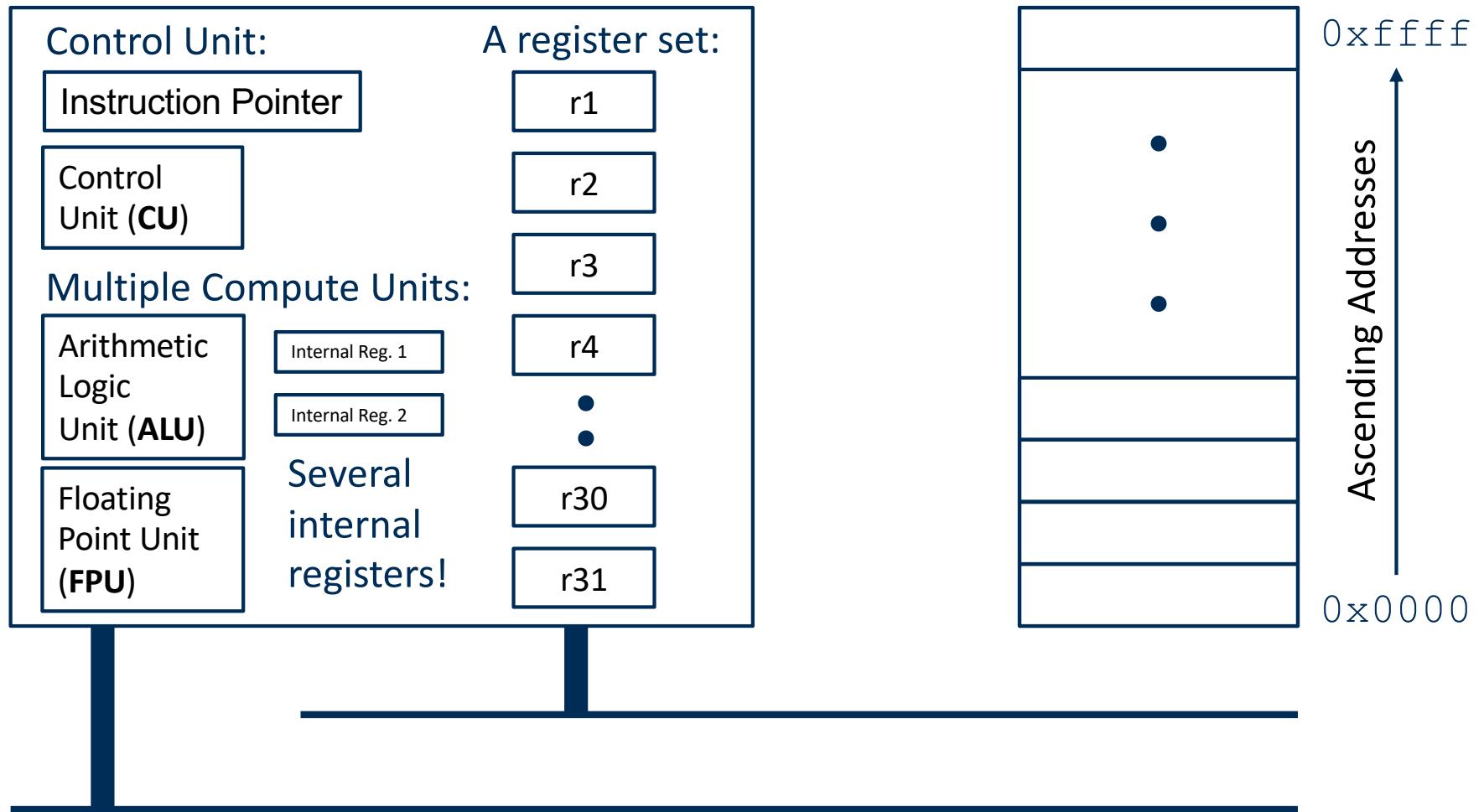
What about the next instruction?



Using the ALU, the CU computes the next pointer by adding the length of this instruction to the current value of the Program Counter (PC), or Instruction Pointer (IP) – here adding 2.

# REPETITION MICROPROCESSORS WRAPUP

Any CPU core is a generalization, i.e. each core has at least:

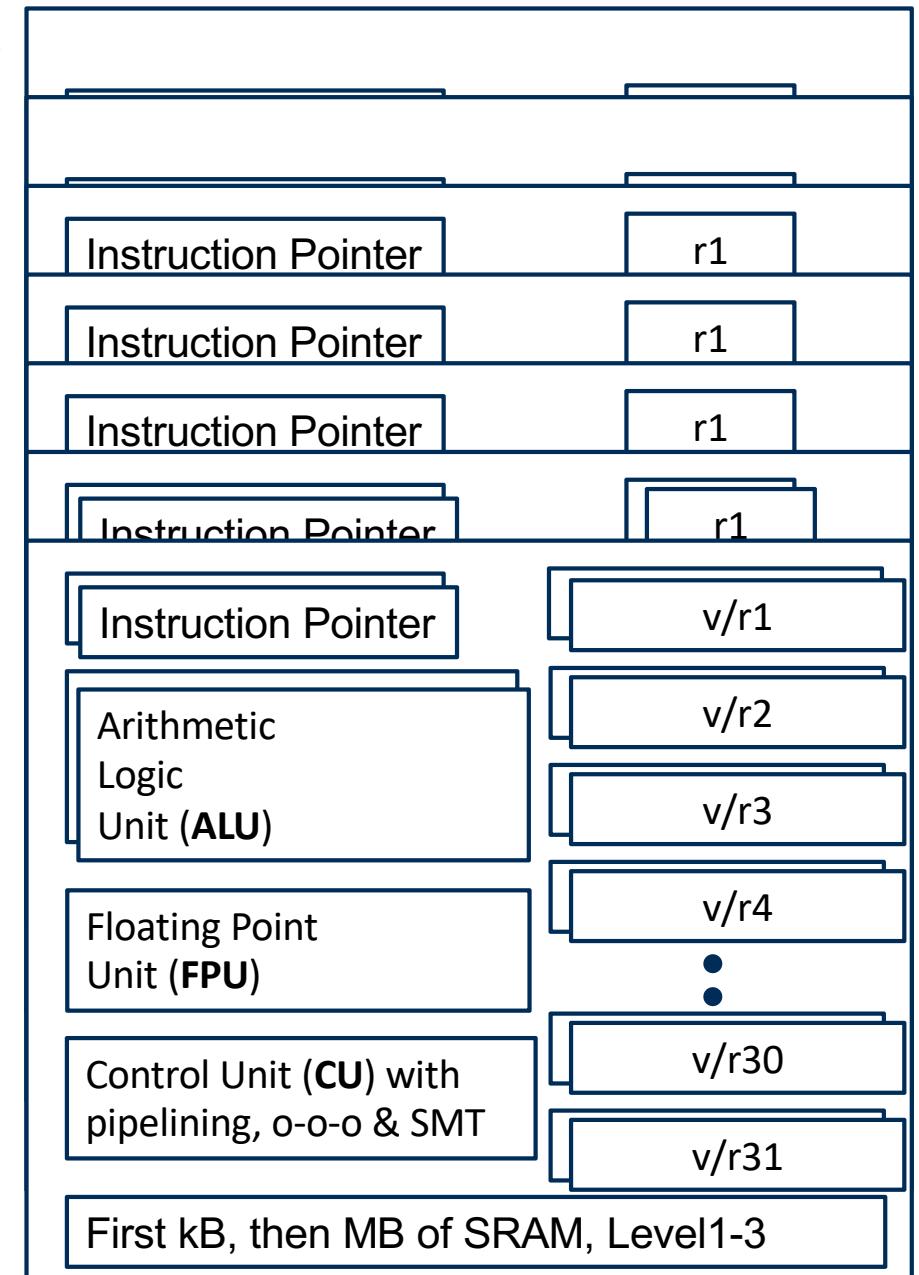


One or multiple buses; one or more address spaces to access code/data.

# MICROPROCESSORS

Steps for improvement: Compare Slide 12

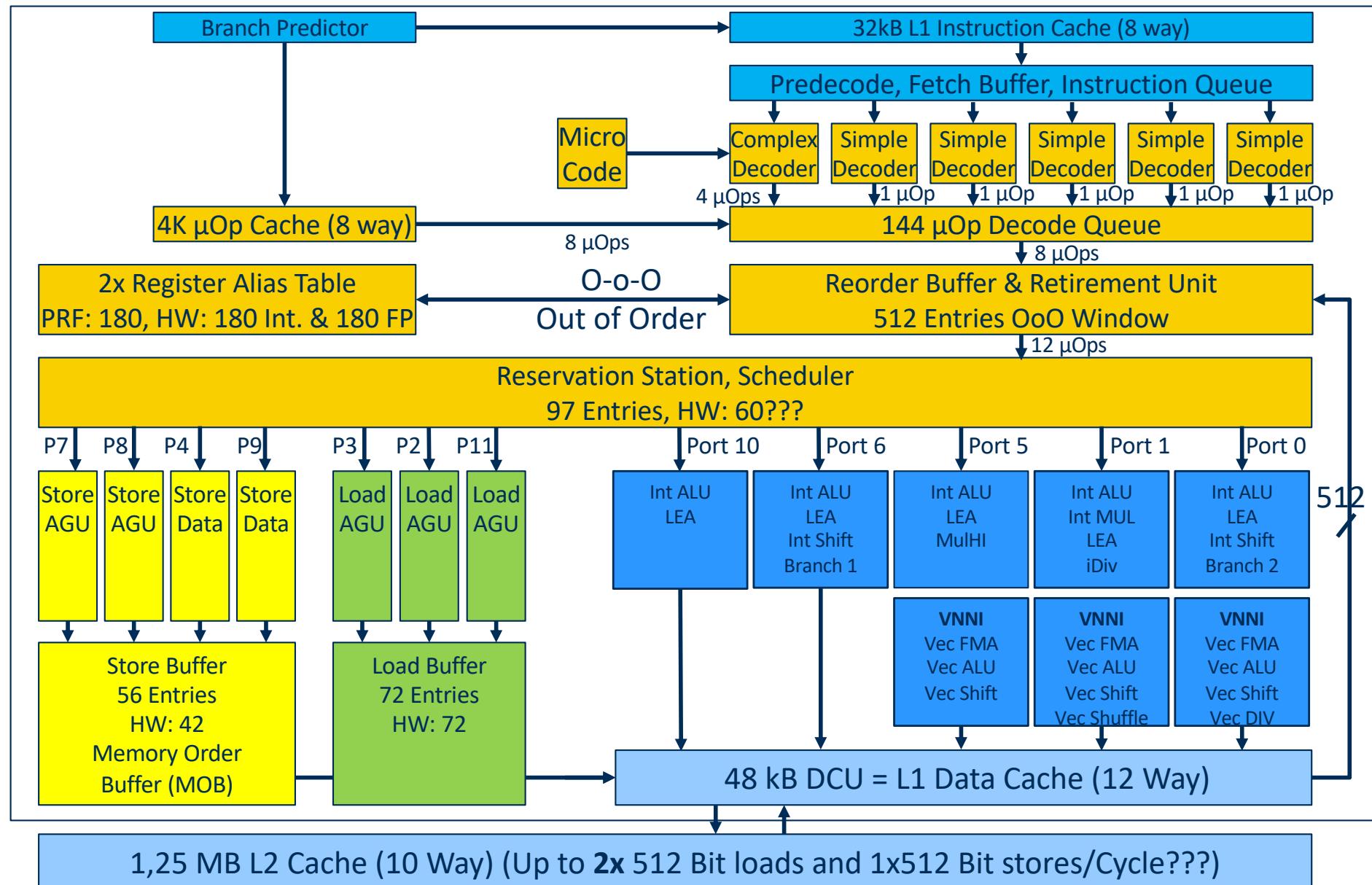
1. Instruction Pipelining (shorter circuits → higher MHz, complex CU, from 5 → 34 stages)
2. Add integrated Cache (fast SRAM decouples DRAM, may be I-/D-Cache, multiple levels)
3. Multiple Instructions per Cycle (duplicate units in ALU, or complete ALU and FPU)
4. Speculative Out-of-Order Execution (compensate for bad instruction order and possibly add more register-files!)
5. Hyperthreading / SMT (not 1 thread of execution, but have HW track 2 threads; needs duplicated state, i.e. 2 IPs, two register files, etc., complex CU)
6. MMX, SSE, AVX (Single-Instruction-Multiple Data, SIMD): vector-operations, e.g. Intel AVX-512: 8 FP doubles, 16 FP floats per register...
7. multi-core.... **Many-core** (not shown here)



Leading to todays:

# INTEL ALDER LAKE & RAPTOR LAKE MICROARCH. (2023)

P-Cores: Golden Cove are an extension of the Willow Cove architecture (~19% faster):



## LECTURE: LITERATURE

According to list of literature:

- Patterson, D., Hennessy, J.: *Computer Organization and Design*, Kaufmann, 2011  
(Deutsche Übersetzung: Rechnerorganisation und –entwurf, Spektrum)
- Hennessy, J., Patterson, D.: *Computer Architecture: A quantitative Approach, 5<sup>th</sup> edition*, Morgan Kaufmann, 2017
- Tanenbaum, A., Austin, T.: *Structured Computer Organization*, Pearson, 6<sup>th</sup> edition, 2013
- Tanenbaum, A., Austin, T.: *Rechnerarchitektur: von der digitalen Logik zum Parallelrechner*, Pearson, 6<sup>th</sup> ed., 2014
- Huang, H.W.: *The HCS12/9S12. An Introduction to the HW and SW interface*, Thomson Learning, 2009
- Beierlein, T.: *Taschenbuch Mikroprozessortechnik*, Carl-Hanser Verl., 2011

