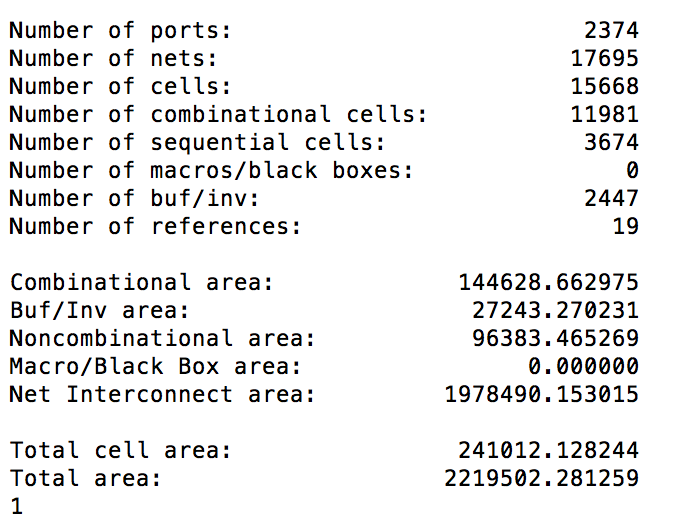
**DSD Final Project Scores (RISC-V)**

**1. Baseline**

(1) Area: (um2)

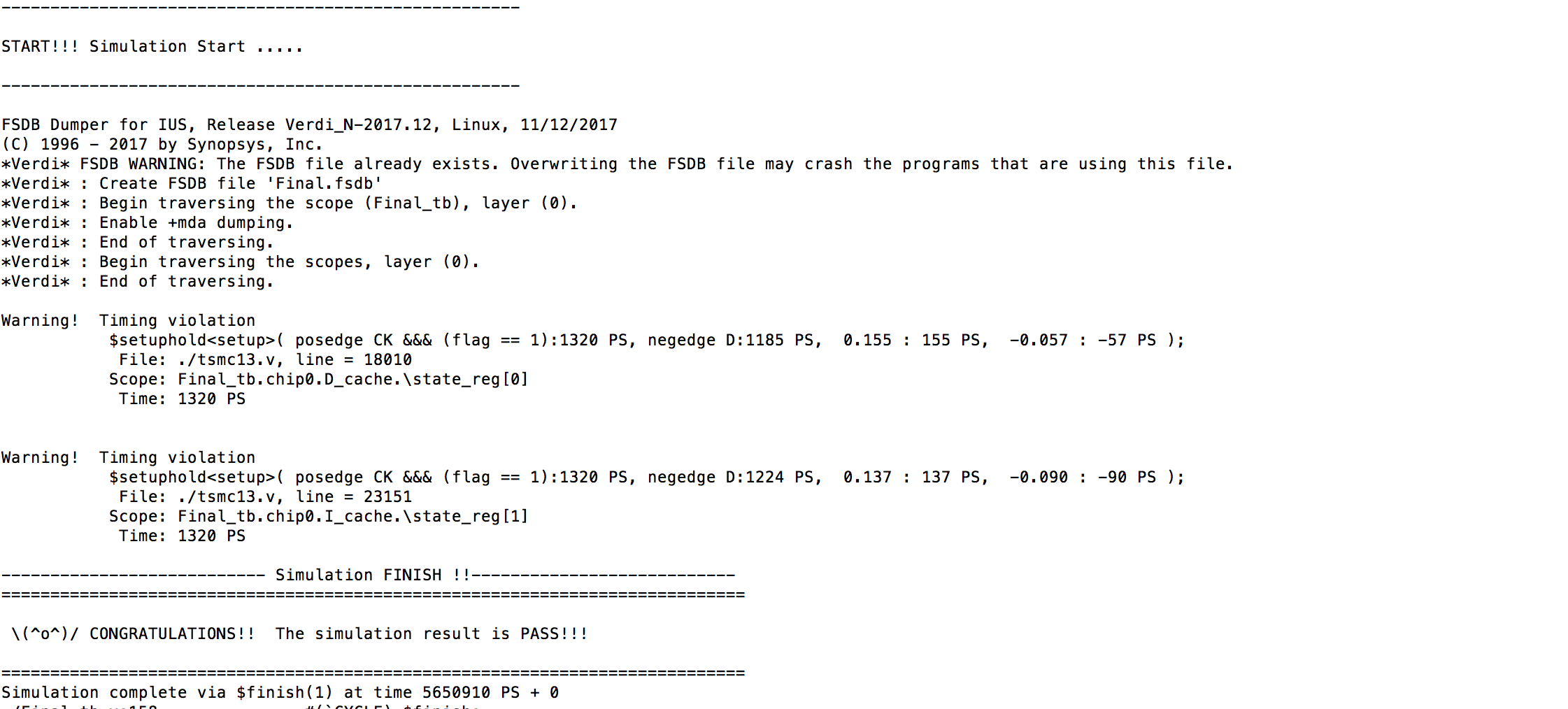
截圖:



A=241012

(2) Total Simulation Time of given hasHazard testbench: (ns)

截圖:



T=5650910(PS)=5651(ns)

(3) Area\*Total Simulation Time: (um2 \* ns)

1361958812

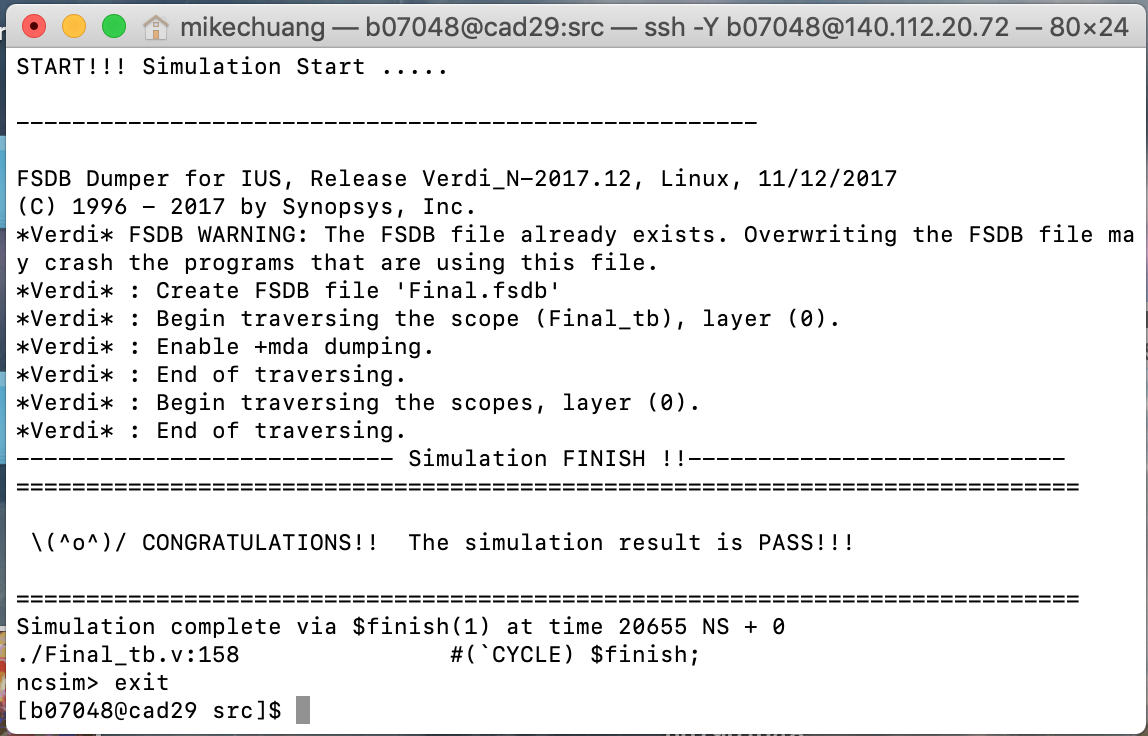
(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

2.5

**2. BrPred**

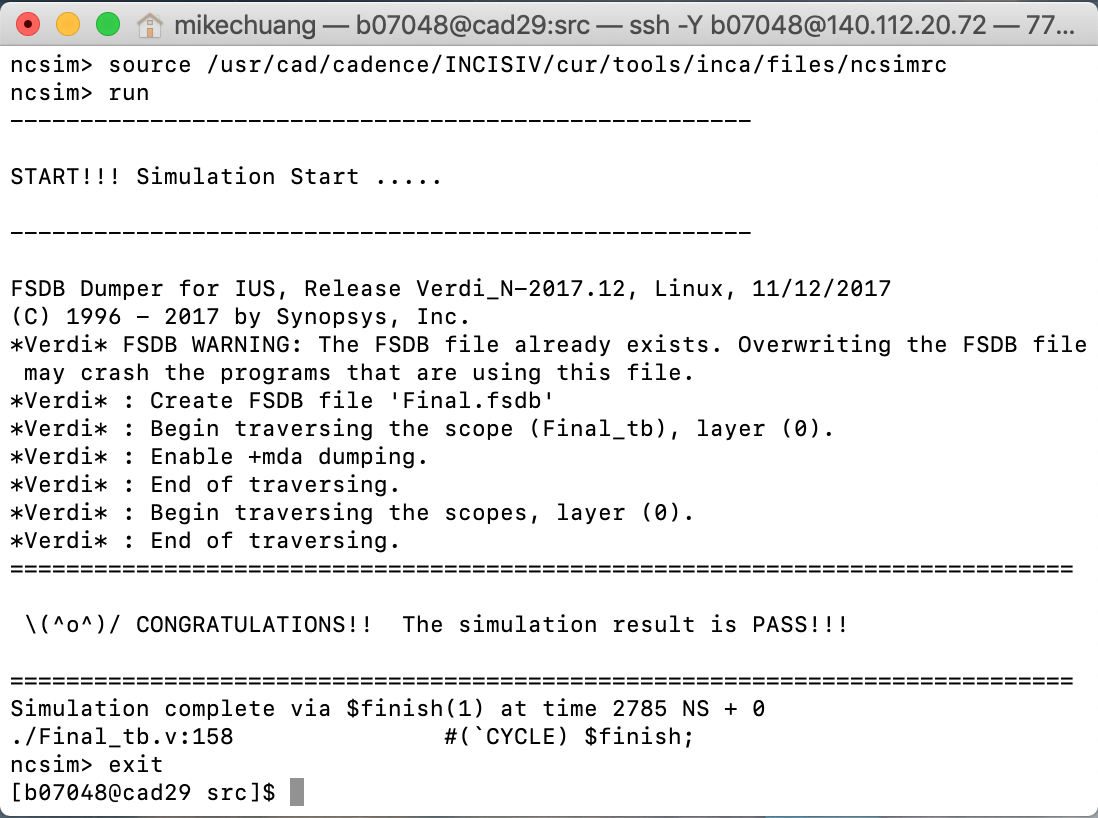
(1) Total execution cycles of given I\_mem\_BrPred:

264



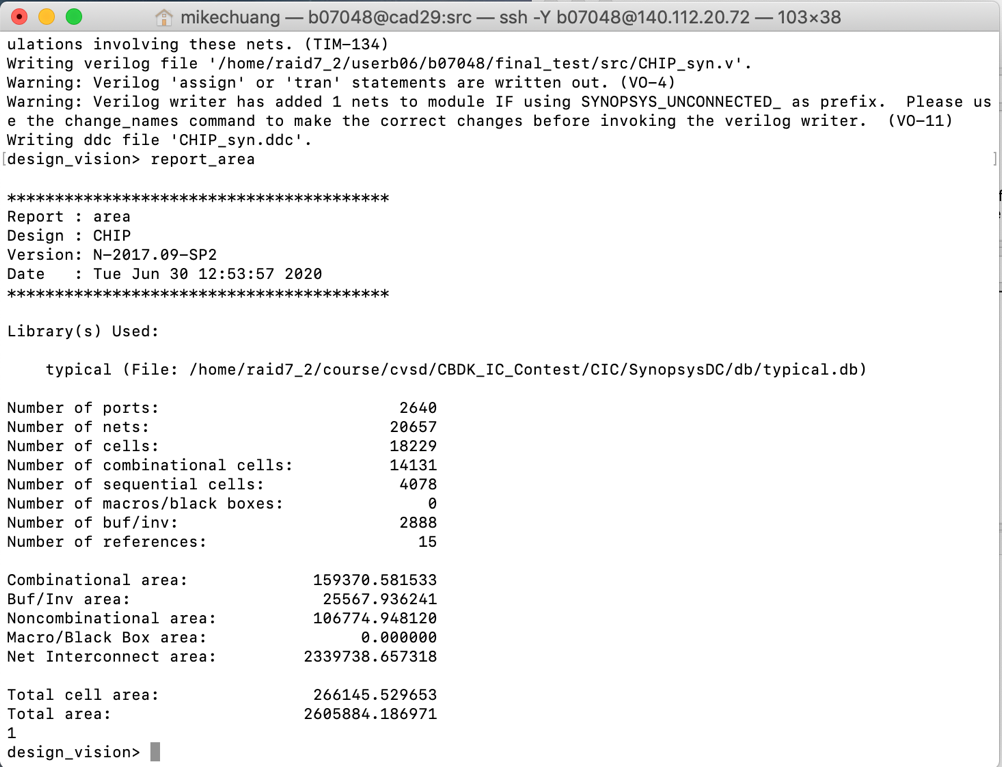
(2) Total execution cycles of given I\_mem\_hasHazard:

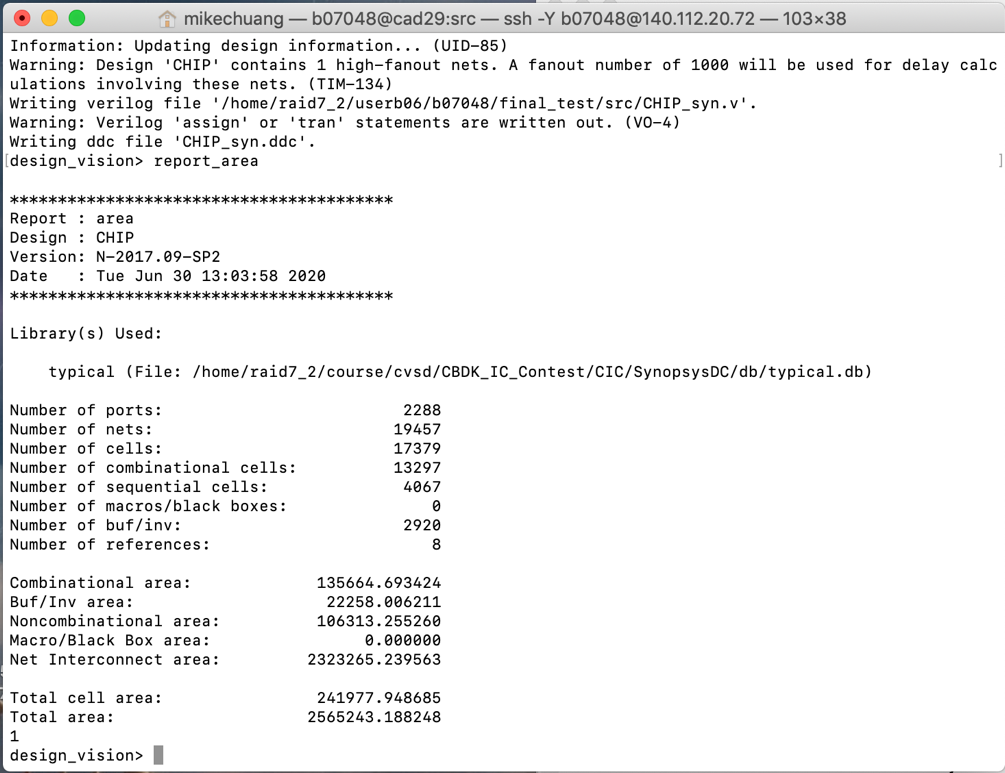
2051



(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um2)

24167.58097 under cycle = 4 ns





**3. L2 Cache**

(1) Average memory access time: (ns)

(2) Total execution time of given I\_mem\_L2Cache: (ns)

截圖:

**4. Compressed instructions**

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um2)

截圖:

(2) Total Simulation Time of given I\_mem\_compression: (ns)

截圖:

(3) Area\*Total Simulation Time: (um2 \* ns)

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)