KAI-CHUN (KEVIN) CHANG

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RESEARCH INTERESTS

My main research interest lies in the **design, modeling, verification, and safety of cyber-physical systems** (CPS), especially for (but not limited to) the application to **autonomous vehicles** and **transportation systems**. I am also interested in **electronic design automation (EDA)**, with a focus on timing analysis and optimization, physical design optimization, and machine learning for EDA.

EDUCATION

National Taiwan University (NTU)

Taipei, Taiwan

B.S. in Electrical Engineering (EE)

Sep. 2018 - June 2022

- Cum. GPA: **4.26/4.30**, ranking: **4/196 (2%)**, last-60-credits GPA: 4.28/4.30
- CPS/EDA related courses (all with an A+ grade): Introduction to Intelligent Vehicles (ranked No. 1 in the class), Logic Synthesis and Verification, Introduction to EDA, Physical Design for Nanometer ICs
- Algorithms/Mathematics Courses (all with an A+ grade): Algorithms (ranked No. 1 in the class), Data Structure and Programming, Convex Optimization, Discrete Mathematics, Differential Equation, Signals and Systems

PUBLICATIONS

- [1] **Kevin Kai-Chun Chang**, Xiangguo Liu, Chung-Wei Lin, Chao Huang, and Qi Zhu, "A Safety-Guaranteed Framework for Neural-Network-Based Planners in Connected Vehicles under Communication Disturbance", accepted to appear in *Design*, *Automation and Test in Europe Conference (DATE)*, April 2023
- [2] **Kevin Kai-Chun Chang**, Chun-Yao Chiang, Pei-Yu Lee, and Iris Hui-Ru Jiang, "Timing Macro Modeling with Graph Neural Networks", in *59th Design Automation Conference (DAC)*, July 2022

RESEARCH EXPERIENCE

Laboratory of Prof. Chung-Wei Lin

Taipei, Taiwan

Research Assistant

Sep. 2022 - Present

Undergraduate Researcher

Jan. 2022 - Aug. 2022

- Working with Professors Qi Zhu (Northwestern University) and Chao Huang (University of Liverpool).
- Proposed a safety-guaranteed framework for NN-based planners in connected vehicle environments, which achieved 100% safe rate under communication disturbance while preserving high efficiency.[DATE'23]

IRIS Lab (Prof. Iris Hui-Ru Jiang)

Taipei, Taiwan

Research Assistant

Sep. 2022 - Present

Undergraduate Researcher

July 2020 - Aug. 2022

- Proposed a novel timing macro modeling approach based on graph neural networks (GNNs), which achieved 10% macro model size improvement in comparison with the state-of-the-art work while preserving extremely high timing accuracy (less than 0.1ps timing error). [DAC'22]
- Incorporating the correlations between design corners and extending the GNN-based framework to various advanced node timing analysis and multi-corner multi-mode (MCMM) models.

HONORS AND AWARDS

1st Place in Bachelor's Thesis Award - NTU

June 2022

College Student Research Creativity Award – National Science and Technology Council (Taiwan)

June 2022

Travel Grant to DAC 2022 – Foundation for the Advancement of Outstanding Scholarship

June 2022

Academic Excellence Award (5 times) – EE Dept. at NTU

Fall '18 – Fall '21

Irving T. Ho Memorial Scholarship – EECS College at NTU

Fall 2021

Research Grant for College Students – National Science and Technology Council (Taiwan)

July '21 - Feb '22

3rd Place in Special Research Project Award - EE Dept. at NTU

July 2021

Bachelor Scholarship – Taiwan Semiconductor Manufacturing Co., Ltd. (TSMC)

Spring 2021

SERVICE

Journal Reviewer - IEEE TCAD (2021, 2022)

Conference Reviewer – ASP-DAC (2022), ISPD (2022, 2023)

WORK AND TEACHING EXPERIENCE

Synopsys, Inc.

Taipei, Taiwan

Technical-Engineering Intern in Digital Design Group

July 2021 - Aug. 2021

· Provided a thorough analysis on 3D IC routing strategies that effectively guides the development of related tools in the world-leading EDA company.

EE Dept. at NTU

Taipei, Taiwan

Teaching Assistant

Feb. 2021 - June 2021

- Algorithms (EE4033): Lectured 4 recitation classes, graded 6 assignments, and received several positive comments from students on the semester course feedback survey.
- Computer Architecture (EE4039): Designed a lab demonstrating memory hierarchy and gave an in-depth lecture about advanced dynamic random-access memory (DRAM) technologies.

SELECTED PROJECTS

Graph-based Interchange Management

[project link]

Course Final Project of Introduction to Intelligent Vehicles

Jan. 2022

- Formulated the highway interchange management problem and converted it into a constraint graph.
- Guaranteed safety and improved passing time by 10% compared to the first-come-first-serve strategy based on the graph and simulated annealing.

Learning Weights and Thresholds of Threshold Logic Networks

[project link]

Course Final Project of Logic Synthesis and Verification

Jan. 2022

- Proposed two neural-network-based approaches to determine weights and thresholds for threshold logic networks with given input-output relations.
- Achieved near 80% accuracy in the function-based method and 70% to 90% accuracy in the networkbased method.

Macro Legalization [project link]

Course Final Project of Physical Design for Nanometer ICs

June 2021

- Proposed a graph-based macro legalization algorithm flow which combined iterative refinement and simulated annealing.
- Ranked No.1 in the final report writing.

TECHNICAL SKILLS

Programming Languages: C/C++(STL), Python, Tcl/Tk, Verilog, Go, MATLAB

Libraries and Toolkits: Git, Docker, LaTeX, Linux, PyTorch

LEADERSHIP AND VOLUNTEER ACTIVITIES

MakeNTU

[website] Taipei, Taiwan

Oct. 2020 - May 2021

General Coordinator Led 100+ staffs and managed over 1 million NTD budget to hold MakeNTU, one of the largest Makeathon

 Designed multiple plans to meet sponsors' requirements, remain within budget, and adapt to COVID-19 precaution policies.

NTU Changhua Family Service Camp

Changhua, Taiwan

General Coordinator

contests in Taiwan.

Aug. 2019 - Jan. 2020

 Led 60+ volunteers to hold a winter camp for 80 students from a rural elementary school in our hometown.