Lab 4 Notes

Kevin Chau 23816929
Lab Partner: Zander Giuffrida

Pre-lab:

See attached notes for pre-lab answers

Signatures:

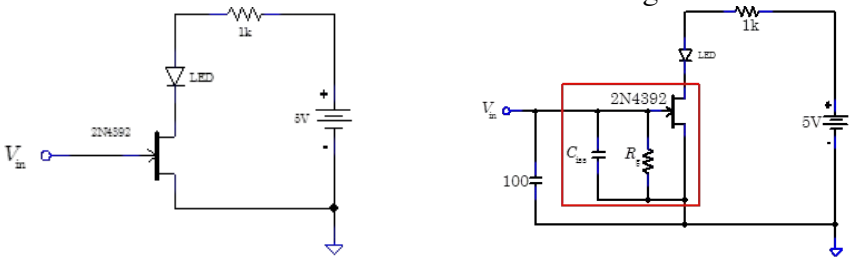
See attached notes for signatures for the pre-lab, 4.3, 4.6, 4.10, 4.11

Problem 4.0

To test that our 2N4392 JFET was working properly, we measured the resistances between various pins using the DMM. We recorded the results R_{GS} = 4.5MΩ , R_{GD} = 4.5MΩ, R_{GD} = 37Ω. The 2N4392 datasheet specifies a drain-source resistance of 60 Ohms max while the JFET we used was working reasonably.

Problem 4.1

We used a JFET and an LED to build the following circuit:



Touching the Gate lead to Ground: LED ON
Touching the Gate Lead to -12V: LED OFF
With the 2.2M resistor, we can still turn on the LED. This is because the JFET can still drive enough current through the LED even with a small input voltage (as in the transistor has amplifying characteristics).

Problem 4.2

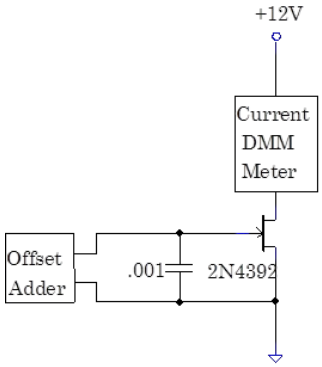
Then we used a stopwatch to measure the "forgetting" time, i.e. the time it took the capacitor to discharge and for the LED to turn on. Without any extra external capacitances, the times were: 1.815s, 1.70s, 1.75s, 1.38s, 1.68s, 1.38s. The average of these times was T_1 = 1.6175s.

With an extra 100uF capactor connected as in the diagram above, the discharging times for the JFET's memory were: 8.355s, 7.86s, 7.7s, 7.51s, 7.89s, 8.61s, 8.215s. The average of these times was T_2 = 8.02s.

We know the time constant for the discharge is R_gC_{iss}. Since we weren't able to measure R_s directly, we can use our two time averages to figure out C_{iss} and then R_g. Eliminating R_g we solved for C_{iss} = 25.35pF. Thus R_g = 63.8GΩ.

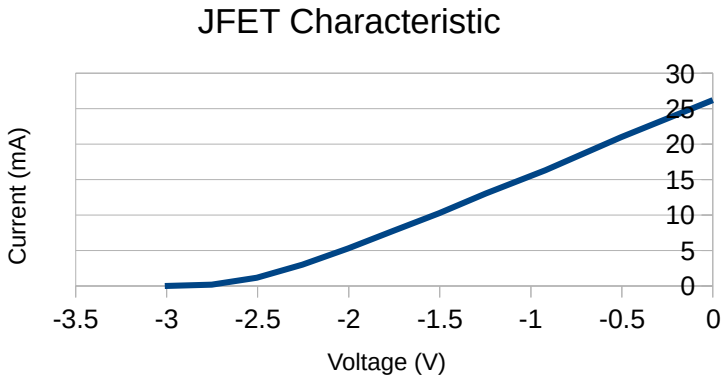
Problem 4.3

We built the following circuit:

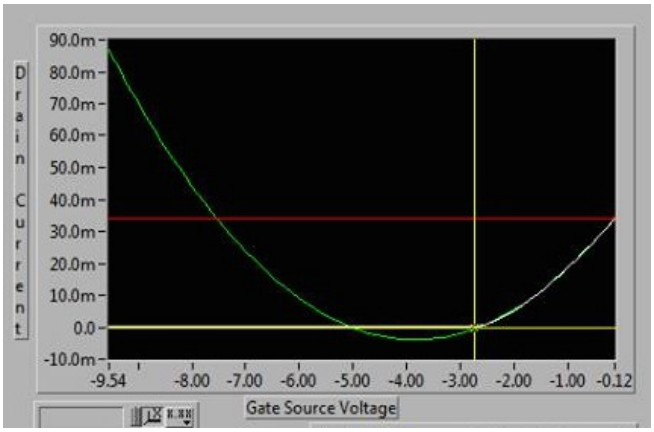


The nominal .001 uF capacitor we used measured 1.085 nF.
The lowest voltage where we got non-negligible current was -3.32V. The current at that point was 0.3uA. Then we took plotted points to determine the gate voltage and current relationship of the JFET:

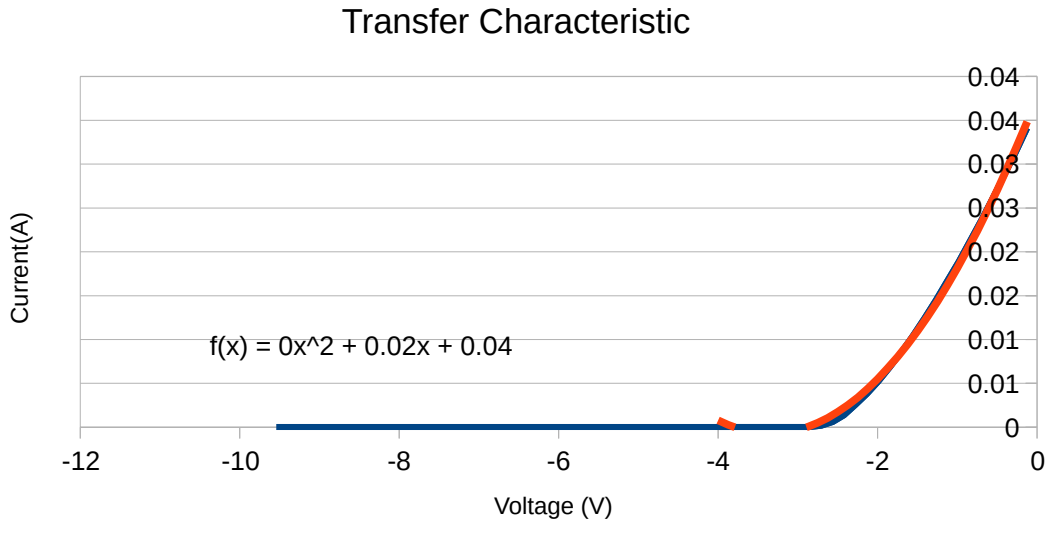
V_{GS} (V)	I_{DS} (A)
-3.01	0.0093
-2.753	0.1844
-2.505	1.182
-2.254	3.01
-2.002	5.3
-1.75	7.8
-1.503	10.273
-1.247	13.051
-0.92	16.3
-0.504	20.965
0	26.2

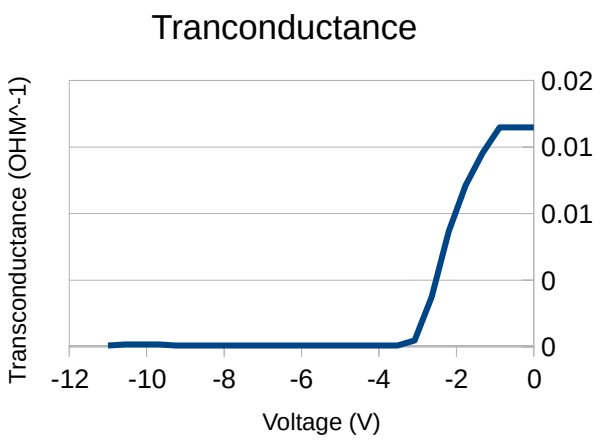


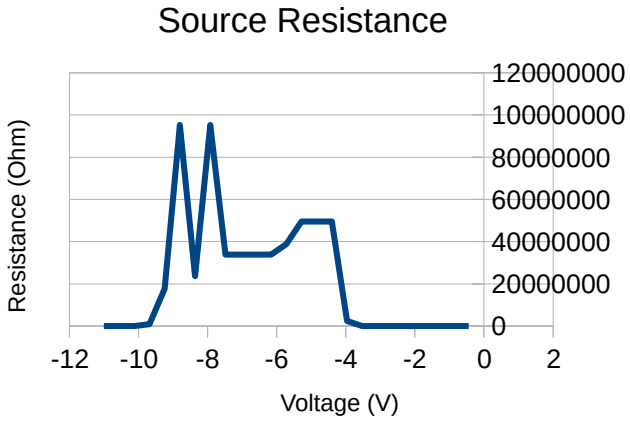
Problem 4.4
Using the Curve Tracer, we took the following data.
JFET Characteristic Curve:



The Curve Tracer was able to fit the characteristic with a parabola well, although the parabolic model only works well when the voltage is over -3.00V. Before this voltage, the curve is essentially just flat and does not have polynomial behavior. We also plotted the data in our own spreadsheet and performed a quadratic regression to check the model. Below shows the same transfer curve data plus the points taken by hand and the quadratic fit. We also show here the transconductance and source resistance curves. The equation for the regression is approximately $I(v) = .0034x^2+.0229v+.0376$.

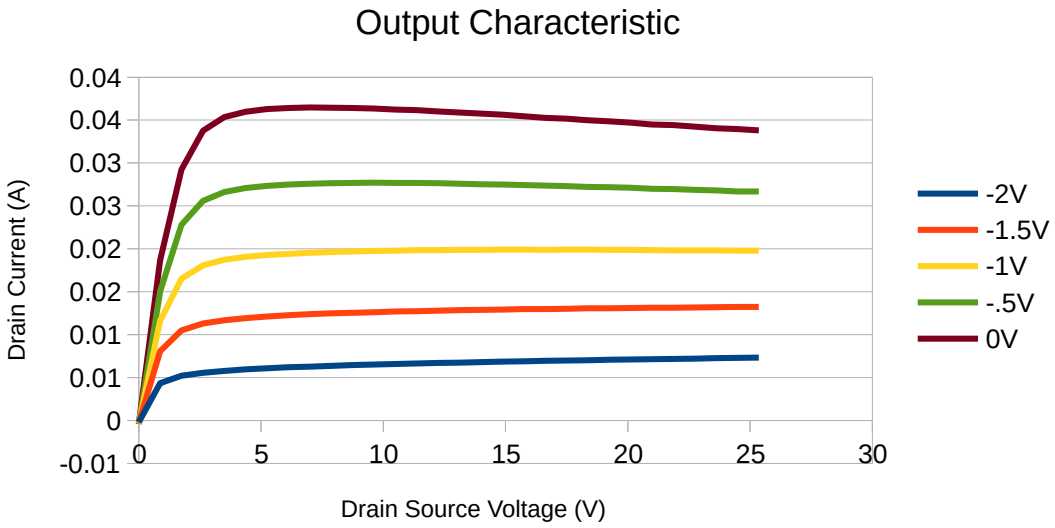






We manually took the derivative of the transfer curve at -1V to find an estimate of the transconductance. Linearizing the curve at the point of V=-1 we get a slope of 0.0156 1/Ohm (if we take the derivative of the quadratic fit, we get something like .0222, which isn't bad). According to the transconductance curve generated by the curve tracer, the transconductance at -1V should be just under 0.015, so the data agrees.

Then we plotted the output characteristic of the JFET:



Problem 4.5

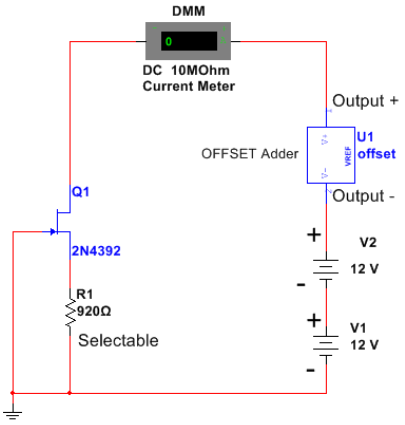
We obtained a new JFET. We used the DMM to measure current and the multimeter to measure the voltage provided by the offset adder. With V_{DS} = 12V as in problem 4.3, we set the gate voltage for a current of about 1.0235mA initially. The voltage we needed for this was V_{GS} = -3.026V. The current drifted upward slowly. It took about a minute for the current to stabilize at 1.030mA.

Next we set V_{GS} = -1.643, for a starting current of 15.0 mA. The current drifted down much quicker than when the current was at 1mA. After a couple of minutes the current stabilized at 13.5mA. Using the 37Ohm Drain Source resistance measured in 4.0, we can calculate the power dissipation using Ohm's Law: P = (I^2)R. Thus we find that the power being burned by the JFET is P = (.0135^2)(37) = 6.74 mW. We can also estimate the power by looking at the JFET data sheet which says there's a max resistance of 60 ohms or by looking at the source resistance curve in 4.4, which also gives a value of roughly 60 ohms—this gives a power dissipation of about 10.9mW

Then we cooled the JFET using circuit coolant. The DMM made a current reading as high as 19.2mA right when the coolant was applied, and then drifted back down to the previous current value as it warmed up.

Problem 4.6

We built the following circuit to test the self-biased current source:

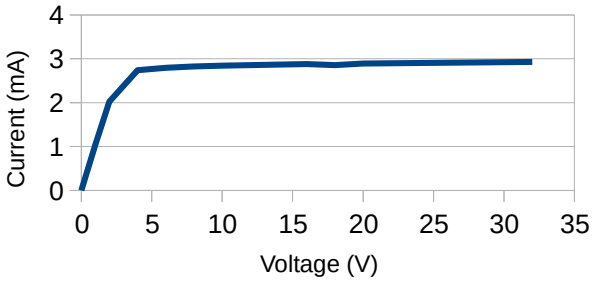


The resistor R1 had a measured of resistance of R1 = 897.6Ohm (920 nominal).
First we used one +12V voltage drop with the power supply and the offset adder set to 0V, so that the Voltage from Drain to Ground was 12V. The measured current was I = 2.858mA. This was within 2.7mA and 3.3mA, so we didn't need to change the resistor to get an appropriate value specified by the lab manual.

With coolant on the JFET, the current with 12V across the JFET was I = 2.850mA. The current changed noticeably but the value did not deviate far from the original measured value of 2.858mA at room temperature.

Then we used combinations of 0V, 12V, and 24V from the power supply and the offset adder to scan a range of 0 to 32V across the JFET and R1. The data below shows the output currents as a function of gate voltage.

$V_{D\text{-}GND}$ (V)	I_{DS} (mA)		
0	0.0005	16	2.877
1	1.05	18	2.855
2	2.0225	20	2.8933
4	2.7395	22	2.899
6	2.7963	24	2.9065
8	2.8235	26	2.9125
10	2.8415	28	2.9185
12	2.855	30	2.924
14	2.8672	32	2.9295



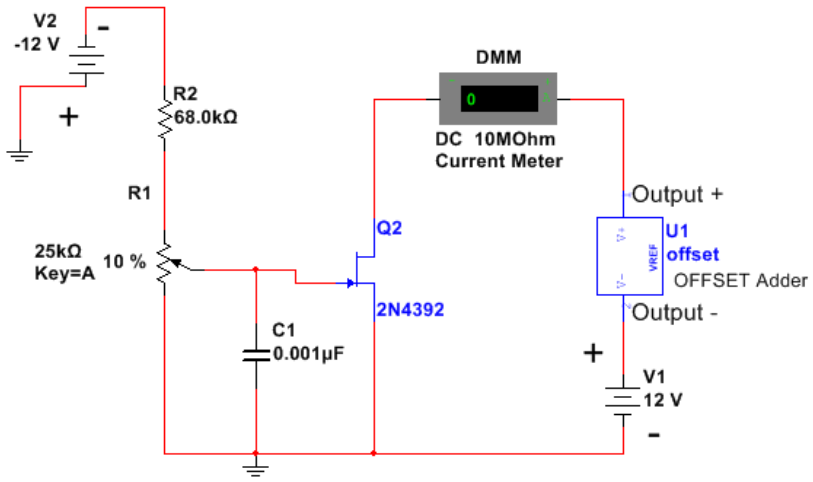
The circuit is a reliable current source past 5V, it provides nearly constant current for different voltages.

Problem 4.7

We substituted the resistor is 4.6 with a resistor with 10.43kΩ. With 12.00V applied across the JFET and resistor, we get a new current of 0.2853mA measured with the DMM. Then we used the offset adder to scan from 3.811V to 21.16V across the circuit. With this range we got a current output range of 0.275mA to 0.288mA. The JFET still acts as a good current source since the transistor is self-biased.

Problem 4.8

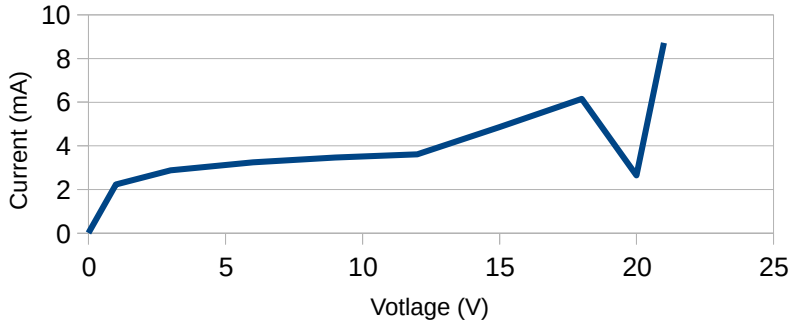
Now we try to externally bias a current source. We build the following circuit:



In place of the nominal resistance listed in the diagram, we used a resistor with the measurement R2 = 67.1kΩ. We also used a C1 = .001uF capacitor as in the diagram. Then we adjusted the potentiometer until we got a current of I = 3.003mA. This corresponded to a potentiometer voltage of V_{pot} = -3.20V.

We varied the voltage with the adder to scan a range from 0V to 21V. The following table has our output current data. There is a linear regime around 3mA.

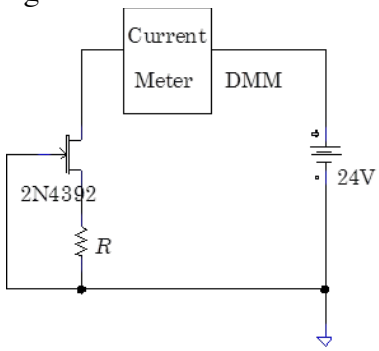
$V_{D\text{-}GND}$ (V)	I_{DS} (mA)
0	0.005
1	2.23
3	2.873
6	3.244
9	3.459
12	3.609
15	4.86
18	6.15
20	2.65
21	8.71



At 12V with circuit cooler, the output current was 6.01mA. This was quite a significant change form the uncooled value. There was a much larger percentage change in value compared to the self-biased source.

Problem 4.9

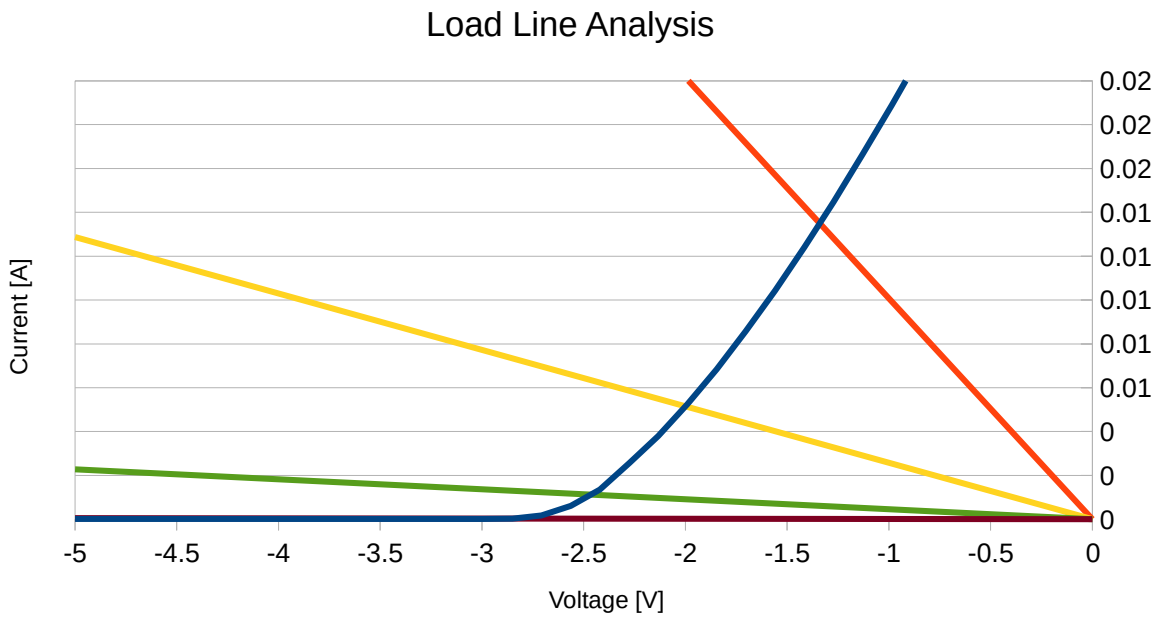
We built the following circuit, replacing the offset adder with the 24V power supply terminals.



For the nominal 100, 390, 2.2k, and 10k resistors, we used the following values (in order): 99.25, 388.37, 2.24k, and 9.89k. We measured the output current for all of these resistors:

R_s (Ohm)	I (mA)
99.25	14.6
388.38	5.844
2240	1.331
9890	0.31

Performing load line analysis, we see that the measured values agree with the values predicted in the output characteristic data taken in 4.3. For example, the red line below shows the 100Ohm line. The line intersects the transfer curve at about .015 A and -1.5V (approximately). The current value of 14.6mA fits this intersection well. Furthermore, we can look at the -1.5V curve of the output characteristic and we see that the current should fall between 10 and 15mA, so the data is acceptable.



Problem 4.10

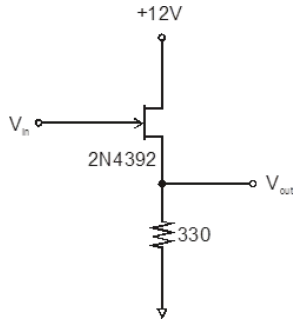
Graphs for the data in 4.6 and 4.8 are shown in each respective section.
For the self biased source, we chose a delta V of 2V to calculate stiffness. For the externally biased source, we used a 3V separation. We calculated the stiff for several pairs of data in 4.6 and 4.8 and then found the average stiffness of both the self and externally biased source.

ΔV	ΔI/ΔV (mA/V)	ΔV	ΔI/ΔV (mA/V)
30-28	0.00275	6-3	0.1855
26-24	0.0031	9-6	0.1075
22-20	0.0033	12-9	0.075
18-16	0.00425	15-12	0.06255
14-12	0.00585		
12-10	0.007		

Left: Self Biased Source Right: Externally Biased Source

The average stiffness for the self biased source was 0.004375. spanning a range from .00275 to .007.
The average stiffness for the externally biased source was 0.2484, spanning .075 and .1855.
Overall, the self biased source seems to have better stiffness (which agrees with our findings).

Problem 4.11
We built the following source follower:



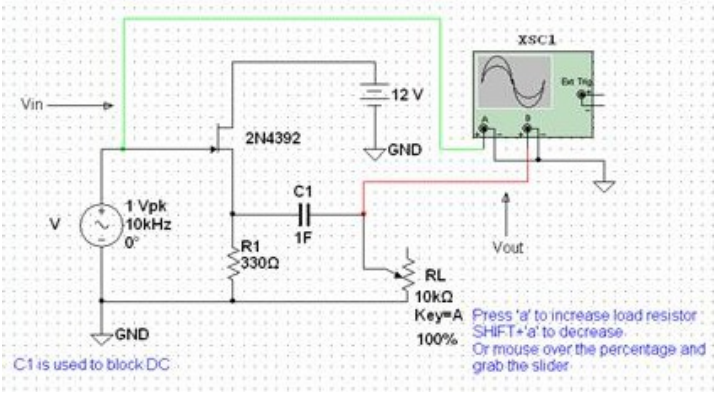
The resistor we used measured R_s = 325.97 Ohm.
Wave generator set to Sine wave.
The output was dead when the offset dropped below -3.7V.

Frequency	$V_{pp,in}$	Offset	$V_{pp,out}$
1000	1	0	720
1000	5	0	3800
100000	1	0	640
10	1	0	540
1000	1	5	760
10000	1	5	740
1000000	1	5	280
1000000	1	0	248
1000	1	-1	720
1000	1	-2	660
1000	1	-3	472
1000	1	-3.7	230
1000	1	-4 DEAD	

The output amplitude of the source follower is always less than the input, so the follower has some non-ideal attenuating behavior. This offset makes sense since we are using a small resistance value. The 330 Ohm resistor may be comparable to the source resistor r_s the JFET, so there may be a small voltage divider effect going on. Ideally, the resistor in the follower should be large to reduce this effect.

Problem 4.12
Then we removed the offset adder from the follower circuit. We drove the circuit directly with 1kHz sine wave from the signal generator. We measured the difference in the amplitudes of the input and output: $\Delta V = V_{pp,out} - V_{pp,in} = 1.10V - 0.880V = -.22V$.
Then the gain G is just $G = 1 + \Delta V/V_{in} = 1 + -.22/1.10V = 1-.2 = .8$
This value seems to agree with our data from 4.12.
Then we set the input to zero, and measured the gate source voltage of V_{GS} = -2.164V.
From the transfer curve in problem 4.3, we estimate that this corresponds to a current of about 5mA.
Thus the source resistance of the JFET is just $V_{GS} / .005 = 2.1621/.005 = 429.72$ Ohm. This explains why our choice of 330Ohm for the resistor in 4.11 resulted in a poor performing follower. Furthermore, we can now calculate a predicted gain of $G = R_s / (R_s + r_s) = 325.9 /(325.9+429.72) = 0.4297$. The gains calculated match to within the same order of magnitude, but are off by a factor of 2.

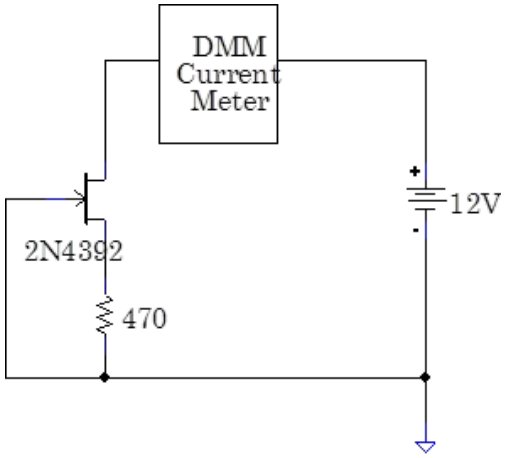
Problem 4.13
We studied this circuit is MultiSim:



Potentiometer increment set to 1%.
As we decrease the load impedance the output amplitude decreases.
By varying the load resistor until channel B had half the amplitude of channel A in the simulated oscilloscope, we were able to determine the output impedance of the modeled follower.
Output Impedance = 0.9% * 10k = 90 Ohm.
Then from the equation $Z = r_s R_s / (r_s + R_s)$ we can determine the source resistance (inverse of transconductance) with $R_s = 330$ as in the diagram. We get $r_s = 123.75$

The blocking capacitor is necessary in this circuit because it acts as a high pass filter with R_s. It blocks DC signals which is necessary since this is an AC source follower.

Problem 4.14
For this problem we studied the circuit below:

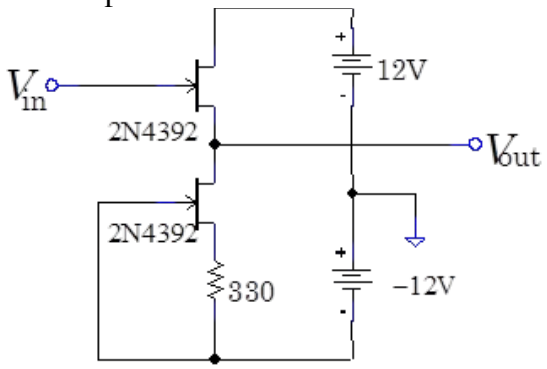


In our circuit we used a resistor R = 480.19 Ohm.
The original JFET current for this circuit was I = 4.8475mA.
We then tested 5 other JFETs, looking for the best characteristic match within 10% of this current.

JFET #	Current (mA)
1	4.942
2	4.455
3	4.894
4	4.1125
5	4.807

JFET 5 matched our original the best, with a current error of only 0.835%

Problem 4.15
The matched JFETs from the previous problem were used to build a current-source driven follower:

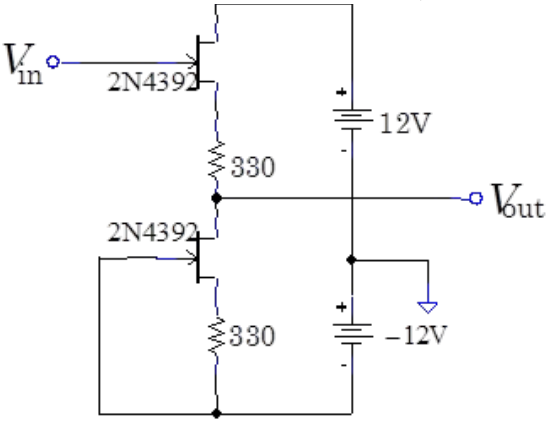


Here we used a resistor of value 341.19 Ohm.
The stiffness calculated in 4.10 was .004375 for the self-biased current source.
The wave generator was set to 1Vpp with a sine wave.
Here we compare the input and output signals:

Frequency	Vpp,in	Vpp,out
1000	1.04	1.04
100000	1.04	1.04
10000	1.04	1.04
100	1.06	1.04
1000000	1.04	0.96

The oscilloscope showed some DC offsets in the two signals, but overall the output was not noticeably attenuated (this follower works well). We can calculate the gain from the stiffness already found. The stiffness of .004375 in 4.10 was calculated in units of mA/V and are just inverse ohm's. So with the current source driving the follower, we can say R_s = (0.004375/1000)^ -1 = 228571 Ohm = 230 kOhm. In the operating range, the follower has an internal transconductance of approximately 0.015, so r_s = 66.7. Thus the gain is just G = R_s/ (R_s + r_s) = 228571 / (228571+66.7) = .9997. This is nearly a factor of unity so the gain calculation matches our data. The source driven follower works well.

Problem 4.16
Now we insert a resistor between V_{out} and the first JFET's drain, as follows:



The resistor had a value of R = 325.01 Ohm.
With a 100Hz Sine wave we measured a Vpp,in of 1.06V and a Vpp,out of 1.04. The source follower works almost identically to the previous circuit. However, this time there was no DC offset between the two signals. Since the DC offset comes from differences in the two JFET characteristic, the secondary resistor helps to make better match these transistors and smooth out their differences. Since both resistors have the same resistor now, and r_s is typically small, we know that the resistor will kill off the DC offset.

Problem 4.17

JFET followers stay linear over a wide range of input voltage, yet the gain depends on the transconductance, which in turn depends on the gate voltage. Explain how feedback keeps the amplifier linear:

The follower uses feedback much like the self-biased current source. However, instead of grounding the gate, we drive an input signal into the follower. The feedback allows the JFET to adjust its current to keep VGS at an appropriate value for the current. The feedback also keeps the gate reverse biased. If there is a large positive voltage trying to forward bias VGS, then the current through R_s increases immediately which in turn increases the source voltage and forces VGS negative. Thus feedback allows the JFET to act linearly over a range of voltages, even though the gain and transconductance depend on the gate voltage.

Problem 4.18

Then we used the Curve Tracer to plot the transfer characteristic of the 2N3819, a different JFET than the one used in the lab. The following plots show the transfer curve, transconductance, and source resistance of this new JFET. The 2N3819 fit a parabolic curve very well. In comparison with the 2N4392, I'd say the fit is better but both transistors fit a parabolic model very well. The equation given by the quadratic regression is $I(v) = .00073v^2+.0053v+.0091$ (in the graph, the fit line is rounded up for the coefficients). The blue line shows the data given by the curve tracer, while the red line is the regression line.