1 Designing complex logic gates (Problem 5)

1.1 Problem

Given a complex logic function, design a static CMOS gate that implements the function.

$$F = \overline{(A + B + C)(D + E)}$$

1.2 Solution

First, simplify the expression. We can see that the above expression has only one literal for each input, so no further simplification is possible. Second, make sure that the entire expression is inverted. Remember that CMOS logic is inherently inverting, so every function should have a bar across the entire expression before converting. Third, translate into CMOS!

To translate a function into CMOS, start with the pull-down network. The pull-down network (PDN) will match the expression. Remember that OR operations become transistors in parallel, and AND operations become transistors in series. Figure 1 shows a good choice for a PDN. This is not the only possibility.

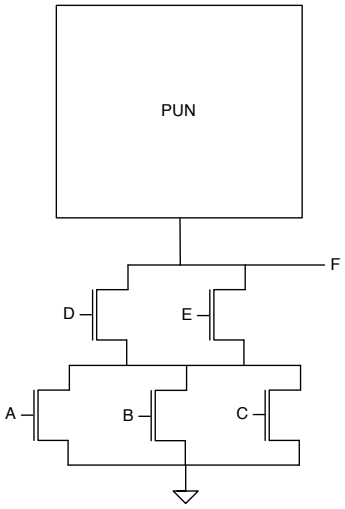


Figure 1: Pull-Down Network for the given Boolean function

Next, design the pull-up network (PUN). Remember that the PUN is the dual the PDN. Transistors in parallel become transistors in series, and transistors in series become transistors in parallel. Figure 2 shows the PUN for the PDN in Figure 1.

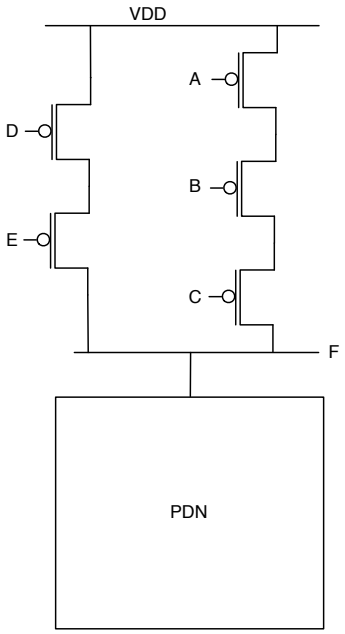


Figure 2: Pull-Up Network for the given Boolean function

Finally, we just need to size the transistors and we're done. For each network, we want the worst-case resistance to equal the resistance of a minimum-sized inverter. Remember that resistance through a device is inversely proportional to its width. In the PDN, the worst-case resistance is always through just two NMOS devices. While it's true that the resistance of the D and E transistors in parallel is less that that of a single NMOS transistor, in the worst case, only one of them is on. Thus each device needs a size of 2 so that the total resistance through any path is 1 or less. For the PUN, there are only two possible paths, so sizing is relatively easy. D and E transistors get a size of 4, and A, B, and C transistors get a size of 6. The final gate is shown in Figure 3.

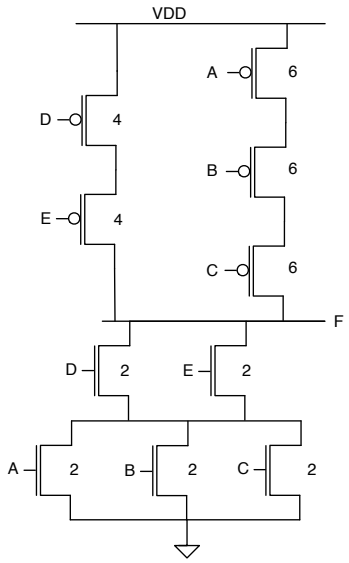


Figure 3: Complete gate with sizing for the given Boolean function

2 CMOS gate sizing

To size a complex CMOS gate, find the worst-case path through the logic network, and size accordingly. Remember that resistance is inversely proportional to the transistor width. For transistors not on the worst-case path, size them so that that path's resistance is also equal to the inverter resistance.

$$R_{path} = R_{M1} + R_{M2} + ... \tag{1}$$

assuming that M1, M2, etc. are in series. Transistors in parallel are ignored because in the worst case, only one of them is on.

$$\frac{1}{W_{path}} = \frac{1}{W_{M1}} + \frac{1}{W_{M2}} + ... \tag{2}$$

where W_{path} is the width of a minimally sized inverter, so W_{path} is 1 for the PDN and 2 for the PUN. Do this for all paths in the PUN and PDN to find the size of every transistor.

3 VTC and simple switch model (Problem 6)

3.1 Problem

Suppose we use a simple switch model with $R_{ON,N} = 2R_{ON,P} = R$ and $V_{TH,N} = |V_{TH,P}| = V_{TH} = 0.25V$. What is the VTC of the inverter below?

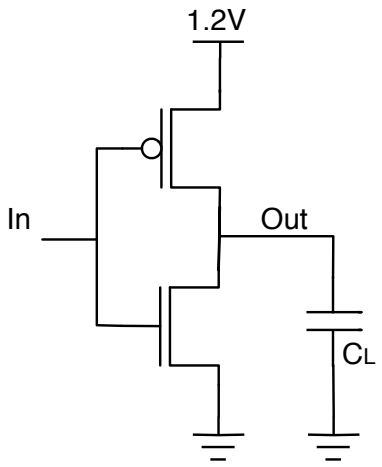


Figure 4: Inverter Schematic

3.2 Solution

Vary the input voltage from 0 to V_{DD} to find the switch states and output voltage. For $V_{in} < V_{TH}$, the PMOS is on and the NMOS is off, so the steady-state output voltage is simply V_{DD}. As V_{in} rises above V_{TH}, the NMOS turns on, making the output voltage determined by a resistive divider, with the top resistor R and the bottom resistor $2R$. Thus the output voltage is $\frac{2}{3}V_{DD}$. Now, as V_{in} further increases, the PMOS turns off. This occurs for $V_{in} > V_{DD} - V_{TH}$. Here only the NMOS is on, and the output is at zero. The VTC is shown below.

Please review the lecture slide on noise margins for how to find them in the above VTC.

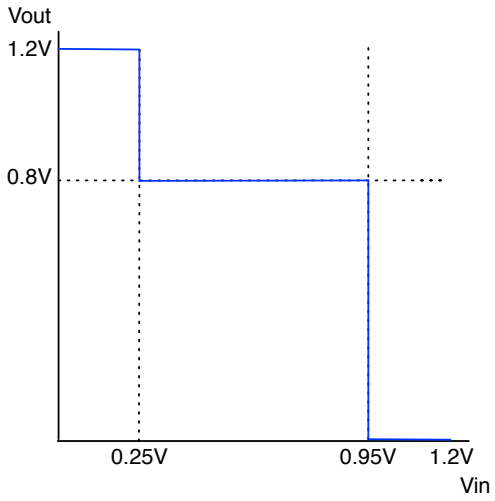


Figure 5: Inverter VTC from simple switch model

4 Sizing a chain of gates (Problems 3,4,6,&7)

4.1 Problem

Here is an old exam question I wrote. It's quite tough, but let's try to walk through it. For this problem, assume you have a reference inverter with Wp $= 2\mu$m, Wn $= 1\mu$m, and $t_{p,inv} = 32$ps. This technology has $\gamma = 2$. Optimally size the following chain for minimum delay. The solution is shown below, so don't view it until you've tried it yourself!

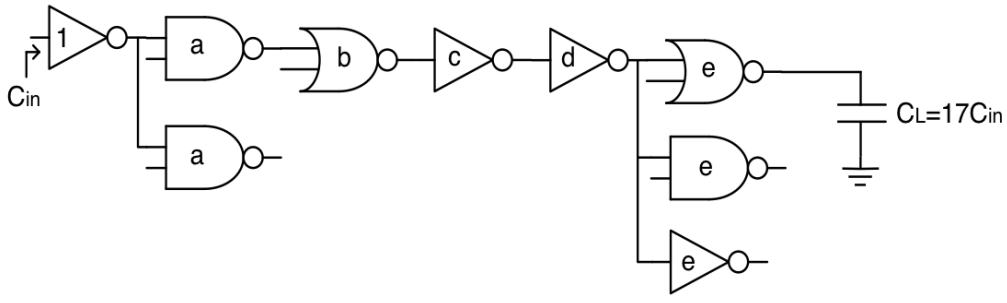
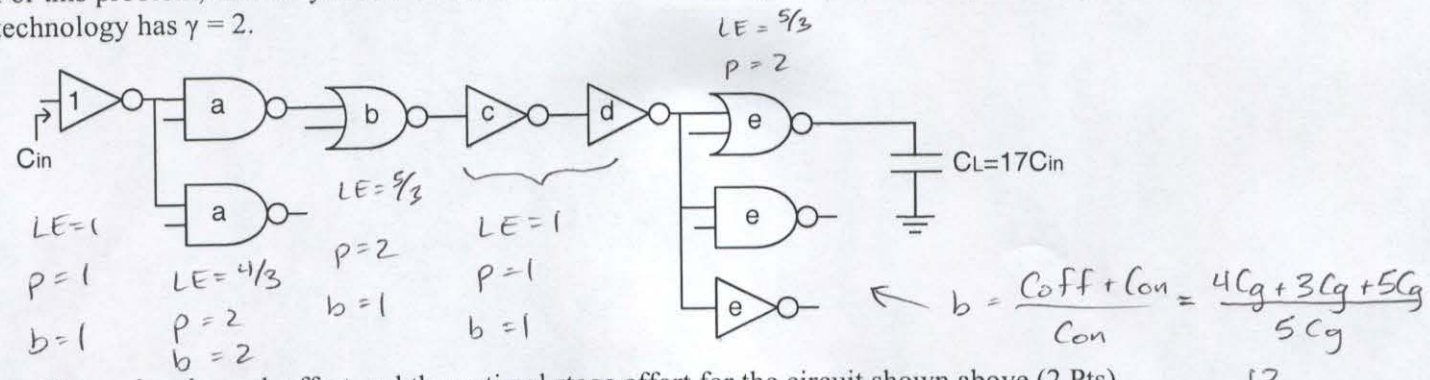


Figure 6

[PROBLEM 1] Logical Effort (12 Pts)

For this problem, assume you have a reference inverter with Wp = 2μm, Wn = 1μm, and $t_{p,inv}$ = 32ps. This technology has γ = 2.



$b = \frac{C_{off} + C_{on}}{C_{on}} = \frac{4C_g + 3C_g + 5C_g}{5C_g} = \frac{12}{5}$

a. Determine the path effort and the optimal stage effort for the circuit shown above (2 Pts)

$F = \frac{C_L}{C_{in}} = 17$

$SE_{opt} = \sqrt[N]{PE} = \sqrt[6]{302} = 2.59$

$\Pi B = 2 \times \frac{12}{5} = \frac{24}{5}$

$\Pi LE = \frac{4}{3} \times \frac{5}{3} \times \frac{5}{3} = \frac{100}{27}$

$PE = F \Pi B \Pi LE = 302.22$

PE = 302.22
SE_{opt} = 2.59

b. Optimally size each stage in the critical path for minimum delay. Give your results in terms of Cin. (3 Pts)

$C_{in,e} = C_L \times \frac{LE_e}{SE_{opt}} = 17 \times \frac{5}{3} \times \frac{1}{2.59} \times C_{in} = 10.94\, C_{in}$

$C_{in,d} = C_{in,e} \times b_e \times \frac{LE_d}{SE_{opt}} = 10.94 \times \frac{12}{5} \times 1 \times \frac{1}{2.59} \times C_{in} = 10.14\, C_{in}$

$C_{in,c} = C_{in,d} \times \frac{LE_c}{SE_{opt}} = 10.14 \times 1 \times \frac{1}{2.59} \times C_{in} = 3.91\, C_{in}$

$C_{in,b} = C_{in,c} \times \frac{LE_b}{SE_{opt}} = 3.91 \times \frac{5}{3} \times \frac{1}{2.59} \times C_{in} = 2.52\, C_{in}$

$C_{in,a} = C_{in,b} \times \frac{LE_a}{SE_{opt}} = 2.52 \times \frac{4}{3} \times \frac{1}{2.59} \times C_{in} = 1.30\, C_{in}$

$C_{in} = C_{in,a} \times b_A \times \frac{LE_1}{SE_{opt}} = 1.30 \times 2 \times 1 \times \frac{1}{2.59} \times C_{in} \approx C_{in}$ ✓

a = 1.30 Cin
b = 2.52 Cin
c = 3.91 Cin
d = 10.14 Cin
e = 10.94 Cin