

### Homework 8: Caches, FIFOs and Counters

Due: Friday Nov 7, 5pm

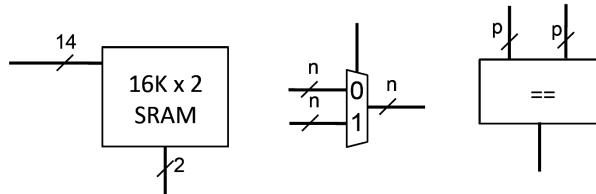
Please include your name, SID and specify either CS150, EE141 or EE241A at the top of your homework handin. Homeworks must be submitted electronically.

1. Suppose you are given a collection of configurable 16Kbit memory blocks. Each block can be configured as a 16K X 1, or a 8K X 2, ..., 512 X 32.

However, your design requires a large memory that is 2K X 32. Which collection of smaller memory blocks would you choose and why? Show a block diagram of how you would build the large memory from the smaller memory blocks, with the necessary address, Din and Dout ports.

2. Assuming we have a 32-bit address space, use the components shown in the diagram below and a small number of two input gates to construct the datapath for a 512KB 4-way set-associative cache. Each cache line is 2 words and each word is 4 bytes. Your cache should include tag storage, data storage, address comparison, data output selection and any other parts you feel are relevant.

Note that the input memory address are byte-, not word-, indexed. However, you do not need to be concerned about the addressing of a byte within a word (i.e. you can assume that all input memory addresses will fall on a word-boundary).

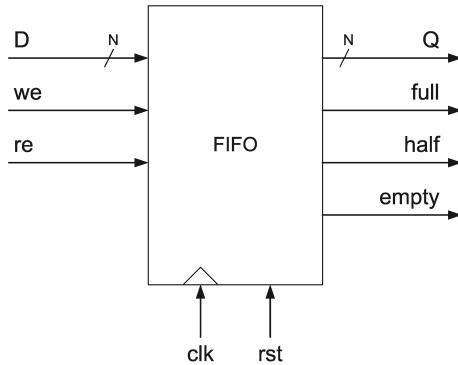


3. Suppose you are running a program with the following data access pattern. The pattern is executed only once.

0x0, 0x8, 0x10, 0x18, 0x20, 0x28

- If you use a direct mapped cache with a cache size of 1 KB and a block size of 8 bytes (2 words), how many sets are in the cache?
- With the same cache and block size as in part (a), what is the miss rate of the direct mapped cache for the given memory access pattern?

- (c) For the given memory access pattern, which one of the following would decrease the miss rate the most (while cache capacity is kept constant)? Explain why.
- Increasing the degree of associativity to 2.
  - Increasing the block size to 16 bytes.
  - Both (i) and (ii) decrease miss rate by the same amount.
  - Both (i) and (ii) have no effect, or make the miss rate worse.
4. Design a 2-entry N-bit wide FIFO circuit. The circuit has interface signals as shown below. The operation is controlled by the **we** and **re** signals. The three outputs **empty**, **half**, and **full**, indicate whether the FIFO is empty, half-full or full, respectively. A read operation when the FIFO is empty results in all zeros on the output. A write operation when the FIFO is full results in no operation. The **rst** signal is a synchronous control that results in the FIFO being empty.



Your design should take the form of a data-path and a FSM-based controller. Using flip-flops, simple logic-gates and multiplexors, draw the datapath part of your design. Clearly label all input, output and control signals (with names of your choice). Use hierarchy.

5. (a) Design a 4-bit synchronous down counter which counts in 2's complement representation, using simple gates and flip flops. Your counter should have a **CE** (count enable) signal and when it reaches the minimum number, it wraps around and start from the maximum number again. Show the steps you have taken to derive the circuit(truth table for next state logic, simplification of the equations, etc).
- (b) How would you generalize your design to N-bits?
6. **For EE241A only:** The JK flip-flop is one of the most universal flip-flops. It has 3 inputs,  $J$ ,  $K$  and  $clk$ , and two outputs,  $Q$  and  $\bar{Q}$ . The output  $Q$  changes on the rising clock edge, following the rules on the next page.

Design a counter which cycles through the sequence (1,2,4,5,6,7), in binary, using J/K flip-flops. Show that when states 000 and 011 are used as don't care statements, the counter may not operate properly. Suggest how to correct this problem.

| J | K | Q  |
|---|---|--|
| 1 | 0 | 1  |
| 0 | 1 | 0  |
| 0 | 0 | Unchanged                                |
| 1 | 1 | $\overline{Q}$ (i.e. the output toggles) |