University of California at Berkeley
Department of Electrical Engineering and Computer Science

EECS150/EE141/EE241A, Fall 2014

Homework 5: Wires and Energy

Due: Friday Oct 10, 5pm

Please include your name, SID and specify either CS150, EE141 or EE241A at the top of your homework handin. Homeworks must be submitted electronically as a signle file in PDF format.

Problem 1: Elmore delay calculation

For the following problem, $C_G = C_D = 2fF/\mu m$, a 1x inverter is sized $2\mu m/1\mu m$ with $R_{n,on} = 1k\Omega/\mu m$, $R_{p,on} = 2k\Omega/\mu m$,$R_{wire} = 0.1\frac{\Omega}{\square}$, $C_{pp} = 20aF/\mu m^2$, $C_{fr} = 14aF/\mu m$.

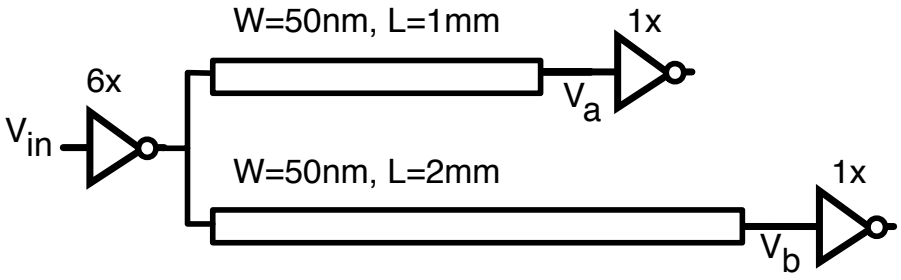

Figure 1

a) Using the π wire model, draw the equivalent RC switch model. What is the propogation delay from a step at V_{in} to V_a and V_b?

b) What is the skew (difference in arrival time at V_a and V_b)?

c) What is the skew relative to the longest path? If the supply voltage is decreased, will the relative skew increase or decrease? Why?

Problem 2: Power and Leakage

Consider an 3-input NOR gate shown in Figure 2 with Vdd=1V, $C_L = 5fF$, $C_D = 2fF/um$, $I_{ON,N} = 600\mu A/\mu m$, $I_{ON,P} = 300\mu A/\mu m$, $I_{OFF,N} = 80nA/\mu m$, $I_{OFF,P} = 50nA/\mu m$, $W_N = 1\mu m$, and $W_P = 2\mu m$.

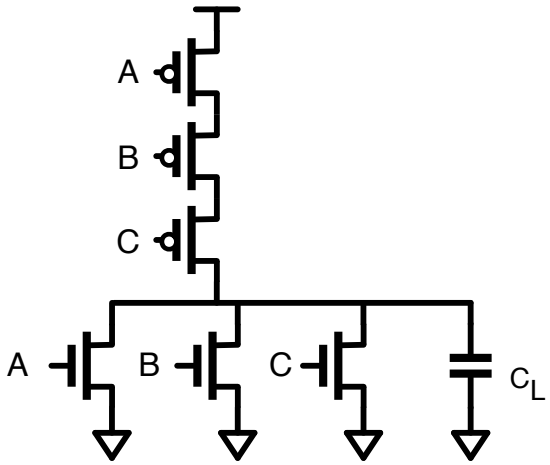

Figure 2

a) Assume that the probability of an input being high is 0.5, and that all inputs are independent. What is the probability that the output is high? What is the probability that the output is low?

b) Under the same assumptions as (a), what is the gate activity factor (i.e. the probability that the output will transition from low to high, $P_{0->1}$)?

c) What is the dynamic power dissipation of the gate if the clock frequency is 3GHz?

d) What inputs would cause the highest leakage? The lowest leakage?

Problem 3: Energy

For Figure 3, $C_1 = C_2 = 100fF$, transistor capacitance is negligable, Vdd=1V, and $V_{TN} = |V_{TP}| = 0.4$.

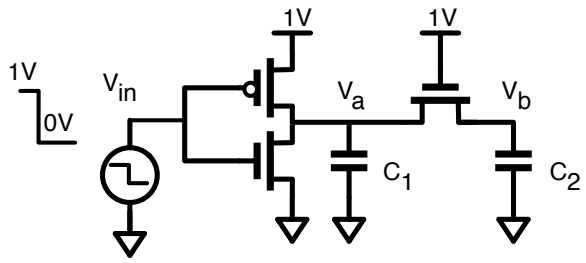

Figure 3

a) How much energy is drawn from the supply for a 1V to 0V step on the input ?

b) How much energy is stored on the capacitors after the voltage step?

c) Where did the energy go?

d) If this "gate" toggled 1 million times in 2 seconds, what would the average power of the gate be?

Problem 4: Short-circuit current

Recall the definition of the response of an RC circuit driven by an ideal voltage pulse in Figure 4 and Equation 1.

$$V_{out}(t) = V_{in}(1 - e^{-\frac{t}{RC}}) \tag{1}$$

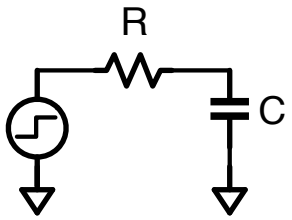

Figure 4: Simple RC circuit corresponding to Equation 1.

a) How much time (in terms of RC) will it take for V_{out} to rise to 50% of V_{in}? (solve for t)

b) How much time will it take for V_{out} to rise to 10% of V_{in}?

c) How much time will it take for V_{out} to rise to 90% of V_{in}?

d) What is the rise time (10 to 90%)?

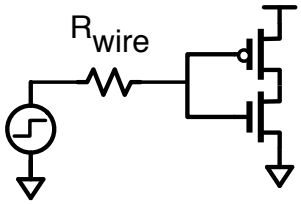

Figure 5: Inverter driven through a wire.

For the inverter shown in Figure 5, assume that the transistors have $R_{on} = 1k\Omega$, $V_{TN} = |V_{TP}| = 0.4$, $C_{in} = 10fF$, $R_{wire} = 1k\Omega$ and Vdd=1V. Use the switch model of the inverter.

e) For a 1V input step, for how long are both transistors on at the same time?

f) What is the short-circuit power?

g) How much short-circuit energy is dissipated?

Problem 5 (EE241A Only): Voltage scaling

To gain intuition about voltage scaling, it is important to estimate delay and energy as a function of voltage. The Alpha Power Law model of a transistor's current can estimate delay over a wide voltage range (Equation 2). Additionally, delay can be approximated by modeling transistors as constant current source for the V_{DD} to $V_{DD}/2$ transition (Equation 3). Use these model with $\alpha = 1.3$, $V_T = 0.3V$, and $V_{DD} = 1V$ to answer the following questions about voltage scaling.

$$I \propto (V_{DD} - V_T)^{\alpha} \tag{2}$$

$$t_d \propto \frac{C(V_{DD}/2)}{I} \tag{3}$$

a) Plot V_{DD} vs. delay, V_{DD} vs. power-delay product (PDP), and V_{DD} vs. energy-delay product (EDP) when considering dynamic energy only for $0.35V < V_{DD} < 1V$. At what V_{DD} is minimal energy obtained?

b) Now consider power as a combination of switching energy, activity, and leakage power ($P = C{\cdot}V_{DD}^2{\cdot}a{\cdot}f + V_{DD}{\cdot}I_{leak}$) Assume at 1V, the design runs at 1Ghz, $C = 1nF$, and $I_{leak} = 100mA$ Plot energy per cycle vs. V_{DD} for activity factor $a = 0.1, 0.2$. The frequency at each Vdd is equal to t_d times a constant that makes the frequency at 1V be 1GHz. Is voltage scaling more or less effective for high activity factors?