Discussion #5

10/3/2014 and 10/6/2014

Review

- Week 1: Intro: EE141 vs. CS150
- Week 2: RTL (Verilog)
- Week 3: Sequential+Combinational, Boolean
- Week 4: Finite State Machines
- Week 5: CMOS + hand models
- **Week 6: Wires + power/energy**

For example

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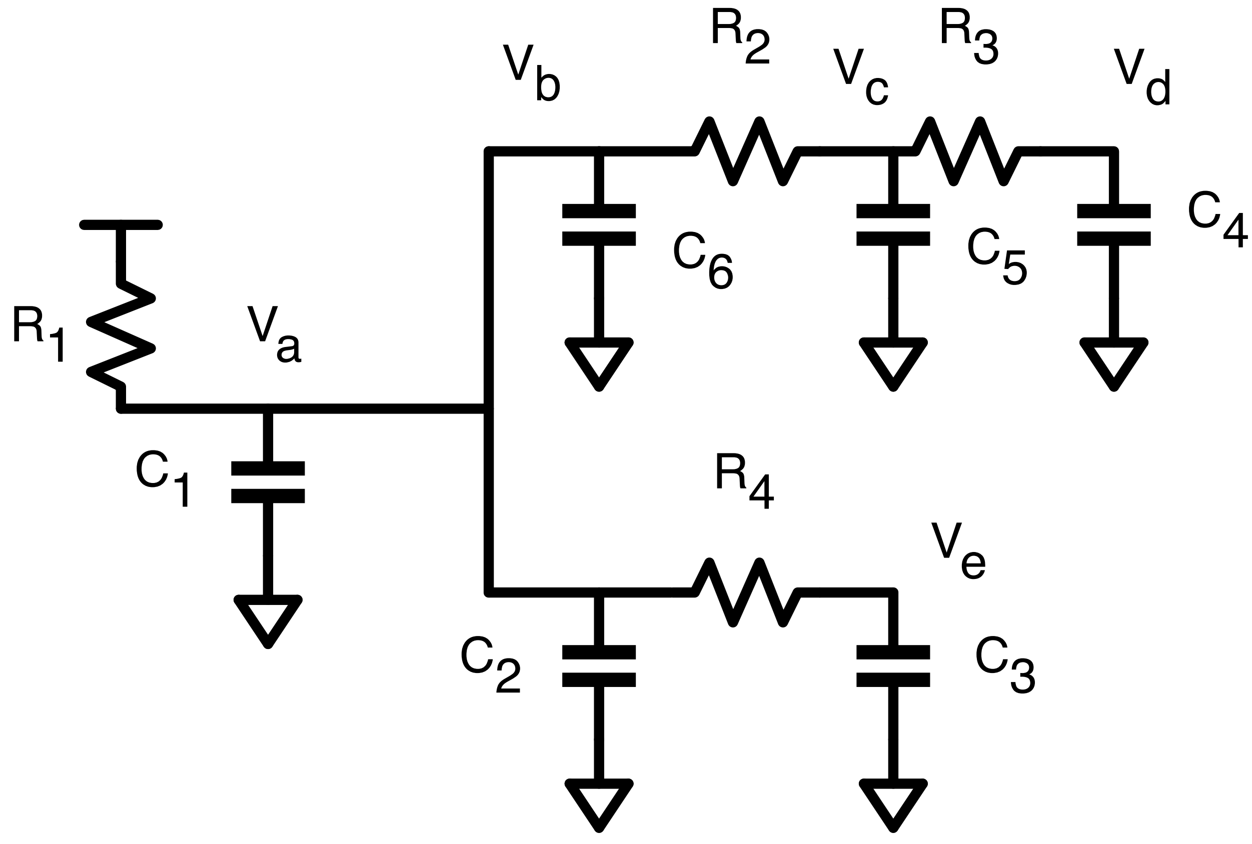
- Design a chip that detects the sequence 3 or ore 1s in a row (out=1 if detected)
- **-> Draw FSM**
- **-> Describe in Verilog (Mealy vs. Moore?)**
- **-> Write table (current state/input | next state/output)**
- **-> Next state logic/K-map**
- **-> Implement at gate-level**
- **-> Gate-level timing**
- **-> Transistor-level timing**

- **-> How would you do this in lab?**

Practice problem

- Elmore delay

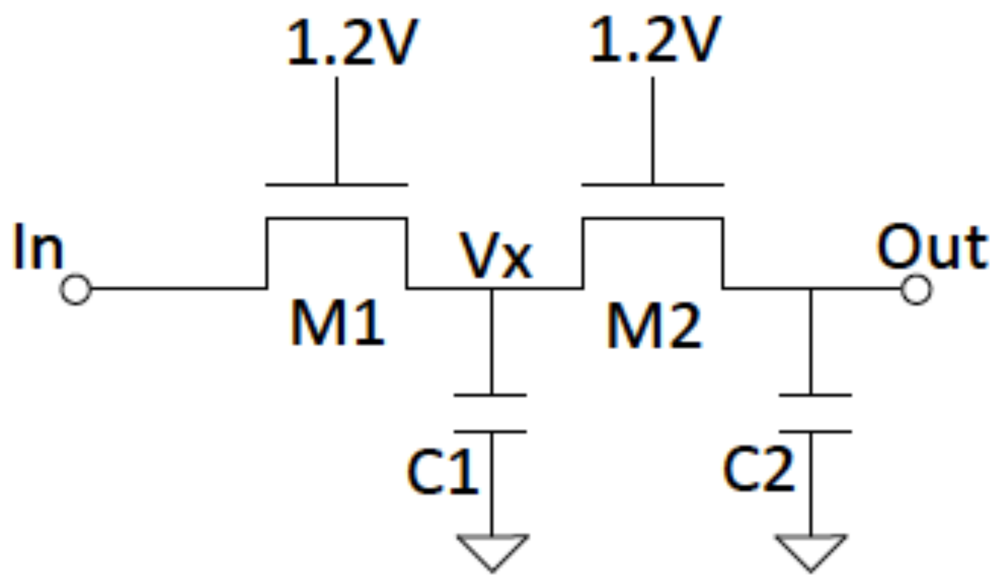


Answer

- Short any resistor not on the desired path:
- Va to Vd: tau = R1(C1+C2+C3+C6) + (R1+R2)(C5) + (R1+R2+R3)(C4)
- Then delay is 0.69tau

Practice Problem

- Energy: Energy when input 0->1.2



For this problem, you can assume an ideal pulse at the input and $C_1 = C_2 = 50fF$. Ignore leakage and device capacitance. The nominal supply voltage is 1.2V, $V_{TH} = V_{TH,N} = |V_{TH,P}| = 0.2V$ and $R_{ON,N} = R_{ON,P} = R$.

Answer

Source is always the lower potential (for NMOS…or higher potential for PMOS)
NMOS can only pull up to Vdd-Vth
PMOS can only pull down to Vth

Both capacitors get charged from 0 to 1V. Note that the supply in this case is the input source. Therefore the total charge drawn from the supply is:

$$Q = C_1 \cdot \Delta V_1 + C_2 \cdot \Delta V_2 = 2C_1(V_{fin} - V_{init})$$

$$E_{0\to1} = Q \cdot V_{SUP} = 2C_1(V_{fin} - V_{init})V_{SUP} = 2 \cdot 50\,fF \cdot 1V \cdot 1.1V = 110\,fJ$$

$$E_{C1,stored} = E_{C2,stored} = \frac{1}{2}C_1 V_{out,fin}^2 = \frac{1}{2}50\,f(1V)^2 = 25\,fJ$$

$$E_{dis} = E_{0\to1} - E_{stored} = 110\,fJ - 25\,fJ - 25\,fJ = 60\,fJ$$