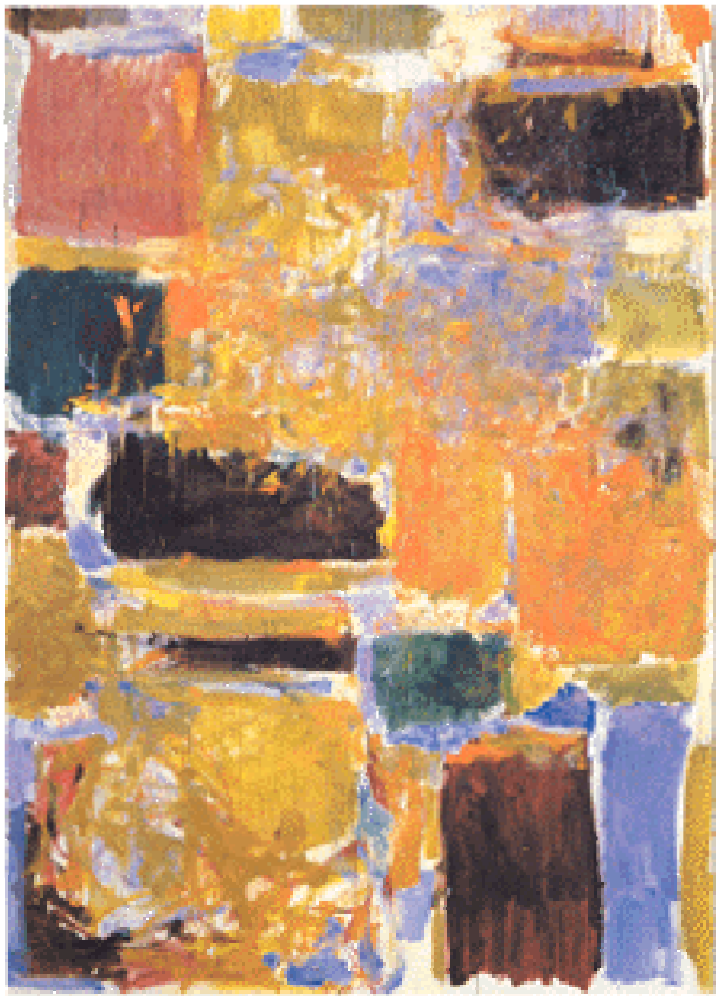
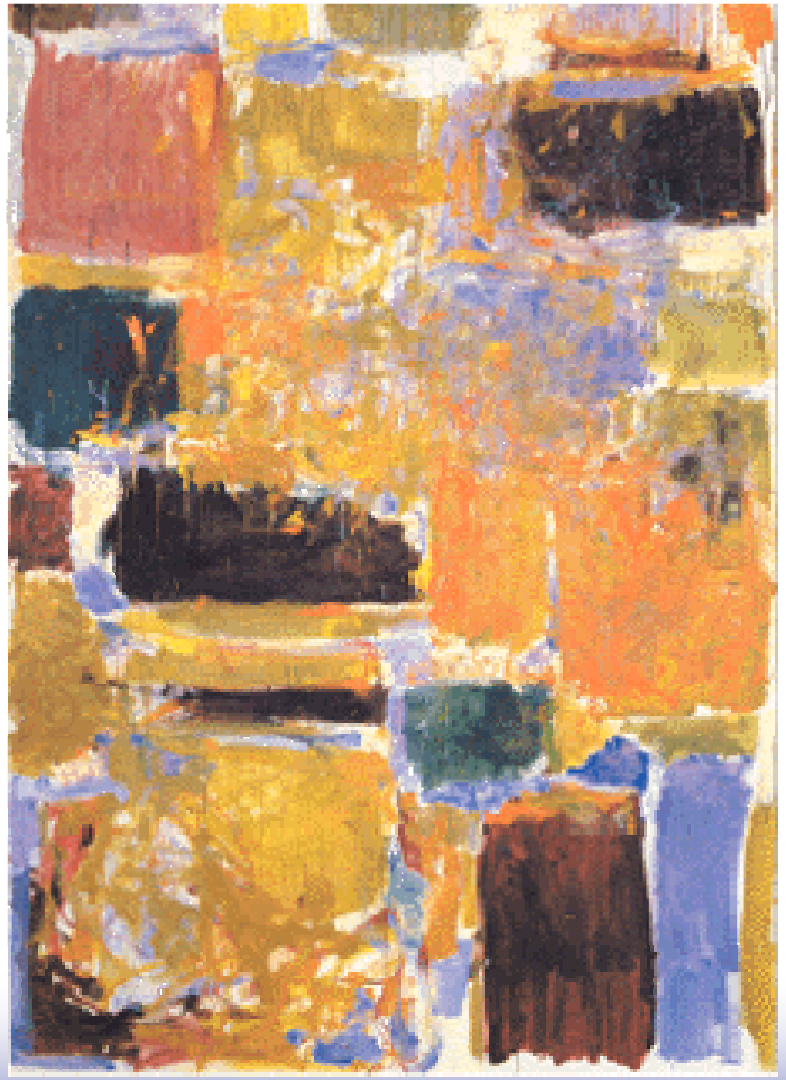


CS150 - EE141/241A
Fall 2014
Digital Design and Integrated Circuits

Instructors:
John Wawrzynek and Vladimir Stojanovic

Lecture 12

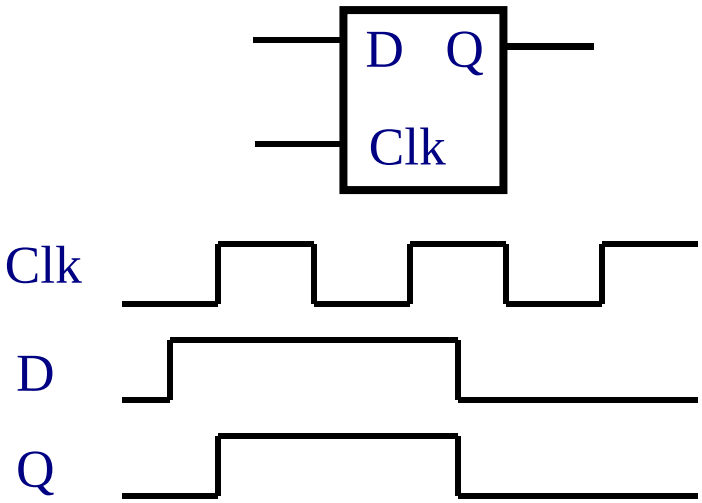
Outline



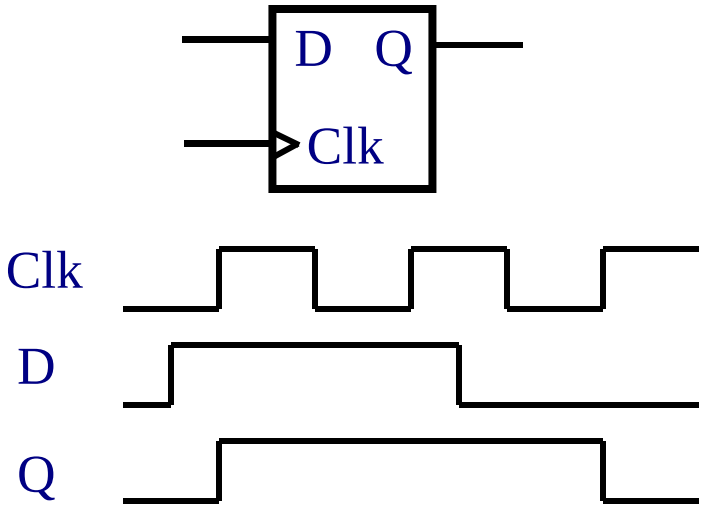
- Latch Design
- Register Design
- Setup, Hold and Clk-Q
- Race conditions

Latch versus Register (Flip-flop)

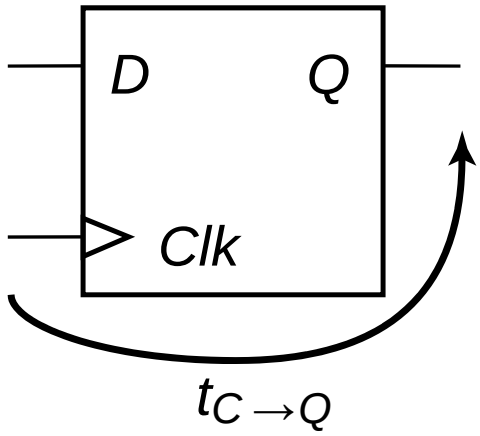
- Latch: level-sensitive
  clock is low - hold mode
  clock is high - transparent



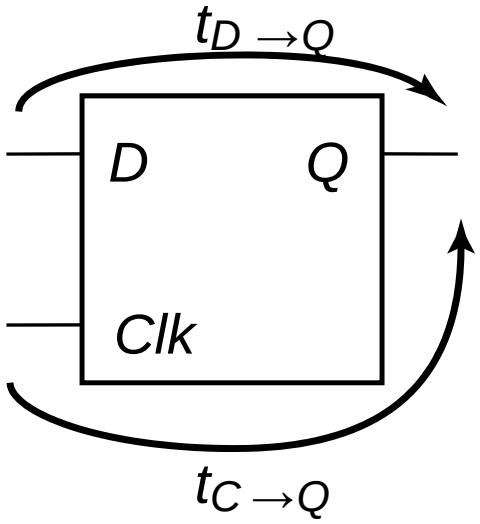
- Register: edge-triggered
  stores data when
  clock rises



Characterizing Timing

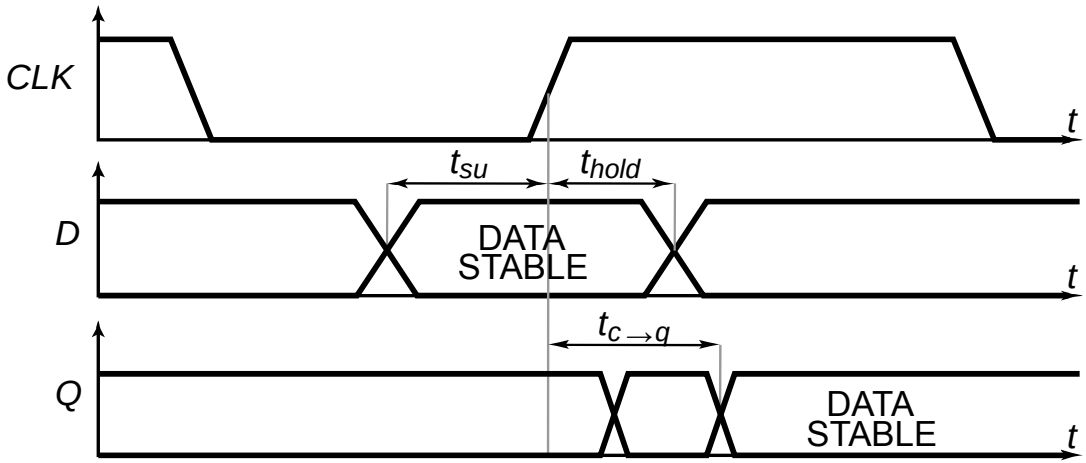


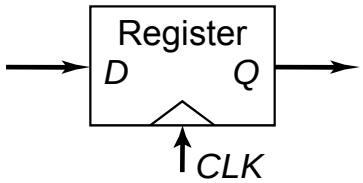
Register

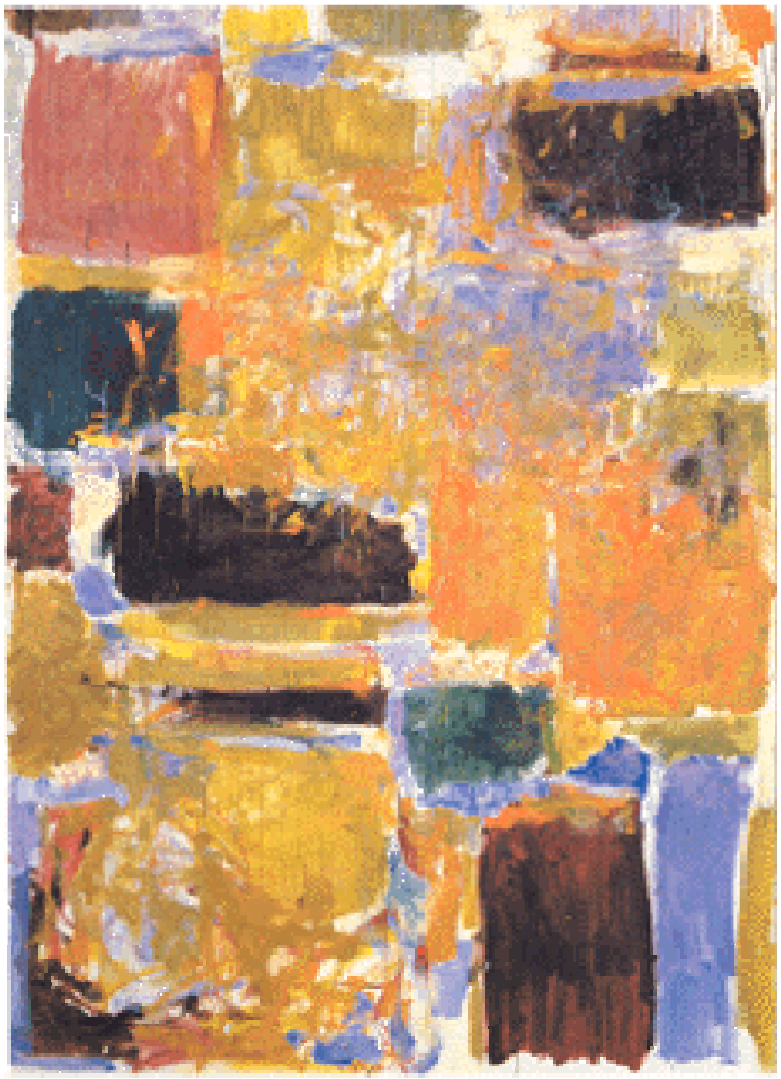


Latch

Timing Definitions – Set-up and Hold Times



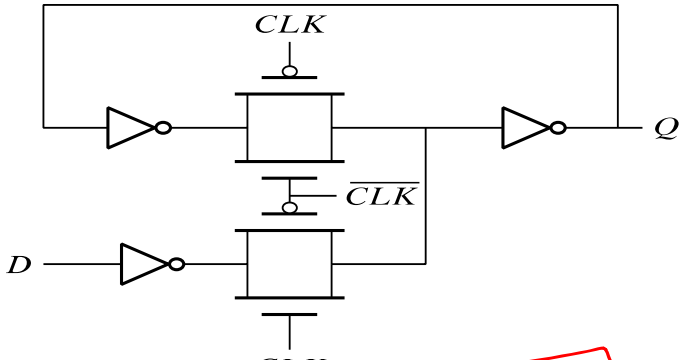




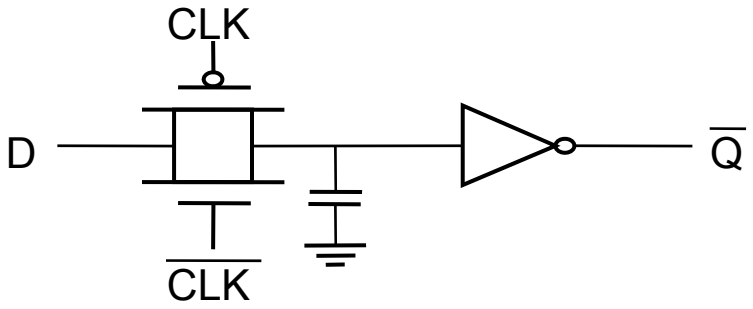
Latch Design

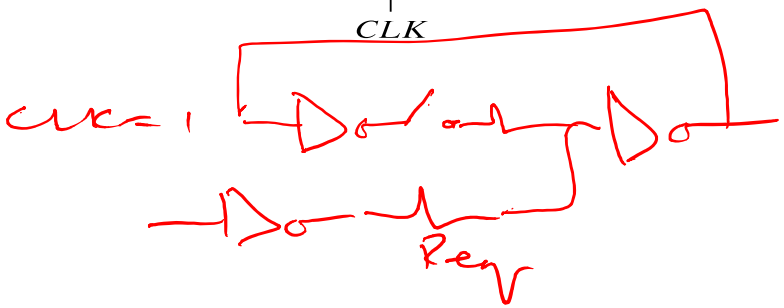
Storage Mechanisms

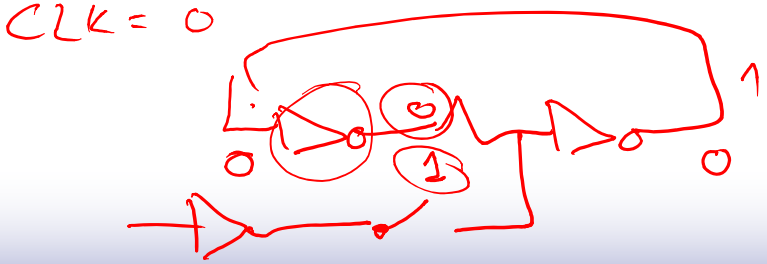
Static



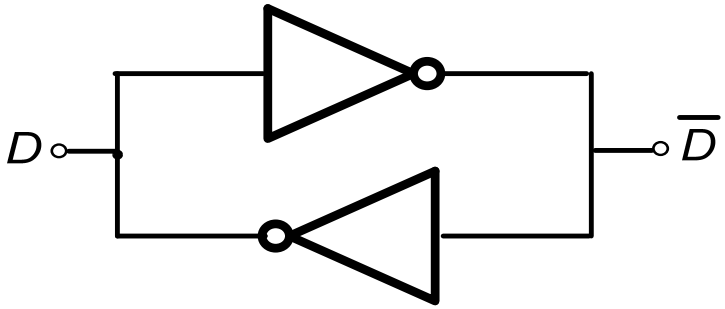
Dynamic





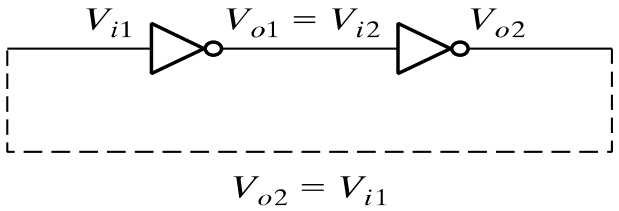


Basic Static Storage Element

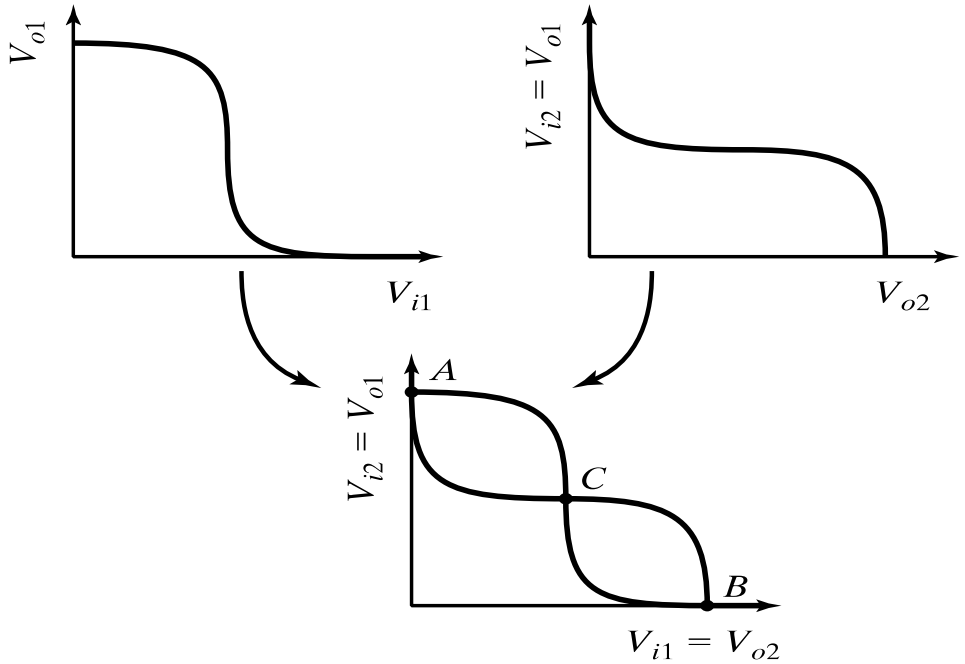


- If D is high, D_b will be driven low
  - Which makes D stay high
- Positive feedback

Positive Feedback: Bi-Stability

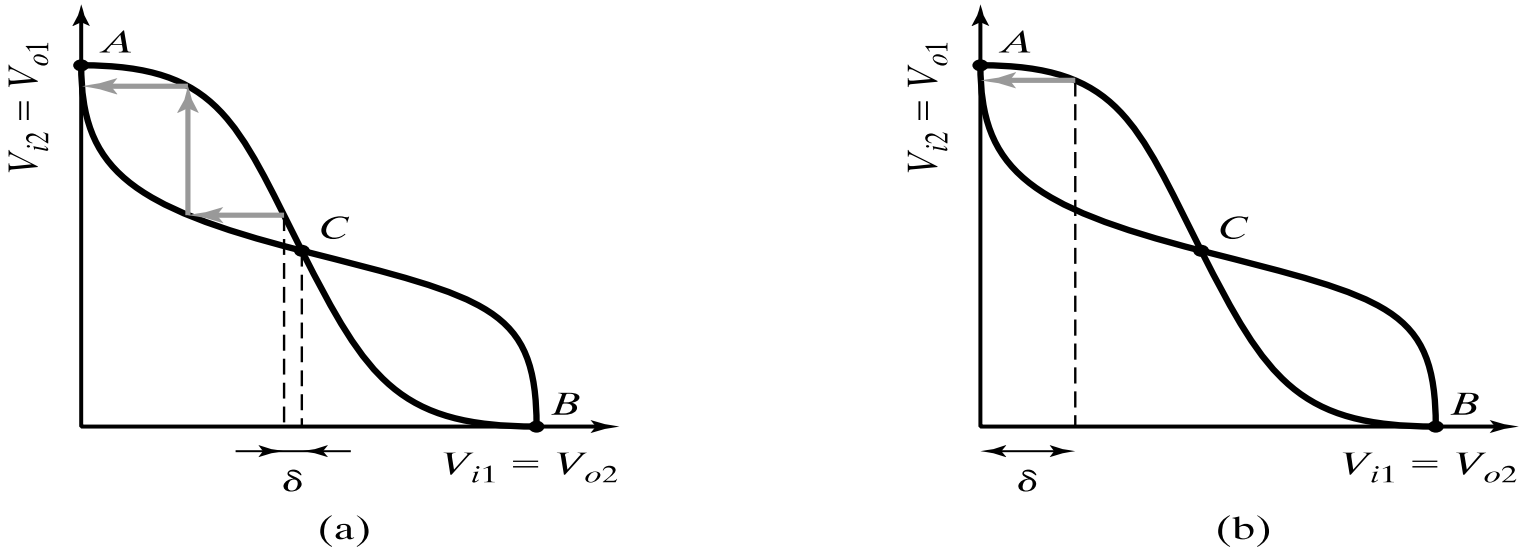


(a)



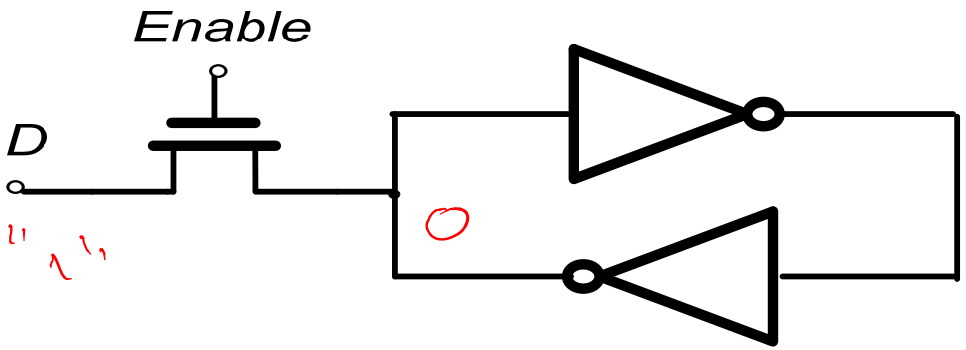
(b)

Meta-Stability



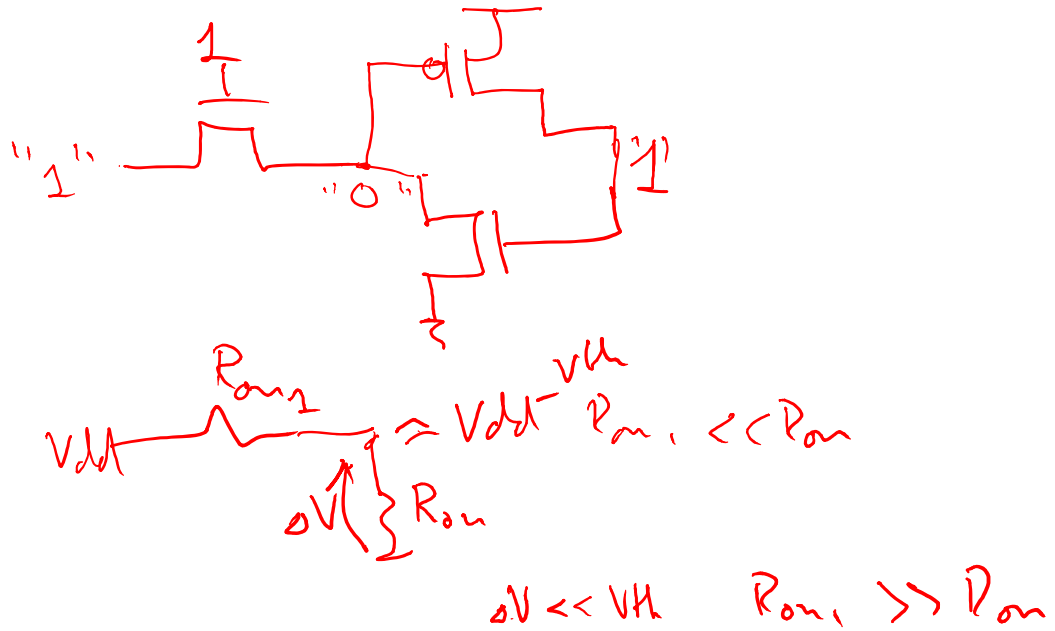
Gain should be larger than 1 in the transition region

The Static Latch



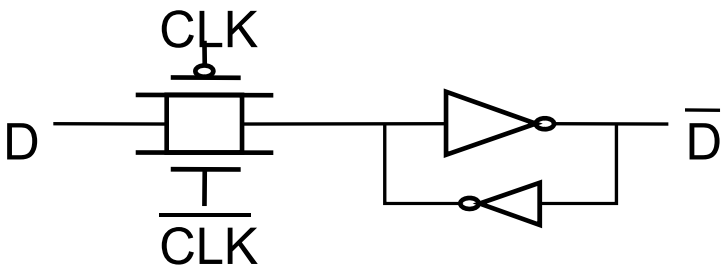
Access transistor must be able to overpower the feedback

Writing a "1"

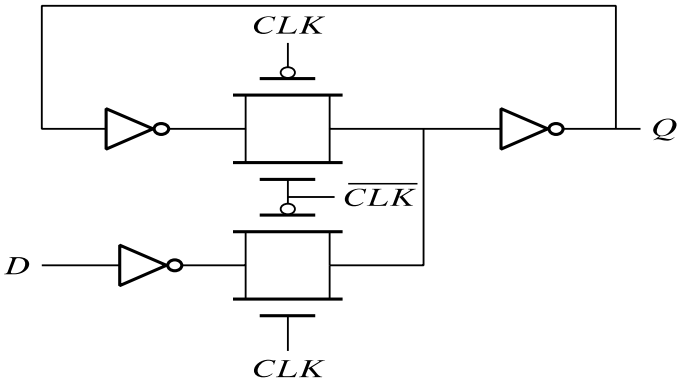

1
0
"1"
"0"
"1"
$R_{on,1}$
V_{dd}
$\approx V_{dd}$
V_H
$R_{on,1} << R_{on}$
ΔV
R_{on}
$\Delta V << V_H$
$R_{on,1} >> R_{on}$

Addressing the write problem

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states



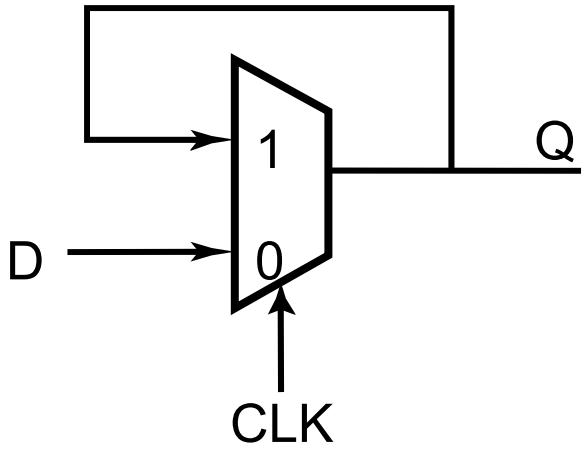
Forcing the state
(can implement as NMOS-only)



Converting into a MUX

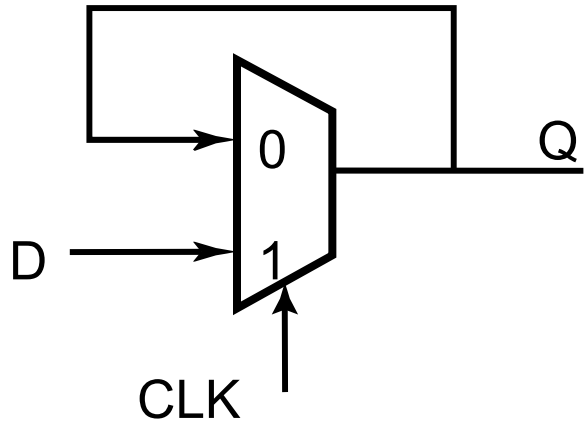
Mux-Based Latches (pseudo-static)

Negative latch
(transparent when CLK= 0)



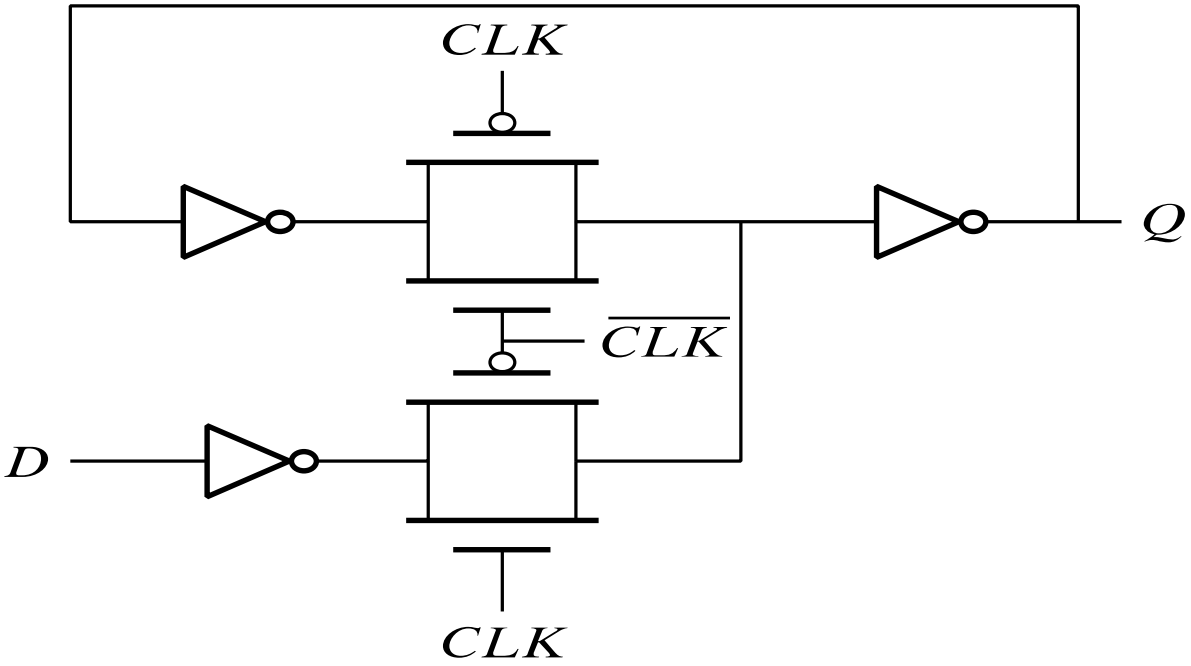
$$Q = Clk \cdot Q + \overline{Clk} \cdot D$$

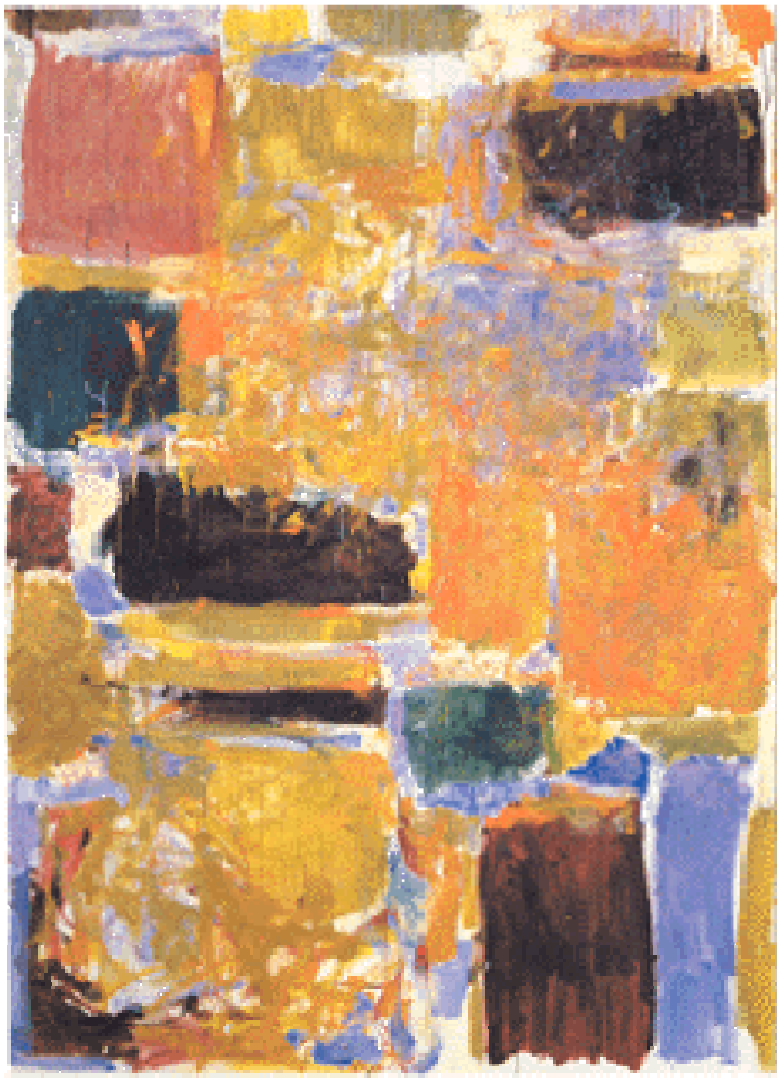
Positive latch
(transparent when CLK= 1)



$$Q = \overline{Clk} \cdot Q + Clk \cdot D$$

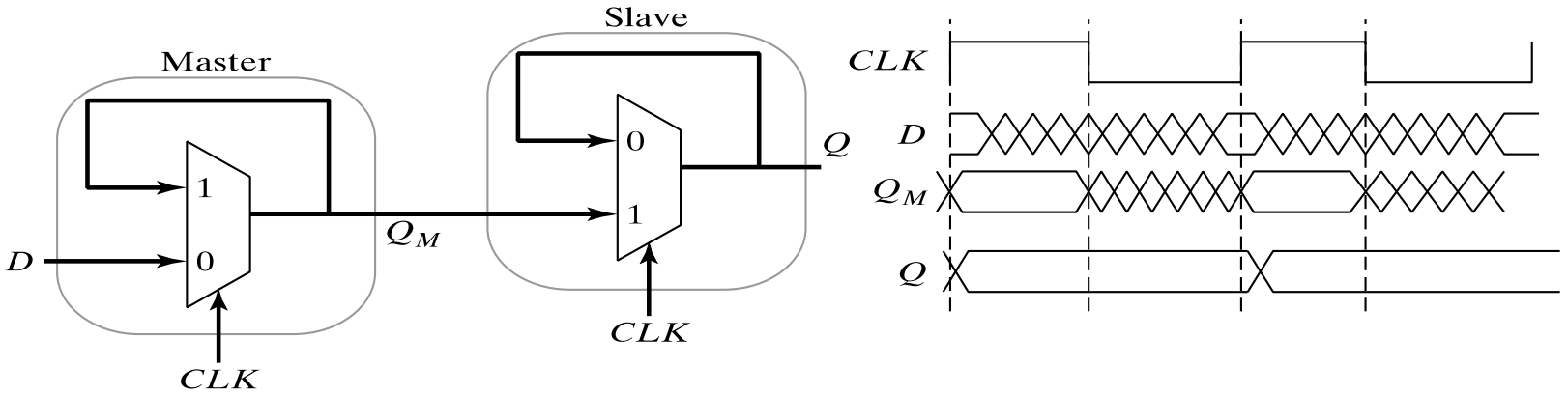
Mux-Based Latch





Register Design

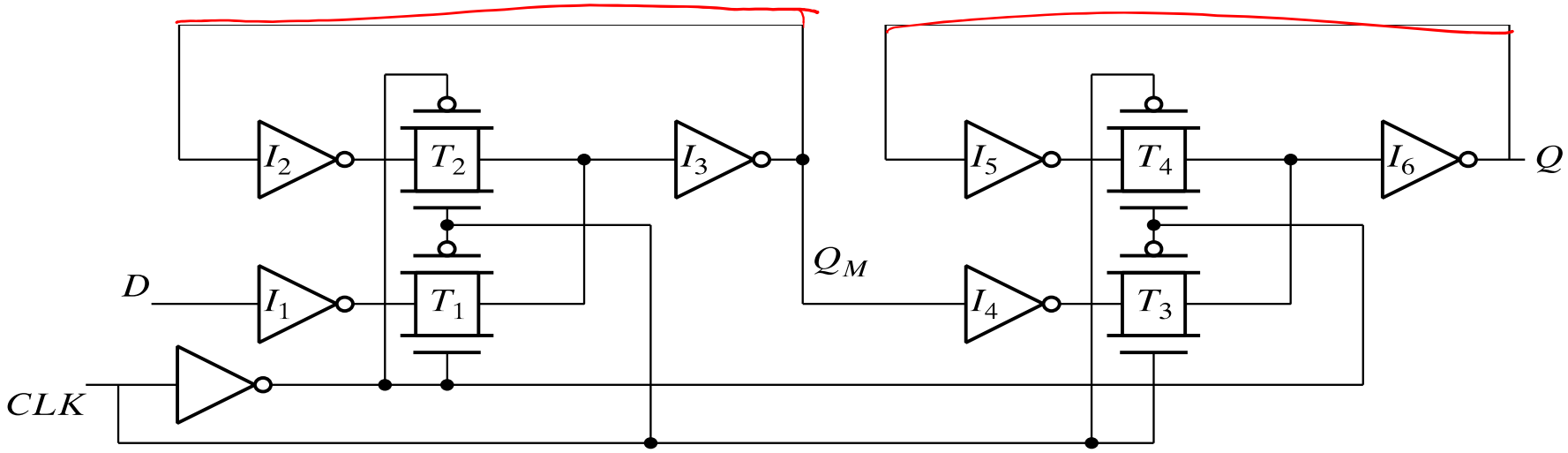
Master-Slave Register (Edge-Triggered)

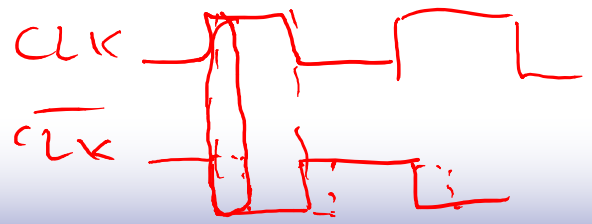


Two opposite latches trigger on edge
Also called master-slave latch pair

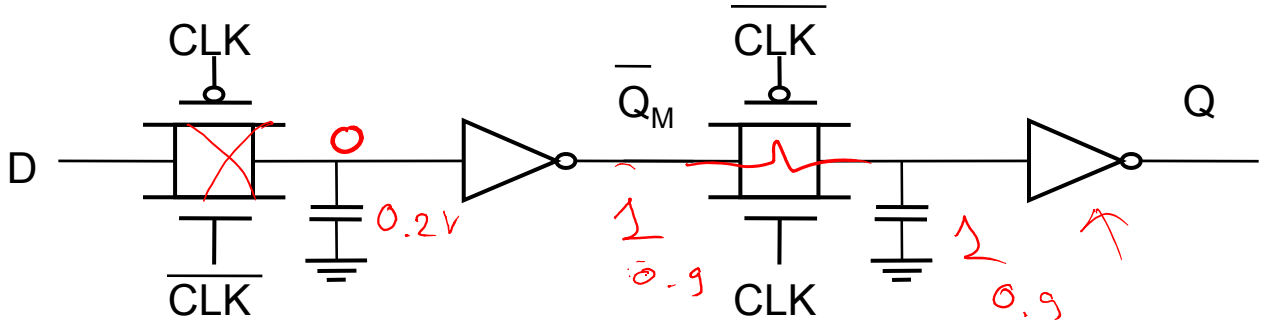
Master-Slave Register

Multiplexer-based latch pair

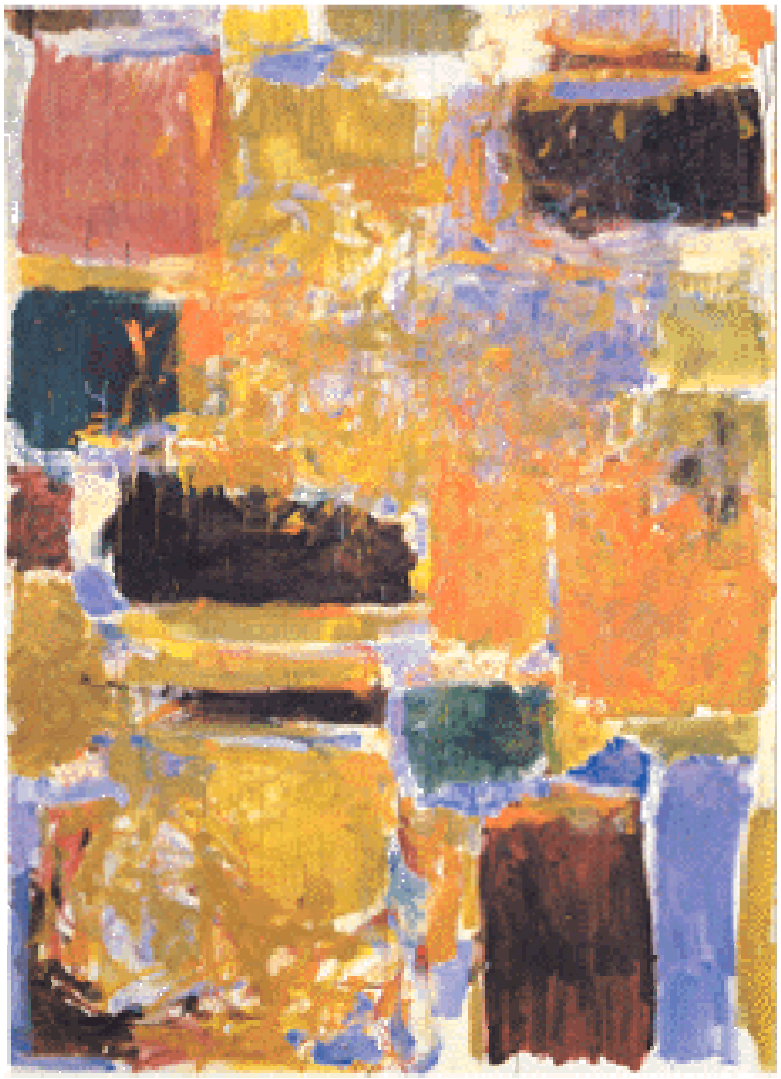




Pass-gate Dynamic MS Register

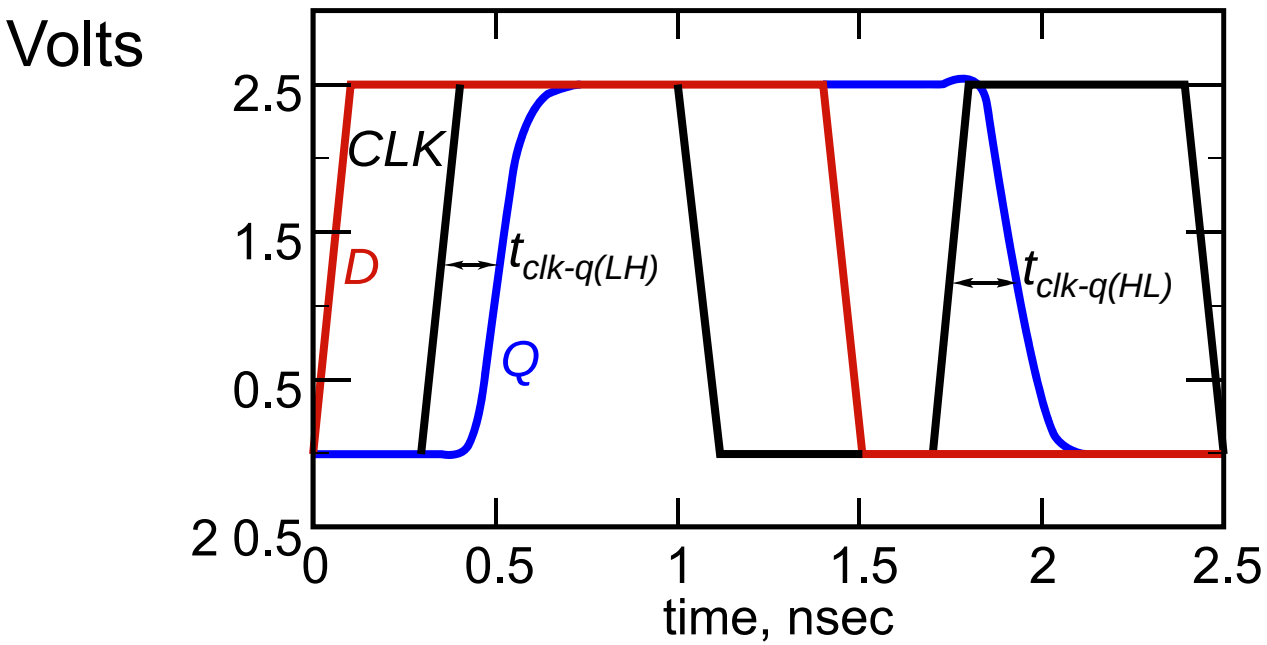


- State stored on caps – no feedback
- Faster than static, but risky due to leakage and coupling

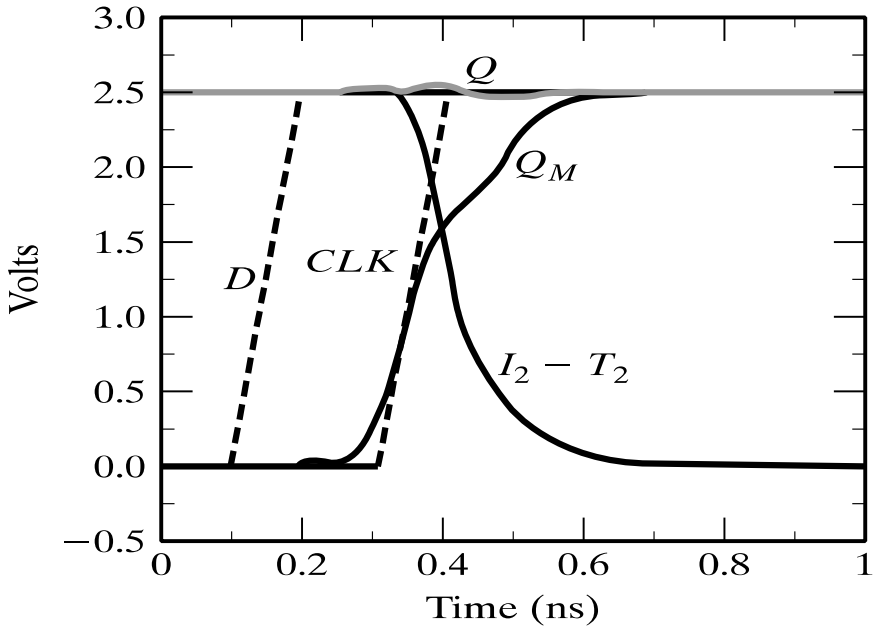


Setup, Hold, Clk-Q

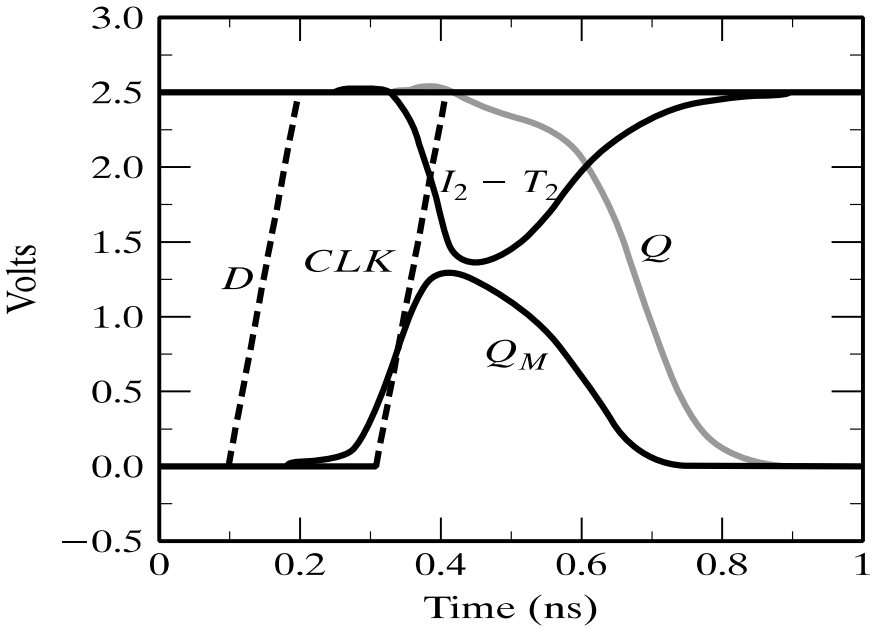
Clk-Q Delay


Volts
2.5
1.5
0.5
2 0.5
CLK
D
Q
$t_{clk\text{-}q(LH)}$
$t_{clk\text{-}q(HL)}$
0
0.5
1
1.5
2
2.5
time, nsec

Setup Time

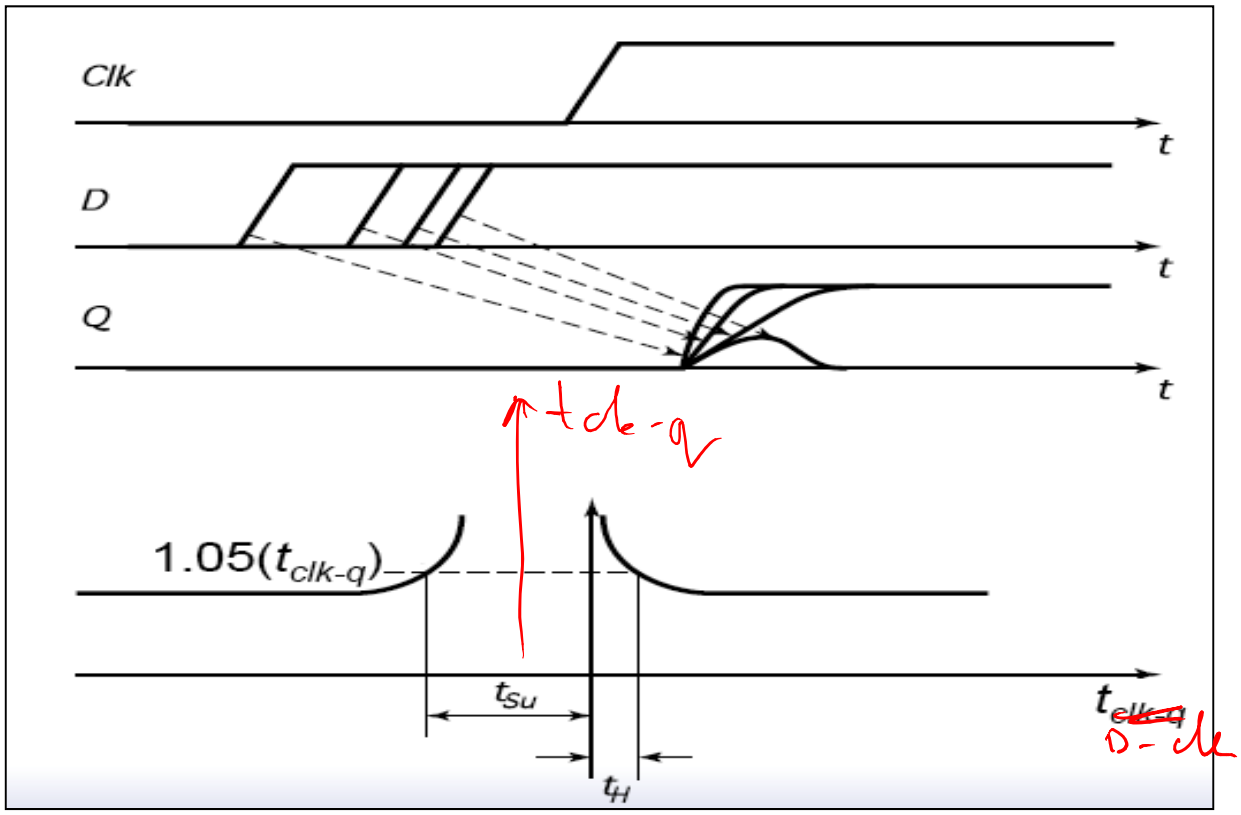


(a) $T_{setup} = 0.21$ ns



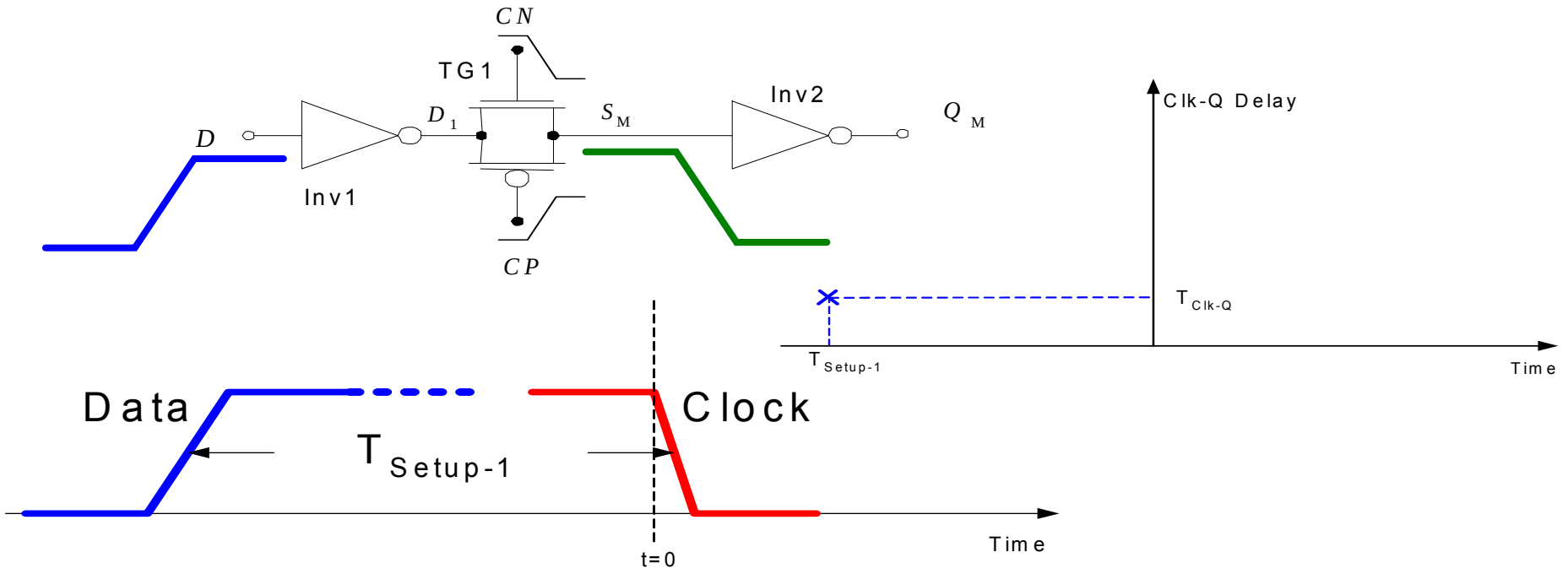
(b) $T_{setup} = 0.20$ ns

More Precise Setup Time



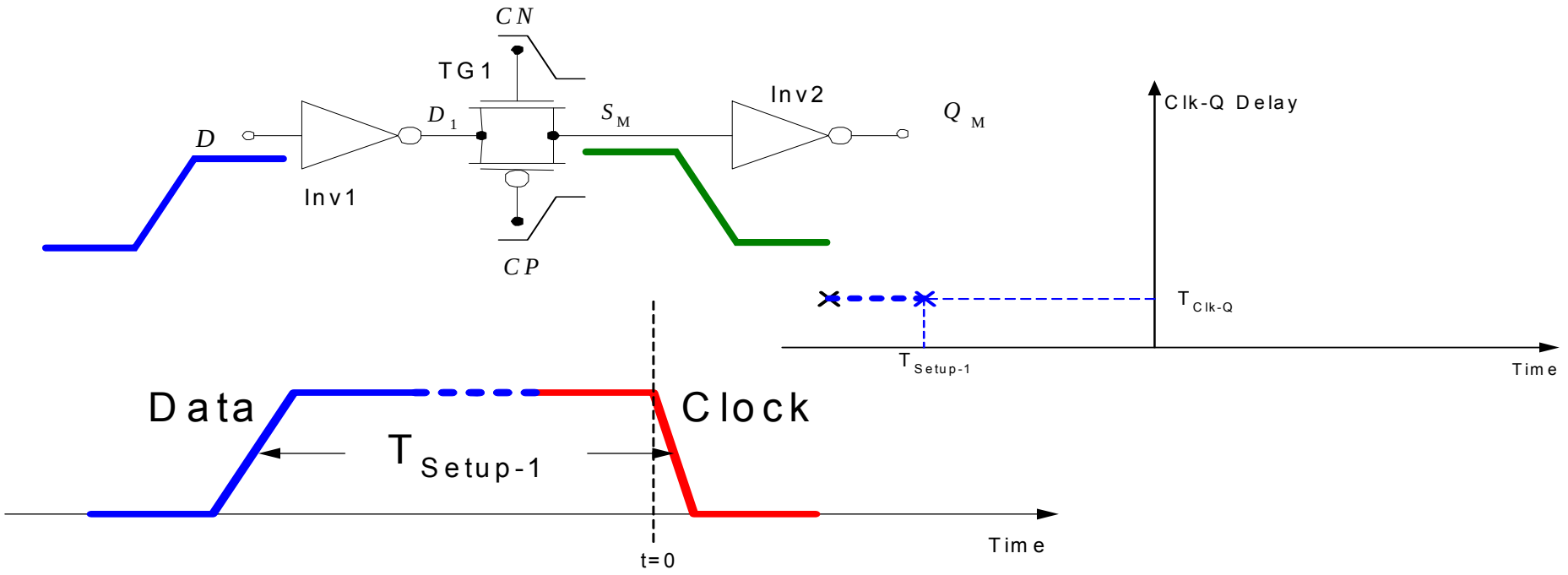
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



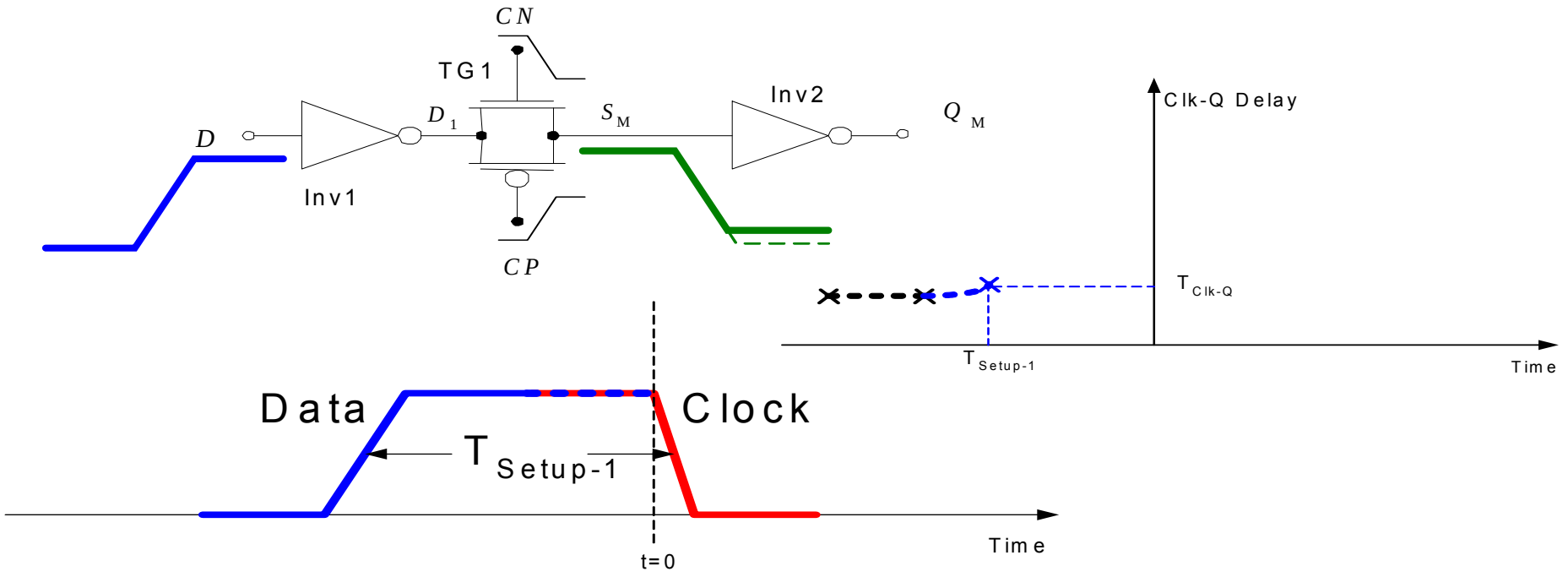
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



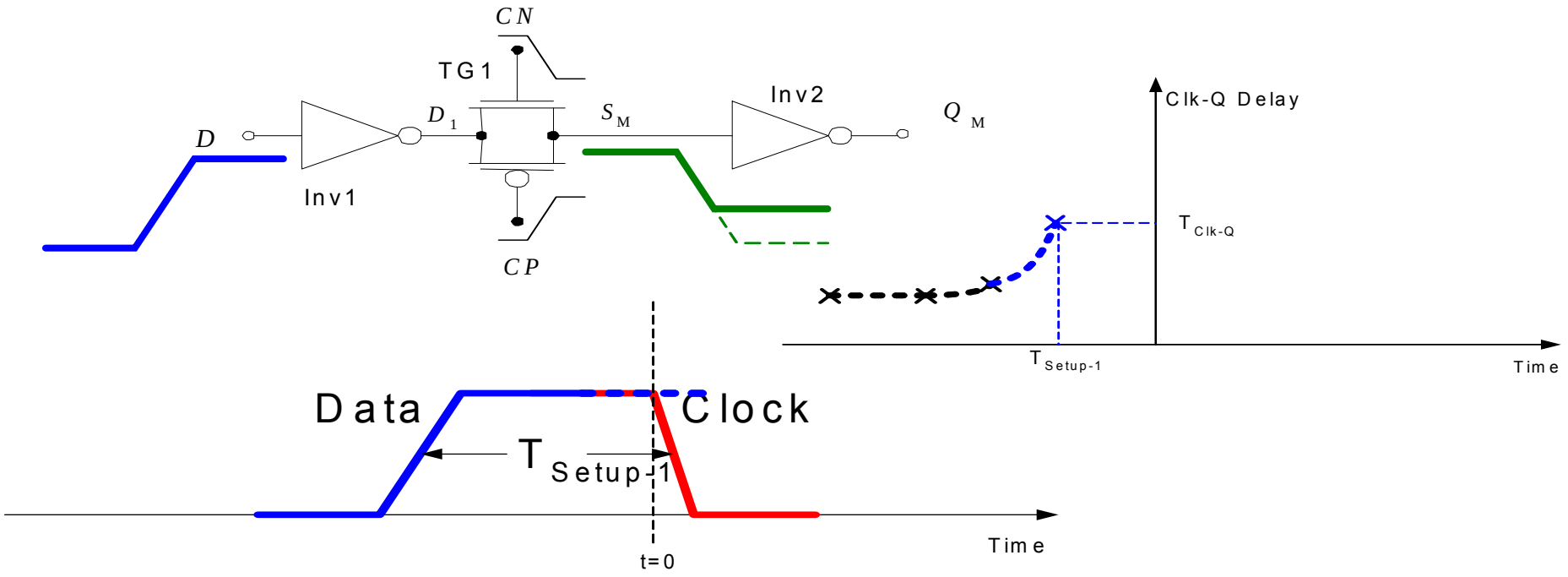
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



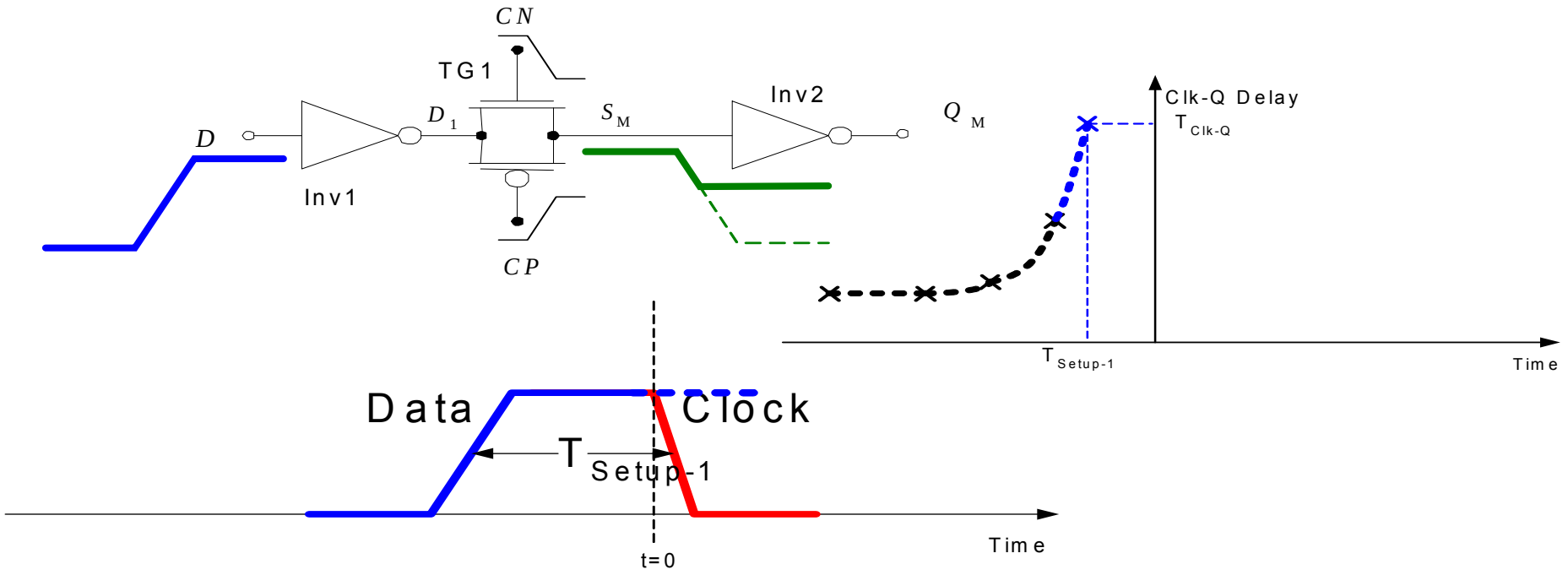
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



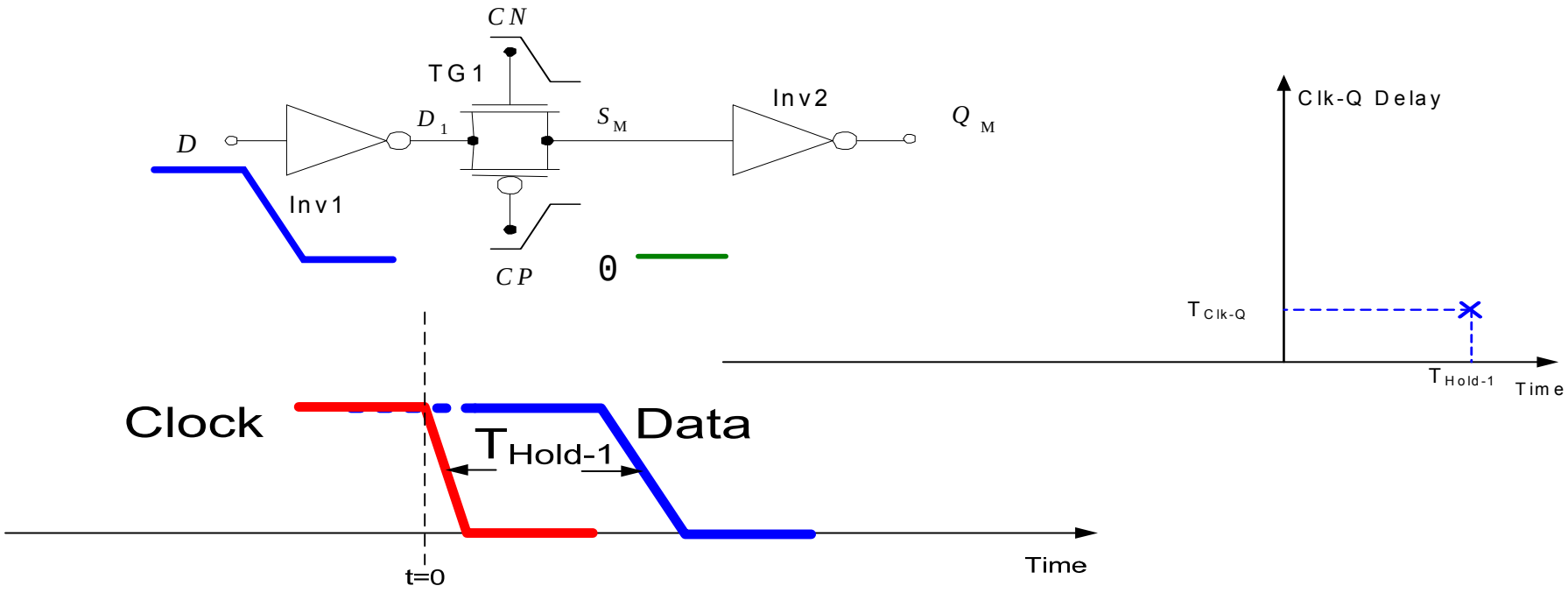
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



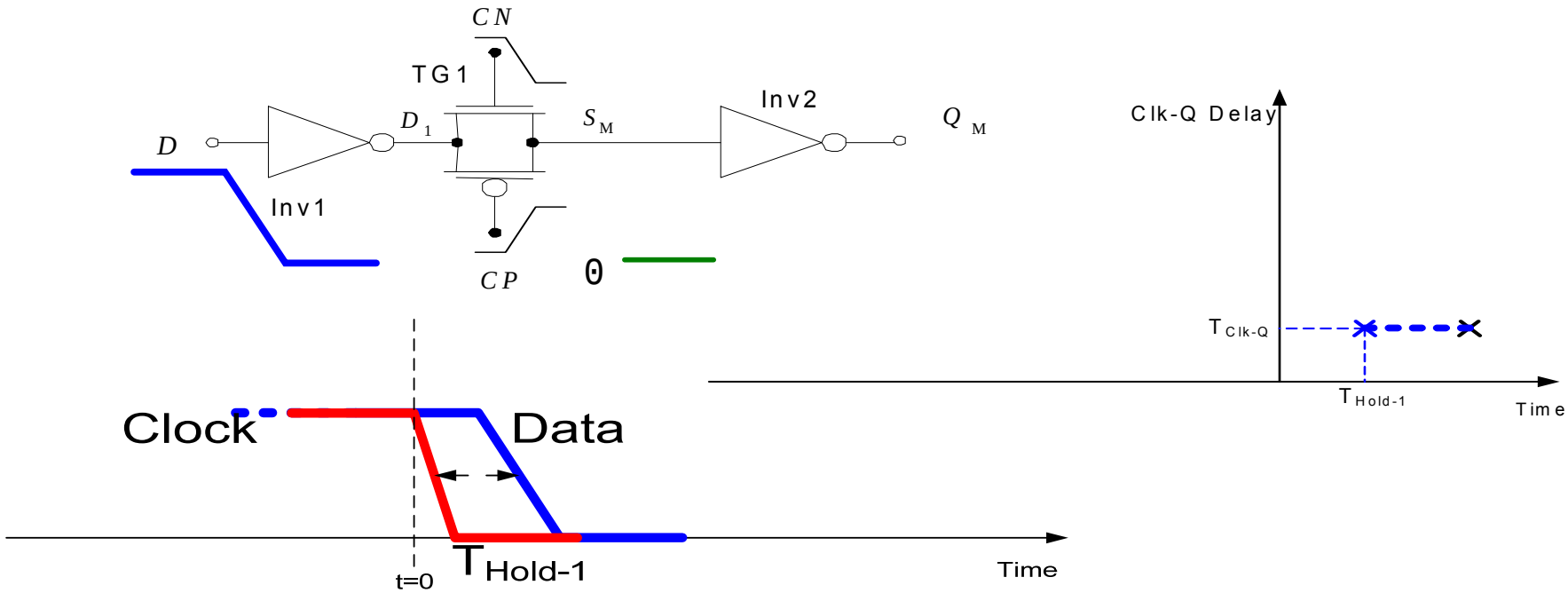
Setup-Hold Time Illustrations

Hold-1 case



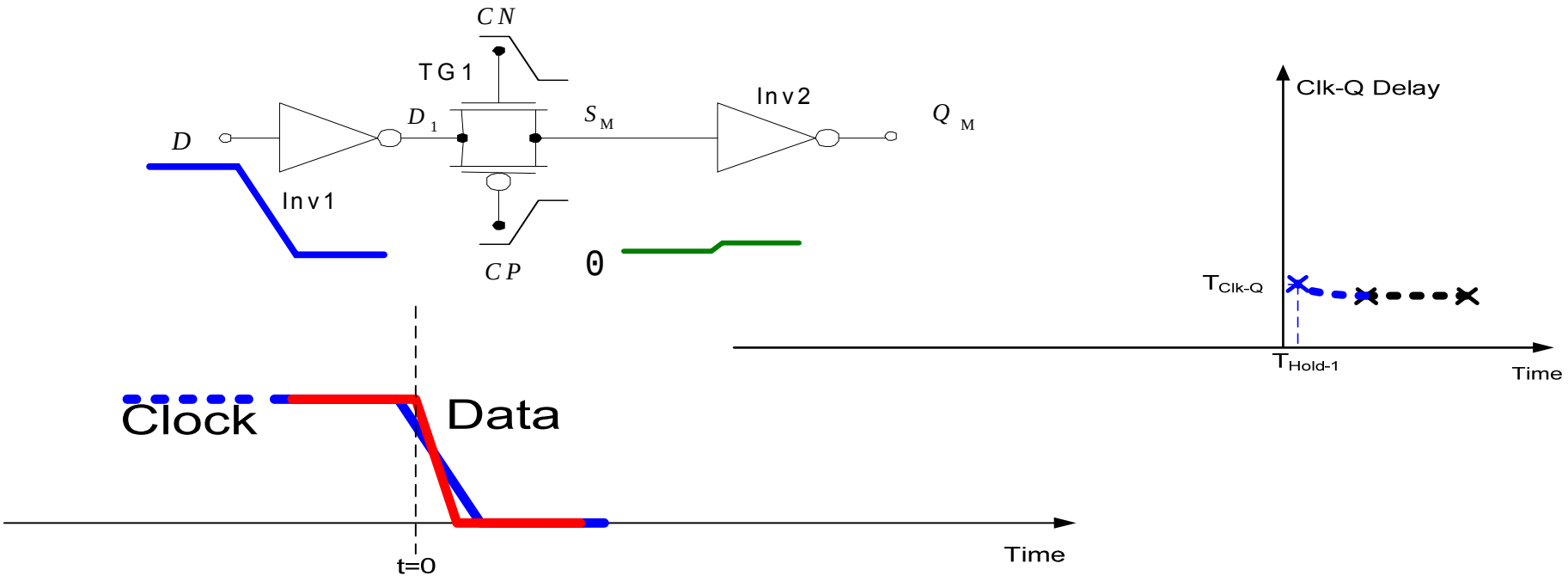
Setup-Hold Time Illustrations

Hold-1 case



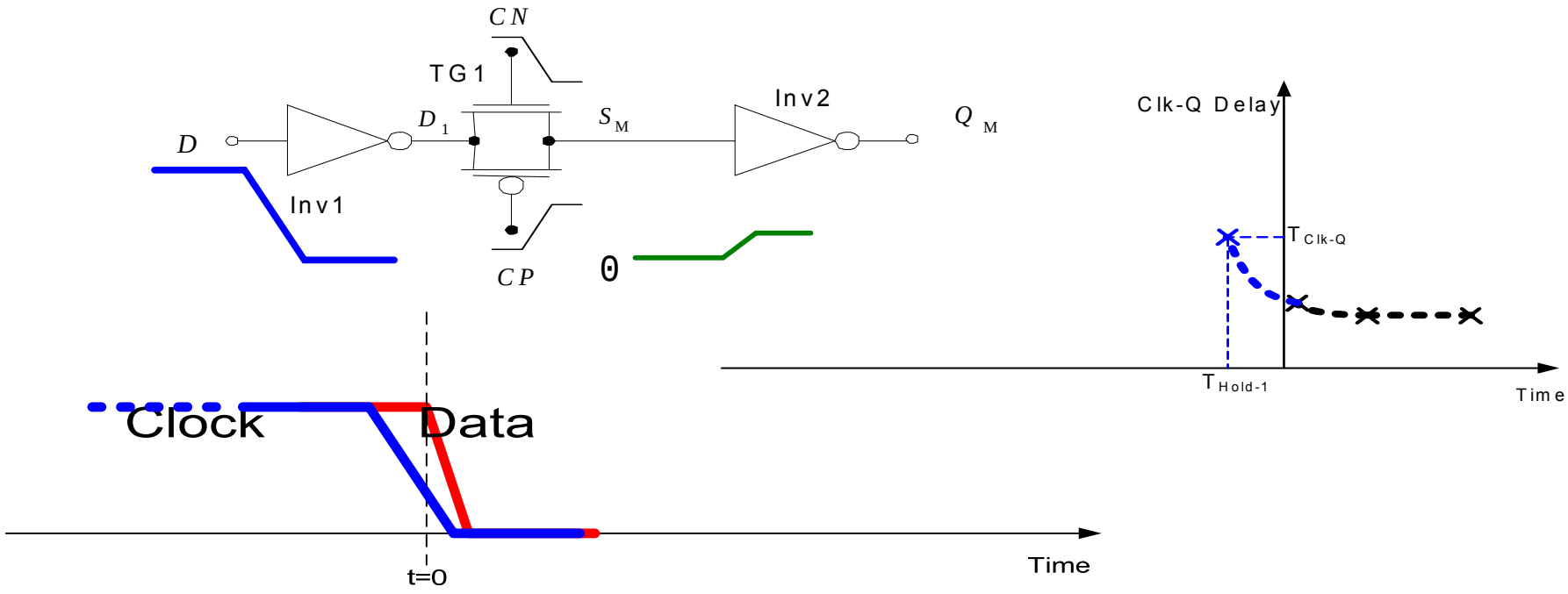
Setup-Hold Time Illustrations

Hold-1 case



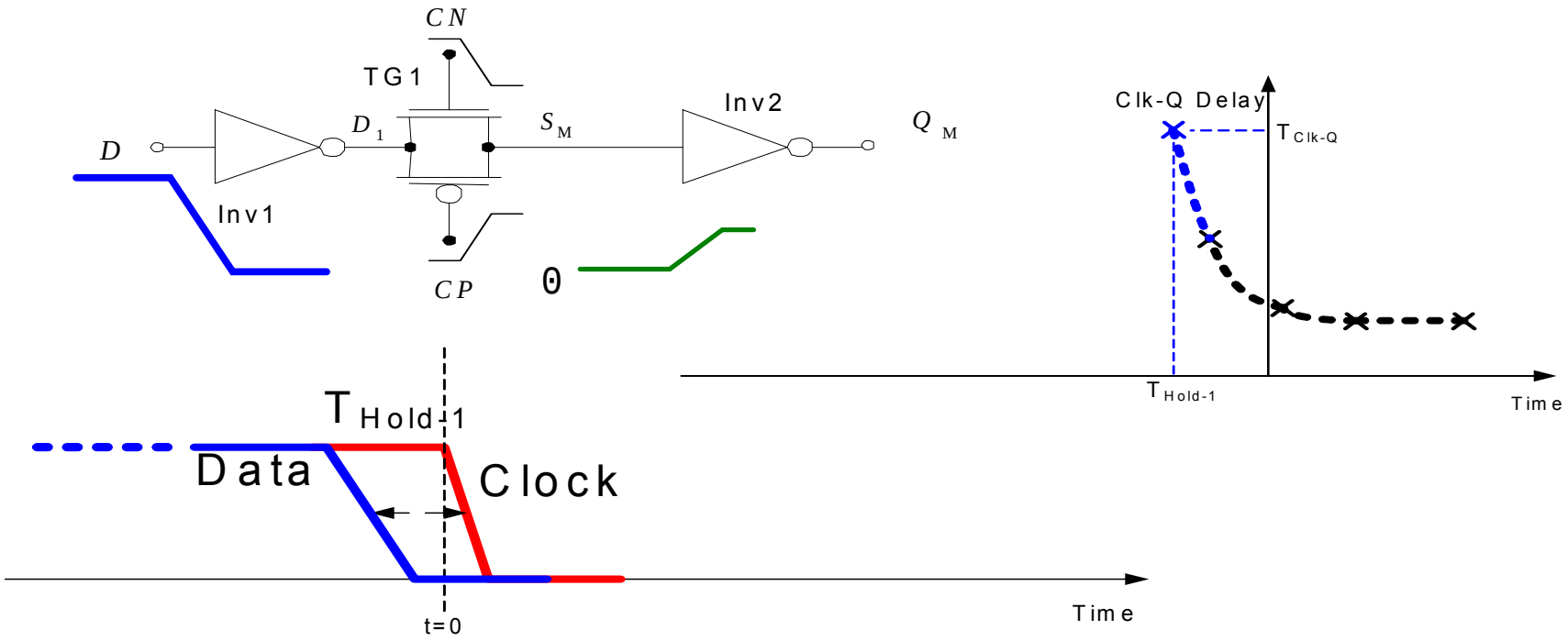
Setup-Hold Time Illustrations

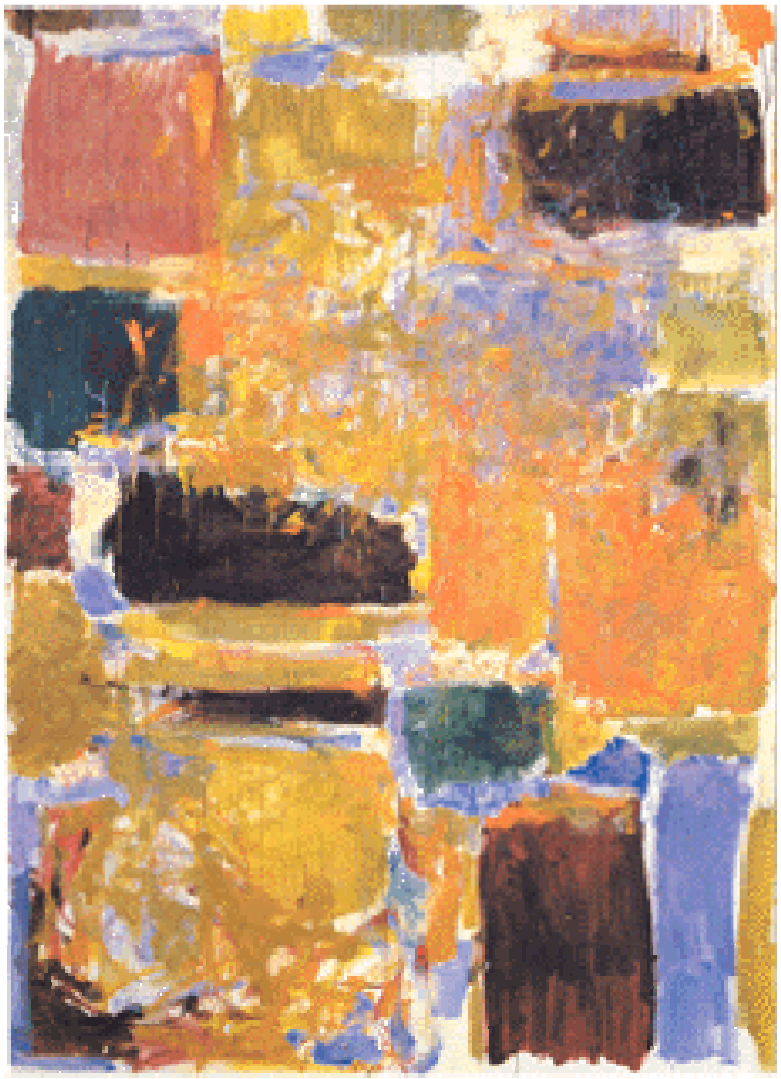
Hold-1 case



Setup-Hold Time Illustrations

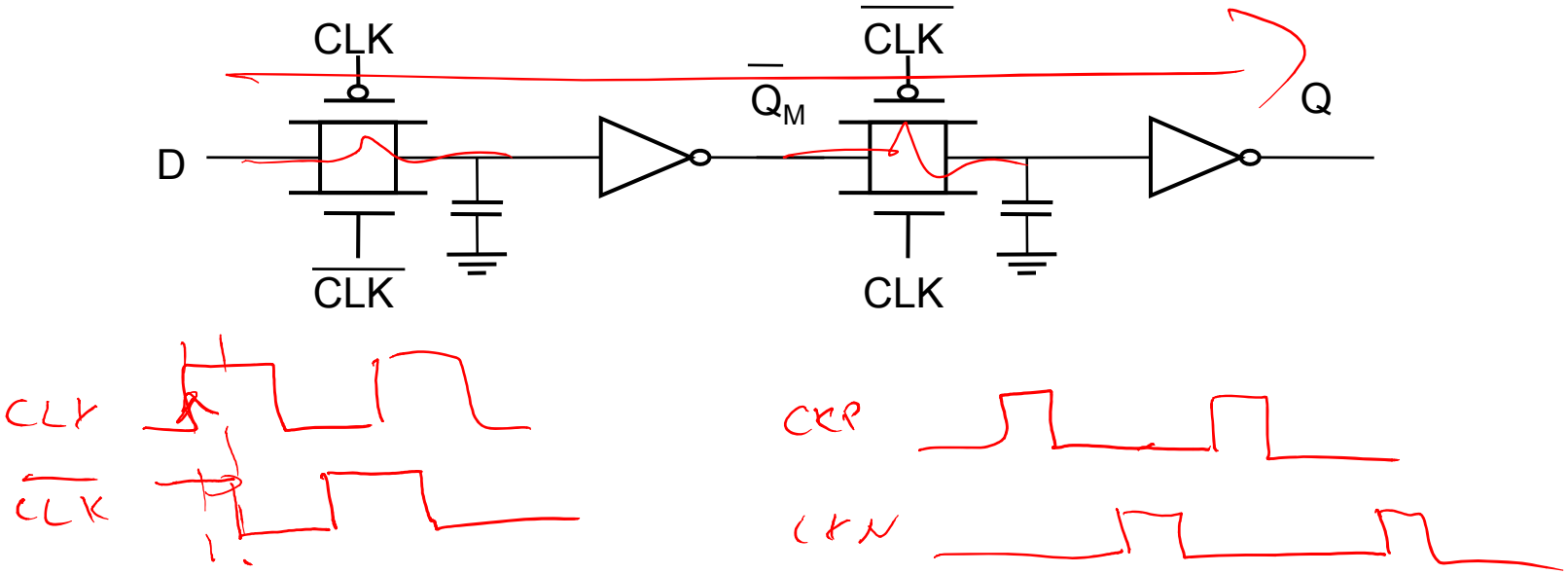
Hold-1 case





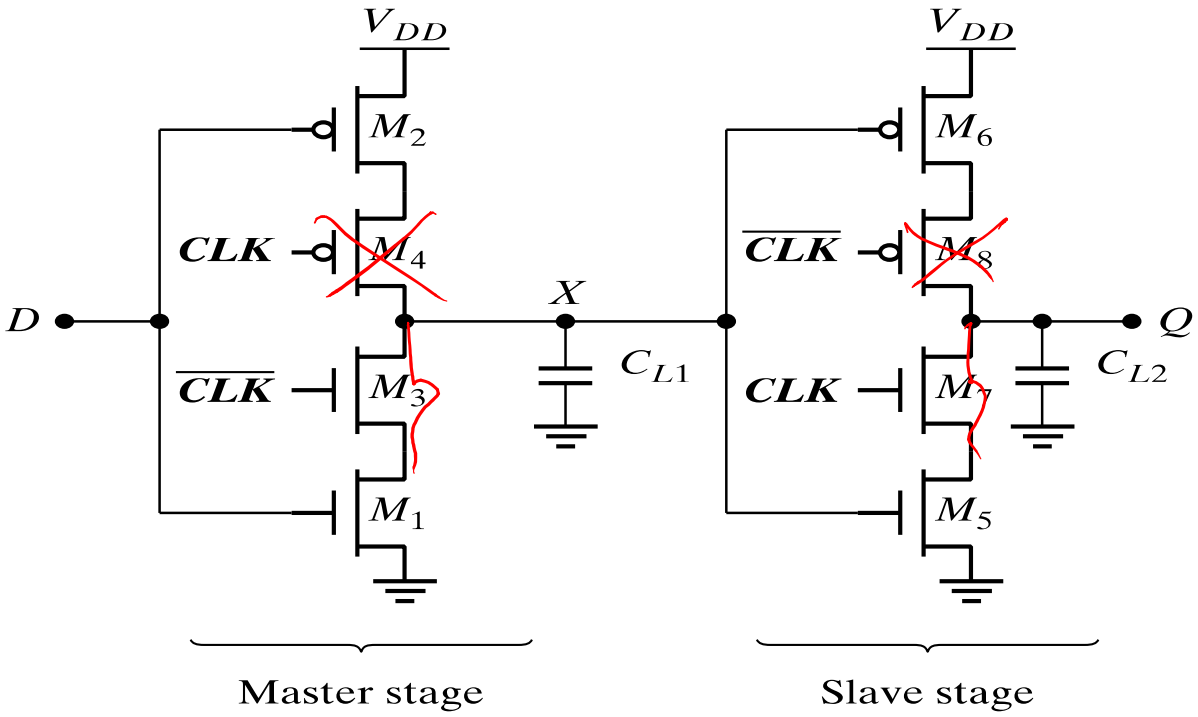
Race conditions

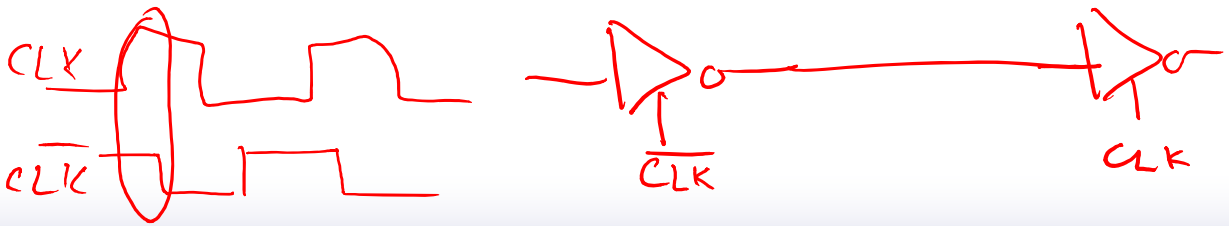
Pass-gate MS Register



- Only works with non-overlapping clocks
- Race-through condition with overlapping clocks

Other Latches/Registers: C²MOS





C^2MOS – No Races

Latch-Based Design

- N latch is transparent when $\Phi = 0$
- P latch is transparent when $\Phi = 1$