University of California at Berkeley
Department of Electrical Engineering and Computer Science

EECS150/EE141/EE241A, Fall 2014

Homework 5: Wires and Energy

Due: Friday Oct 10, 5pm

Please include your name, SID and specify either CS150, EE141 or EE241A at the top of your homework handin. Homeworks must be submitted electronically as a signle file in PDF format.

Solution : For grading, each question is worth 25 points, and breakdown for each part is included in the solutions.

Problem 1: Elmore delay calculation

For the following problem, $C_G = C_D = 2fF/\mu m$, a 1x inverter has $L = 0.1\mu m, W_p = 2\mu m, W_n = 1\mu m$, with $R_{n,on} = 10\frac{k\Omega}{\square}$, $R_{p,on} = 20\frac{k\Omega}{\square}$,$R_{wire} = 0.1\frac{\Omega}{\square}$, parallel plate capacitance $C_{pp} = 20aF/\mu m^2$, and total fringing capacitance $C_{fr} = 14aF/\mu m$.

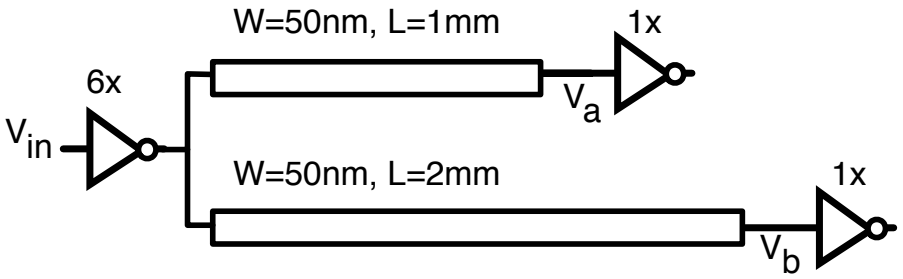

Figure 1

a) Using the π wire model, draw the equivalent RC switch model. What is the propogation delay from a step at V_{in} to V_a and V_b?

Solution : *15 points*

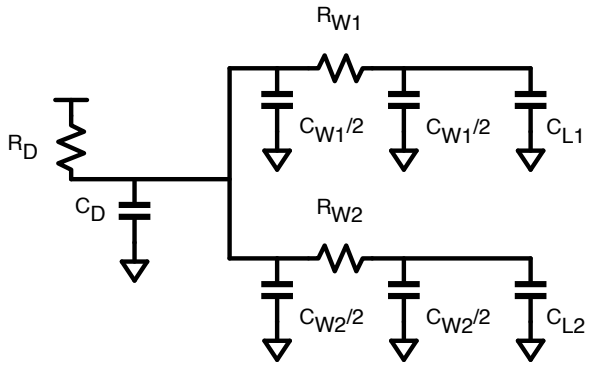

Figure 2

$$
\begin{aligned}
R_D &= \frac{1k}{6} = 167\Omega \\
R_{W1} &= 0.1\Omega \cdot \frac{1mm}{50nm} = 2k\Omega \\
R_{W2} &= 0.1\Omega \cdot \frac{2mm}{50nm} = 4k\Omega \\
C_D &= 2\frac{fF}{um} \cdot (2um + 1um) \cdot 6 = 36fF \\
C_{L1} &= C_{L2} = 2\frac{fF}{um} \cdot (2um + 1um) = 6fF \\
C_{W1} &= 20\frac{aF}{um^2} \cdot 0.05um \cdot 1000um + 14\frac{aF}{um} \cdot 1000um \\
&= 1fF + 14fF = 15fF \\
C_{W2} &= 20\frac{aF}{um^2} \cdot 0.05um \cdot 2000um + 14\frac{aF}{um} \cdot 2000um \\
&= 2fF + 28fF = 30fF \\
t_{D,Va} &= ln(2)[(R_{W1} + R_D)(C_{L1} + \frac{C_{W1}}{2}) + (R_D)(C_D + C_{W2} + C_{L2} + \frac{C_{W1}}{2})] \\
&= 0.69[(2k + 167)(6f + 7.5F) + (167)(36f + 30f + 6f + 7.5f)] \\
&= 0.69[(29.3p + 13.3p)] = 29.3ps \\
t_{D,Vb} &= ln(2)[(R_{W2} + R_D)(C_{L2} + \frac{C_{W2}}{2}) + (R_D)(C_D + C_{W1} + C_{L1} + \frac{C_{W2}}{2})] \\
&= 0.69[(4k + 167)(6f + 15F) + (167)(36f + 15f + 6f + 15f)] \\
&= 0.69[(87.5p + 12.0p)] = 68.7ps
\end{aligned}
$$

b) What is the skew (difference in arrival time at V_a and V_b)?

Solution : *5 points*

$$t_{skew} = |t_{D,Va} - t_{D,Vb}| = 39.4ps$$

c) What is the skew relative to the longest path? If the supply voltage is decreased, will the relative skew increase or decrease? Why? (Hint: what happens to your answer from part (a) and (b) if $R_D >> R_W$.)

Solution : *5 points*

Relative skew is

$$t_{skew,rel} = 39.4ps/68.7ps = 0.57$$

The relative skew decreases. As the supply voltage decreases, the R and C of the wires stay constant while the R of the transistor increases (less overdrive voltage). At the extreme, $R_D >> R_W$, factor out R_D, and the capacitances are equal so $t_{D,Va} = t_{D,Vb}$. The question asked about relative skew because as R_D increases, the absolute delay and therefore skew will actually get larger. But the relative skew will decrease, because the wires beging to look less significant compared to the gate. In particular, the wire resistance looks very small compared to the high drive resistance of the inverter. Note that the difference in wire capacitance doesn't affect the answer that much, for two reasons: first, the π model places half of the capacitance before the resistor so both paths see the same half capacitance from both of the wires, and second, when calculating Elmore delay, the resistors off of the measured path get shorted, so capacitance past the resistor also get seen. Note that Elmore delay is an approximation and a bound on the worst case. For example, if you care about the path to C_{L1}, R_{W2} does not appear in the result. But in reality, if R_{W2} is large, then almost all of the current would go to C_{L1} and none to C_{L2}, so including C_{L2} in the delay equation would be pessimistic.

Problem 2: Power and Leakage

Consider an 3-input NOR gate shown in Figure 3 with Vdd=1V, $C_L = 5fF$, $C_D = 2fF/um$, $R_{ON,N} = 16.6\frac{k\Omega}{\square}$, $R_{ON,P} = 33.2\frac{k\Omega}{\square}$, $R_{OFF,N} = 125\frac{M\Omega}{\square}$, $R_{OFF,P} = 200\frac{M\Omega}{\square}$, $L = 0.1\mu m$, $W_N = 1\mu m$, and $W_P = 2\mu m$.

a) Assume that the probability of an input being high is 0.5, and that all inputs are independent. What is the probability that the output is high? What is the probability that the output is low?

Solution : *7 points*

$$P(Out = 1) = P(A = 0) * P(B = 0) * P(C = 0) = 1/8$$
$$P(Out = 0) = 1 - P(Out = 1) = 7/8$$

b) Under the same assumptions as (a), what is the gate activity factor (i.e. the probability that the output will transition from low to high, $P_{0->1}$)?

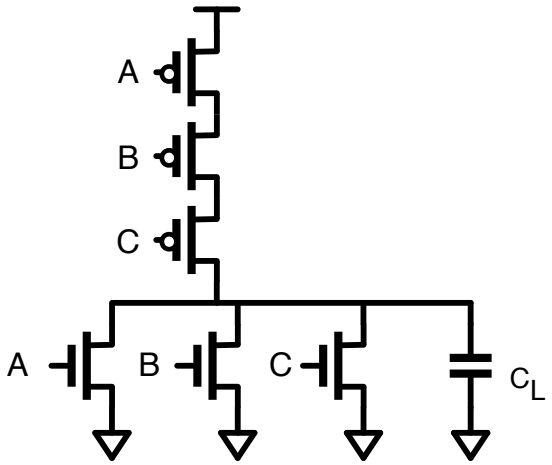

Figure 3

Solution : *6 points*

$$P_{0->1} = P(Out = 0) * P(Out = 1) = 1/8 \cdot 7/8 = 7/64 \approx 0.11$$

c) What is the dynamic power dissipation of the gate if the clock frequency is 3GHz?

Solution : *6 points*

$$\begin{aligned} C_{nmos} &= 2f * (1 + 1 + 1) \\ C_{pmos} &= 2f * (2) \\ P_{dyn} &= a \cdot C_L \cdot V_{DD}^2 \cdot f = 7/64 \cdot (5f + 2f(2 + 3)) \cdot (1V)^2 \cdot 3GHz \\ &= 4.92uW \end{aligned}$$

The solution is also correct if the capacitance in the PMOS stack is included. It was not included in the solution, because in reality, the contribution of the PMOS stack capacitance would depend on the input combinations (eg. if only the C input changes, the capacitance between A/B never gets discharged).

d) What inputs would cause the highest leakage? The lowest leakage?

Solution : *6 points..don't need to include actual calculations or get actual numbers, just get the trend correct and explain.*

If the output is 1, all of the PMOS are on and the NMOS are leaking. $I_{leak} = \frac{1}{R_{total}} = \frac{1}{R_{pmos}+R_{nmos}} = \frac{1}{(R_{off,n}*0.1/1*1/3)+(R_{on,p}*0.1/2*3} = \frac{1}{125M*0.1/3+33.2k*0.1/2*3} = 240nA$ (you could exclude the PMOS entirely and get the same answer because on resistance is much smaller than off resistance...and the following calculations will do just that) If the output is 0, one or more of the NMOS are on, and the PMOS is leaking. The worst case occurs when only one

of the PMOS is off. $I_{leak} = \frac{1}{R_{off,p}*0.1/2} = 100nA$ The best case occurs when all of the PMOS are off $I_{leak} = \frac{1}{R_{off,p}*0.1*3/2} = 33nA$

So the worst case (highest) leakage occurs when A=B=C=0 (maximum parallel leakage paths through the NMOS) and the best case (lowest) leakage occurs when A=B=C=1 (maximum stack effect because 3 high resistances in series).

Problem 3: Energy

For Figure 4, $C_1 = C_2 = 100fF$, transistor capacitance is negligable, Vdd=1V, and $V_{TN} = |V_{TP}| = 0.4$.

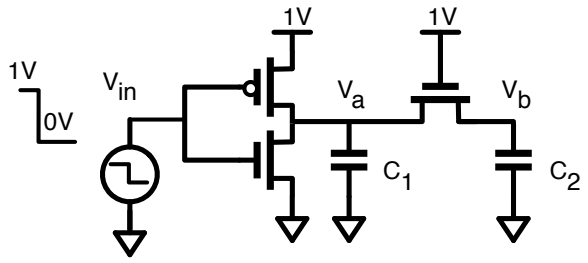

Figure 4

a) How much energy is drawn from the supply for a 1V to 0V step on the input ?

Solution : *7 points*

Note that the NMOS can only pull up to $V_{DD} - V_{TN}$...

$$\begin{aligned} E_{supply} &= (C_1 \Delta V_a)V_{DD} + (C_2 \Delta V_b)V_{DD} \\ &= 100fF(1V)(1V) + (100fF)(0.6V)(1V) \\ &= 160fJ \end{aligned}$$

b) How much energy is stored on the capacitors after the voltage step?

Solution : *7 points*

$$\begin{aligned} E_{stored} &= \frac{1}{2}C_1(V_a)^2 + \frac{1}{2}C_2(V_b)^2 \\ &= 0.5 * 100fF(1V)^2 + 0.5 * (100fF)(0.6V)^2 \\ &= 68fJ \end{aligned}$$

c) Where did the energy go?

Solution : *4 points* The energy was dissipated in the transistors. When the output toggles again, no further charge will be pulled from the supply, and the rest of the energy will be dissipated through the pull down network. This is why we generally talk about energy pulled from the supply, and not necessarily how much is stored on capacitors at any given moment.

d) If this gate's output changes (from 0 to 1) 1 million times in 2 seconds, what would the average power of the gate be?

Solution : You have calculated how much energy gets drawn from the supply for a 0 to 1 transition already. You are told the gate changes 1 million times, so you know the total energy drawn from the supply. Power is just energy per unit time, so divide by the entire period of operation. *4 points*

$$\begin{aligned} P &= E_{total}/T \\ &= E_{supply} * 1 \times^{6} /2s \\ &= 160fJ * 1 \times^{6} /2s \\ &= 80nW \end{aligned}$$

Problem 4: Short-circuit current

Recall the definition of the response of an RC circuit driven by an ideal voltage pulse in Figure 5 and Equation 1.

$$V_{out}(t) = V_{in}(1 - e^{-\frac{t}{RC}}) \tag{1}$$

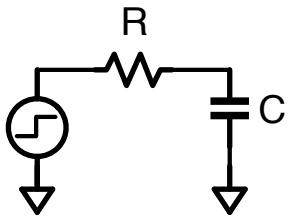

Figure 5: Simple RC circuit corresponding to Equation 1.

a) How much time (in terms of RC) will it take for V_{out} to rise to 50% of V_{in}? (solve for t)

Solution : *3 points*

$$
\begin{aligned}
V_{in}/2 &= V_{in}(1 - e^{-\frac{t}{RC}}) \\
1/2 &= 1 - e^{-\frac{t}{RC}} \\
e^{-\frac{t}{RC}} &= 1/2 \\
ln(e^{-\frac{t}{RC}}) &= ln(1/2) \\
-\frac{t}{RC} &= ln(1) - ln(2) \\
t &= ln(2)RC \\
t_{50} &= 0.69RC
\end{aligned}
$$

b) How much time will it take for V_{out} to rise to 10% of V_{in}?

Solution : *3 points*

$$
\begin{aligned}
0.1 * V_{in} &= V_{in}(1 - e^{-\frac{t}{RC}}) \\
\frac{t}{RC} &= ln(1/0.9) \\
t_{10} &= 0.1RC
\end{aligned}
$$

c) How much time will it take for V_{out} to rise to 90% of V_{in}?

Solution : *3 points*

$$
\begin{aligned}
0.9 * V_{in} &= V_{in}(1 - e^{-\frac{t}{RC}}) \\
\frac{t}{RC} &= ln(1/0.1) \\
t_{90} &= 2.3RC
\end{aligned}
$$

d) What is the rise time (10 to 90%)?

Solution : *3 points*

$$t_r = t_{90} - t_{10} = 2.2RC$$

For the inverter shown in Figure 6, assume that the transistors have $R_{on} = 1k\Omega$, $V_{TN} = |V_{TP}| = 0.4$, $C_{in} = 10fF$, $R_{wire} = 1k\Omega$ and Vdd=1V. Use the switch model of the inverter.

e) For a 1V input step, for how long are both transistors on at the same time?

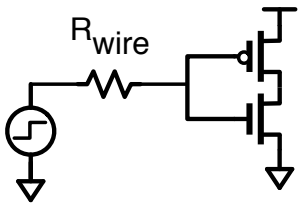

Figure 6: Inverter driven through a wire.

Solution : *5 points*

From 0 to 0.4V, the PMOS is on but the NMOS is off, from 0.4V to 0.6V both are on, and from 0.6V to 1V the NMOS is on but the PMOS is off. So we need to find t_{40} and t_{60}.

$$\begin{aligned}
0.6 * V_{in} &= V_{in}(1 - e^{-\frac{t}{RC}}) \\
\frac{t}{RC} &= ln(1/0.4) \\
t_{60} &= 0.92RC \\
0.4 * V_{in} &= V_{in}(1 - e^{-\frac{t}{RC}}) \\
\frac{t}{RC} &= ln(1/0.6) \\
t_{40} &= 0.51RC \\
t_{on} &= t_{60} - t_{40} = 0.41RC \\
&= 0.41 * 1000 * 10f = 4.1ps
\end{aligned}$$

f) What is the short-circuit power?

Solution : *4 points*

$$P = IV = V^2/R = 1^2/2k = 0.5mW$$

g) How much short-circuit energy is dissipated?

Solution : *4 points*

$$E = P \cdot t = 0.5mW * 4.1ps = 2.05fJ$$

Problem 5 (EE241A Only): Voltage scaling

To gain intuition about voltage scaling, it is important to estimate delay and energy as a function of voltage. The Alpha Power Law model of a transistor's current can estimate delay over a wide voltage range (Equation 2). Additionally, delay can be approximated by modeling transistors as constant current source for the V_{DD} to $V_{DD}/2$ transition (Equation 3). Use these model with $\alpha = 1.3$, $V_T = 0.3V$, and $V_{DD} = 1V$ to answer the following questions about voltage scaling.

$$I \propto (V_{DD} - V_T)^{\alpha} \tag{2}$$

$$t_d \propto \frac{C(V_{DD}/2)}{I} \tag{3}$$

a) Plot V_{DD} vs. delay, V_{DD} vs. power-delay product (PDP), and V_{DD} vs. energy-delay product (EDP) when considering dynamic energy only for $0.35V < V_{DD} < 1V$. At what V_{DD} is minimal energy obtained?

Solution : *15 points*

Energy is always going to be smaller at lower voltages (or if you consider the range provided, $0.35V$)

$$I = (V_{DD} - 0.3)^{1.3} \tag{4}$$

$$t_d = \frac{V_{DD}}{2 \cdot I} = \frac{V_{DD}}{2 \cdot (V_{DD} - 0.3)^{1.3}} \tag{5}$$

$$pdp = V_{DD}^2 f t_d = V_{DD}^2 \tag{6}$$

$$edp = pdp \cdot t_d \tag{7}$$

Once you have these equations, plug them into Python, Matlab, Excel etc and compute for different voltages. Note that power delay product is equal to energy (well, energy consumed during t_D). Solution plots in Figure 7...

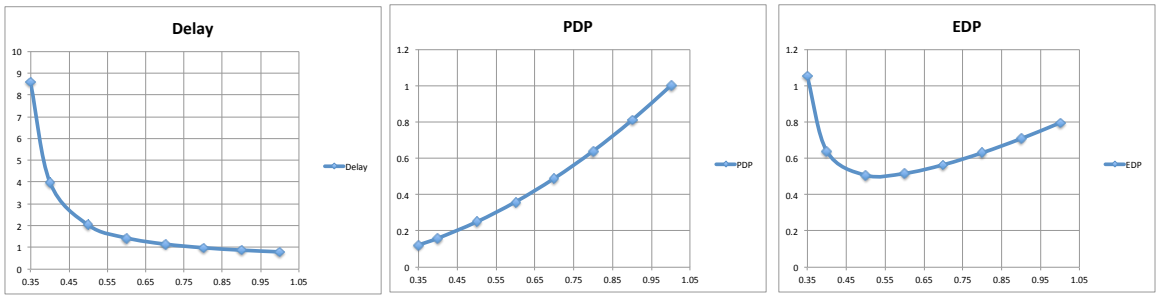

Figure 7

b) Now consider power as a combination of switching energy, activity, and leakage power ($P = C{\cdot}V_{DD}^2{\cdot}a{\cdot}f{+}V_{DD}{\cdot}I_{leak}$) Assume at 1V, the design runs at 1Ghz, $C = 1nF$, and $I_{leak} = 100mA$ Plot energy per cycle vs. V_{DD} for activity factor $a = 0.1, 0.2$. The frequency at each Vdd is equal to t_d times a constant that makes the frequency at 1V be 1GHz. Is voltage scaling more or less effective for high activity factors?

Solution : *10 points*

For 20% activity...

$$f = 1 \times 10^9 * t_{D,1V}/t_D \tag{8}$$

$$E = 1/f * (V_{DD} * 0.1 + 0.2 * 1n * f * V_{DD}^2) \tag{9}$$

Without considering leakage, you always want to scale voltage. But if there is leakage (there always is), then energy will havea minimum. This is because at low voltage near the threshold, delay increases pretty dramatically. This means that each cycle becomes very long, and integrates a lot of leakage current (even if the leakge current is low). So the amount of leakage energy per cycle increases, and actually begins to pass the amount of dynamic energy. The higher the activity factor, the less of an impact this has, because leakage is a smaller proportion of overall energy. Solution plots in Figure 8...

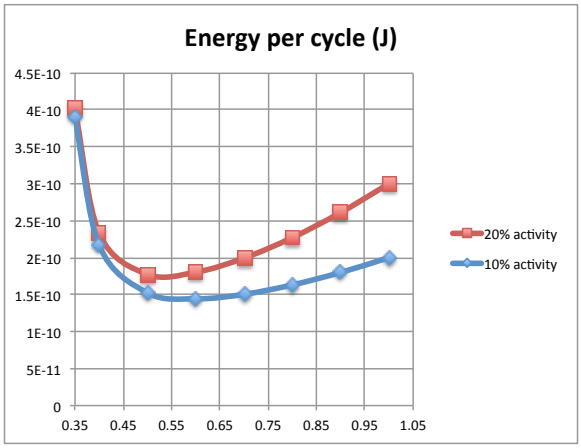

Figure 8