University of California at Berkeley
Department of Electrical Engineering and Computer Science

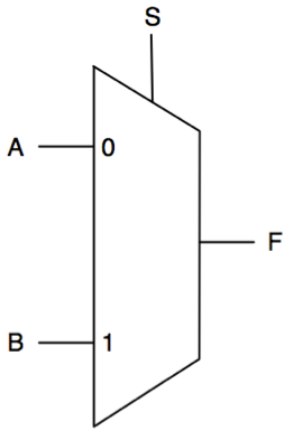
EECS150/EE141/EE241A, Fall 2014

Homework 4: CMOS Logic and Logical Effort

Due: Friday Oct 3, 5pm

Please include your name, SID and specify either CS150, EE141 or EE241A at the top of your homework handin. Homeworks must be submitted electronically as a signle file in PDF format.

1. The gate below is a multiplexer, which selects between its inputs based on the `Sel` input.



   (a) Write out the logical expression for the output as a function of its inputs.

   (b) Implement the MUX using CMOS transistors

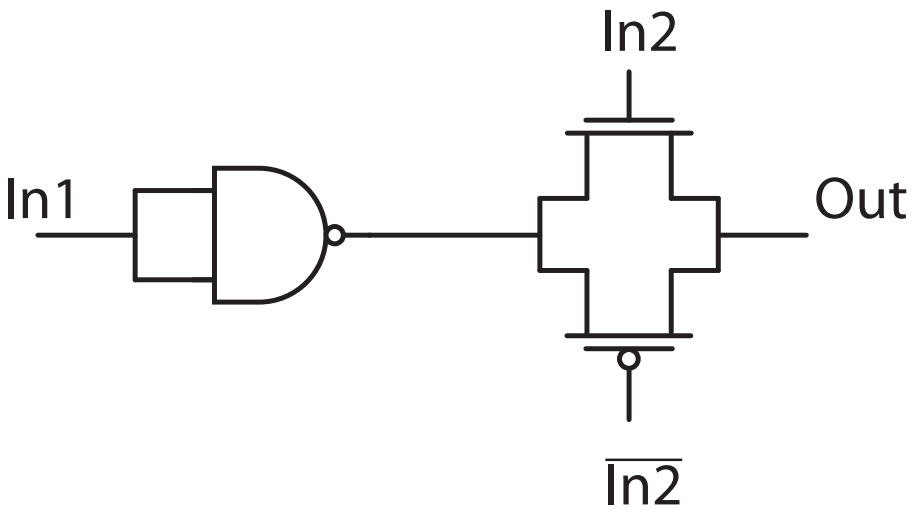
   (c) Create the following logical expressions out of this gate. Report your answer in the form of a table, where the columns correspond to A, B, Sel, and Output. You are given the inputs X and Y, but not their complements. You can also use VDD and GND.

      i. X
      ii. XY
      iii. $X + Y$
      iv. $\overline{X}$
      v. $X\overline{Y}$

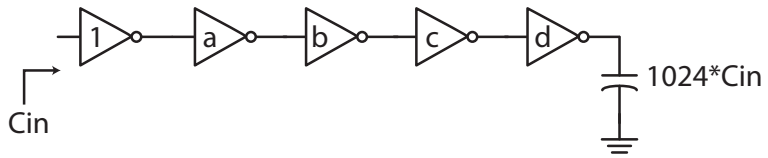
   (d) Create an XOR gate out of 3 multiplexers. Again you have the inputs X and Y, but not their complements.

   (e) Using your implementation from part b, calculate the logical effort for each input for the XOR gate.

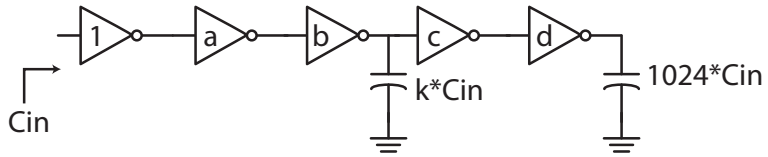
2. Compute the logical effort of the circuit below. Provide separate answers for the input transitioning from low to high and from high to low. Assume the NAND gate is sized for equal pull-up and pull-down strength when the inputs are not tied together (this is the normal way that NAND-gates are sized). What is the function of this circuit?



3. Figure out the sizes for inverters a, b, c, and d such that the delay from input to output is minimized. Use $\gamma = 1$

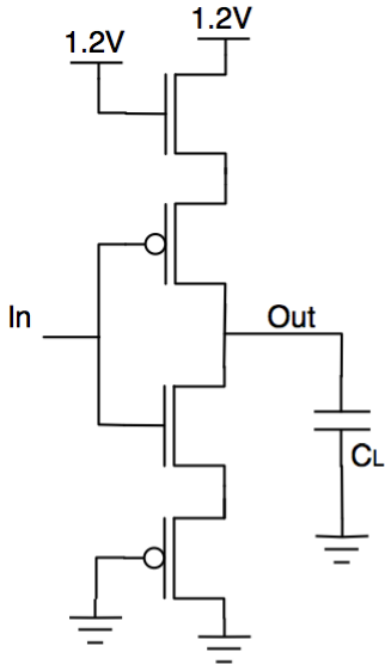


4. Repeat the sizing for minimum delay, but now include the fixed capacitance of `k*Cin` as shown in the figure below.



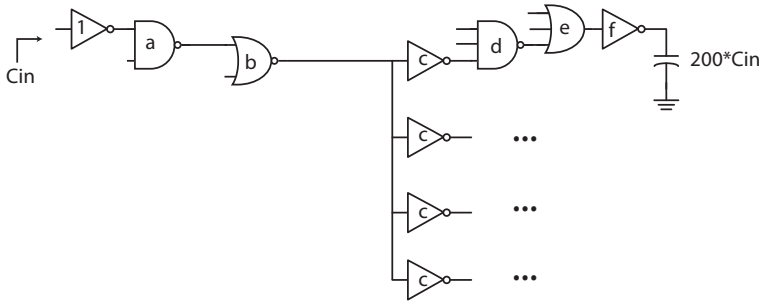
5. Draw the schematic of the CMOS logic gate that implements the function $F = \overline{A + ((BC) + (D + E))}$ Assuming that a balanced inverter is sized 2 to 1 (pmos to nmos) size the schematic for balanced pull-up and pull-down resistance. What is the logical effort of this gate for each input?

6. Sketch the VTC of the gate shown below for each input. Annotate input and output noise voltages in terms of Vdd and Vth. What is the minimum supply voltage that this gate will operate at?



You can assume that $V_{th} = V_{th_N} = |V_{th_P}| = 200mV$.

7. Size the gates in the chain below for minimum delay.



8. **For EE241A only:** Size the gates in the chain below for minimum delay.