CS150 - EE141/241A
Fall 2014
Digital Design and Integrated Circuits

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Lecture 6

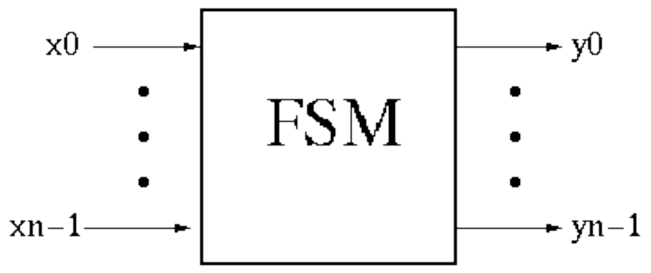
Outline

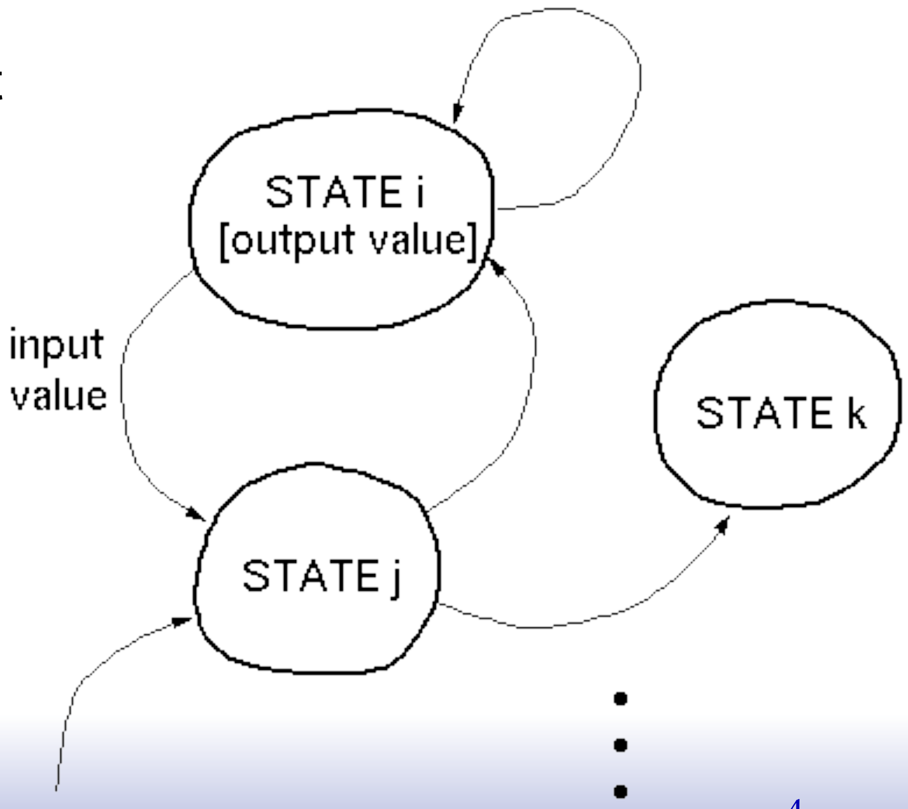
- *Finite State Machine Design Process*
- *Design Example*
- *Moore Versus Mealy Machines*
- *FSMs in Verilog*

FSM Design Process

Finite State Machines (FSMs)

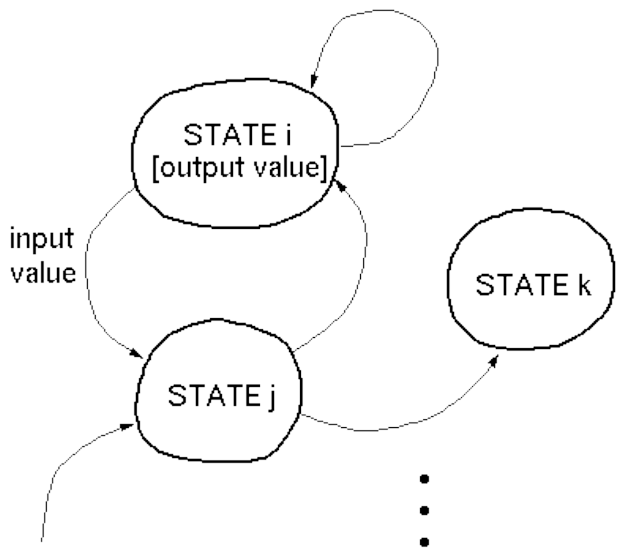
- **FSM** circuits are a type of sequential circuit:
  - output depends on present and past inputs
    - effect of past inputs is represented by the current state

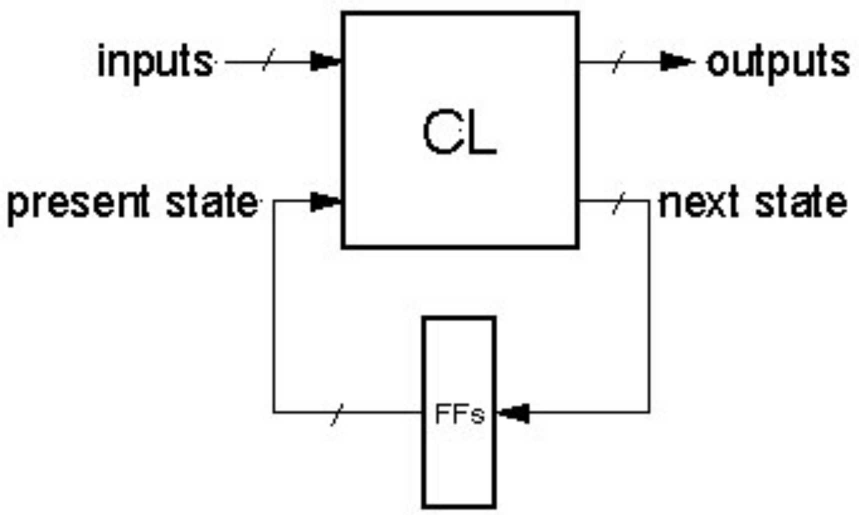




- Behavior is represented by **State Transition Diagram:**
  - traverse one edge per clock cycle.

FSM Implementation





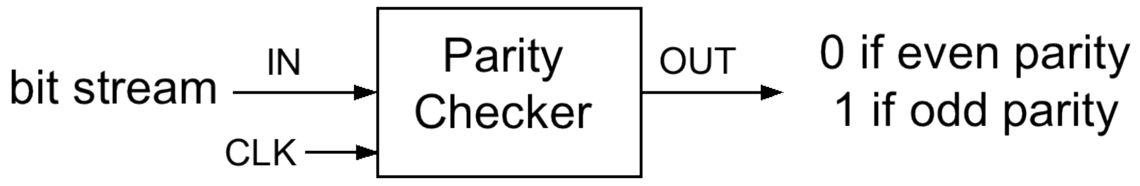
- Flip-flops form state register
- number of states ≤ $2^{\text{number of flip-flops}}$
- CL (combinational logic) calculates next state and output
- Remember: The FSM follows exactly one edge per cycle.

Later we will learn how to implement in Verilog. Now we learn how to design "by hand" to the gate level.

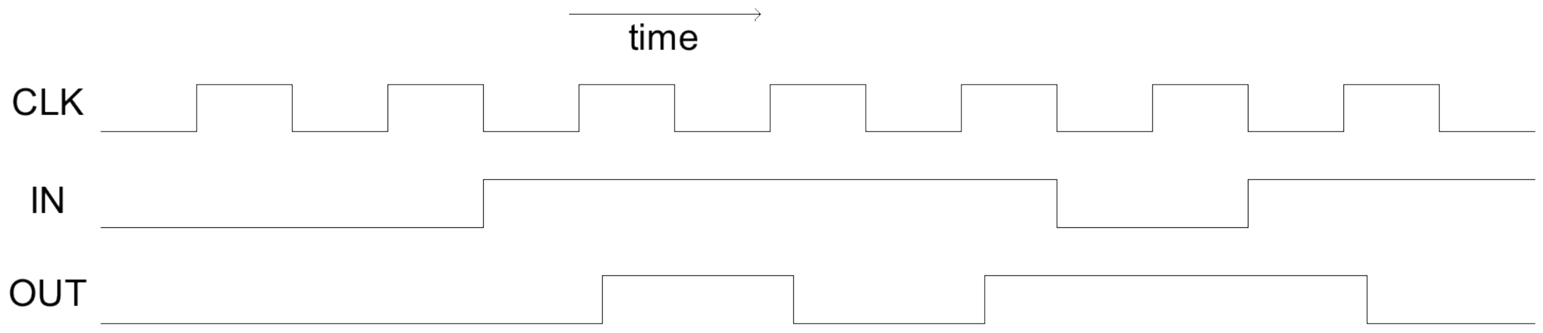
Parity Checker Example

A string of bits has "even parity" if the number of 1's in the string is even.

- Design a circuit that accepts a bit-serial stream of bits and outputs a 0 if the parity thus far is even and outputs a 1 if odd:

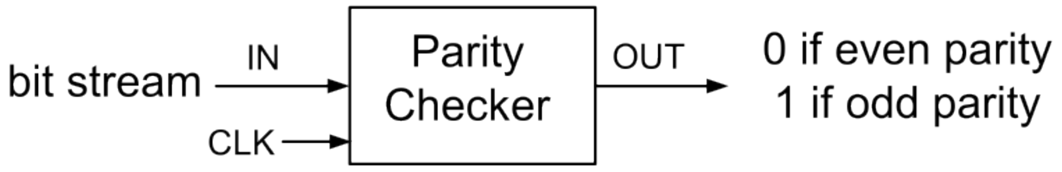


example:	0	0	1	1	1	0	1
	even	even	odd	even	odd	odd	even



Next we take this example through the "formal design process". But first, can you guess a circuit that performs this function?

Formal Design Process

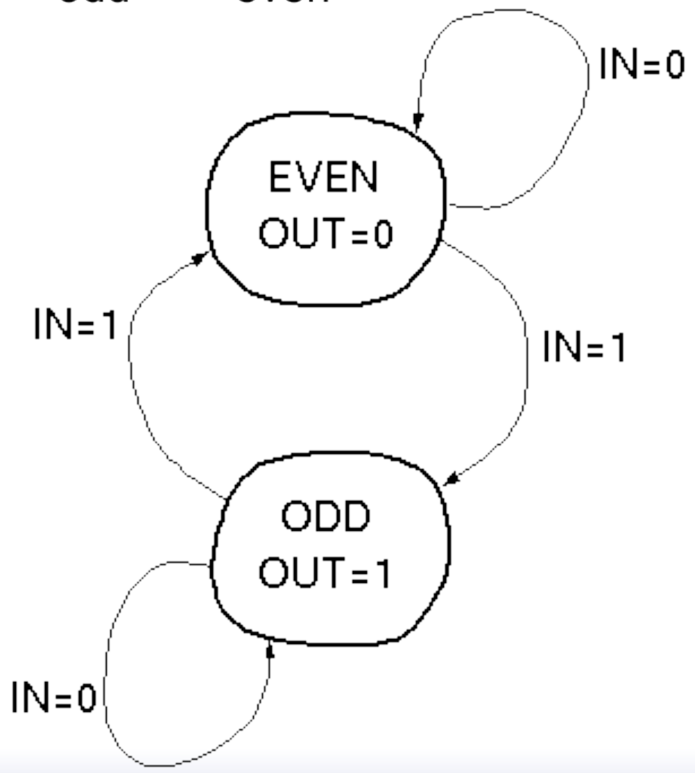


example:	0	0	1	1	1	0	1
	even	even	odd	even	odd	odd	even

time $\longrightarrow$

"State Transition Diagram"

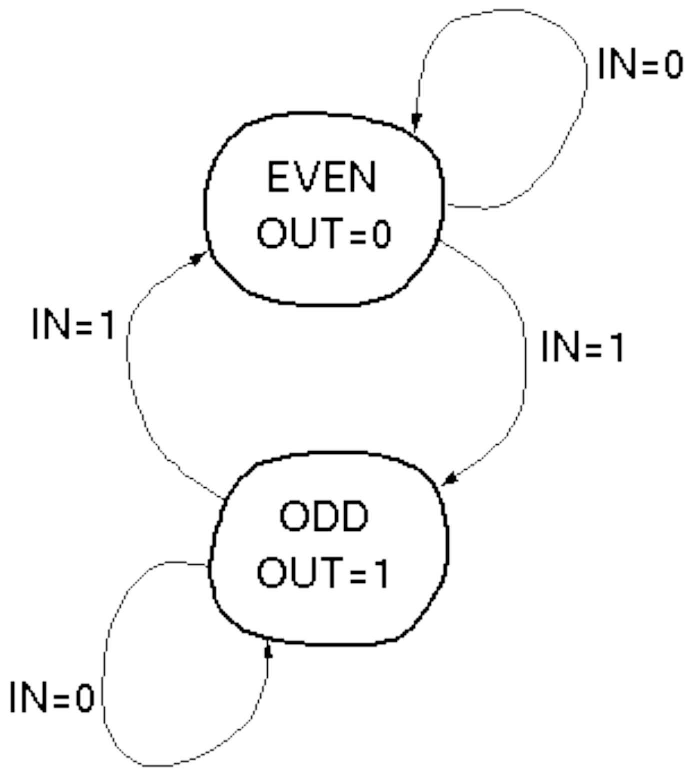
- circuit is in one of two "states".
- transition on each cycle with each new input, over exactly one arc (edge).
- Output depends on which state the circuit is in.



Formal Design Process

State Transition Table:

present state	*OUT*	*IN*	*next state*
EVEN	*0*	*0*	*EVEN*
EVEN	*0*	*1*	*ODD*
ODD	*1*	*0*	*ODD*
ODD	*1*	*1*	*EVEN*



Invent a code to represent states:

Let 0 = EVEN state, 1 = ODD state

present state (ps)	*OUT*	*IN*	*next state (ns)*
0	*0*	*0*	*0*
0	*0*	*1*	*1*
1	*1*	*0*	*1*
1	*1*	*1*	*0*

Derive logic equations from table (how?):

OUT = PS

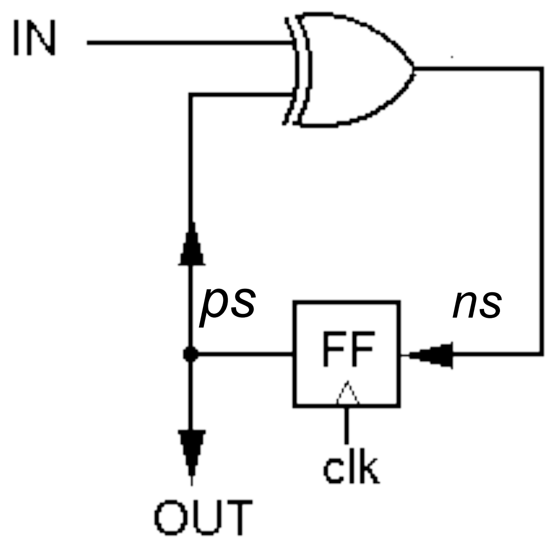
NS = PS xor IN

Formal Design Process

Logic equations from table:

OUT = PS

NS = PS xor IN



- Circuit Diagram:
  - XOR gate for NS calculation
  - DFF to hold present state
  - no logic needed for output in this example.

Formal Design Process

Review of Design Steps:

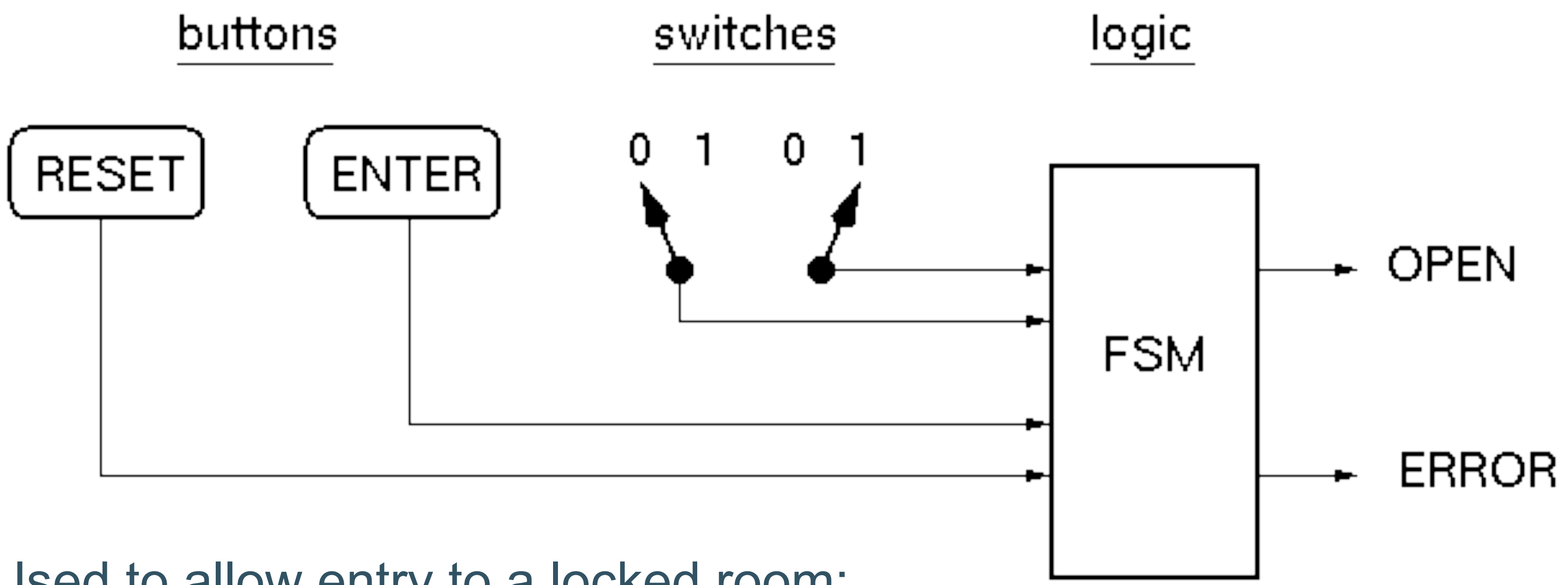
1. *Specify circuit function (English)*
2. *Draw state transition diagram*
3. *Write down symbolic state transition table*
4. *Write down encoded state transition table*
5. *Derive logic equations*
6. *Derive circuit diagram*

   Register to hold state

   Combinational Logic for Next State and Outputs

FSM Design Example

Combination Lock Example



- Used to allow entry to a locked room:

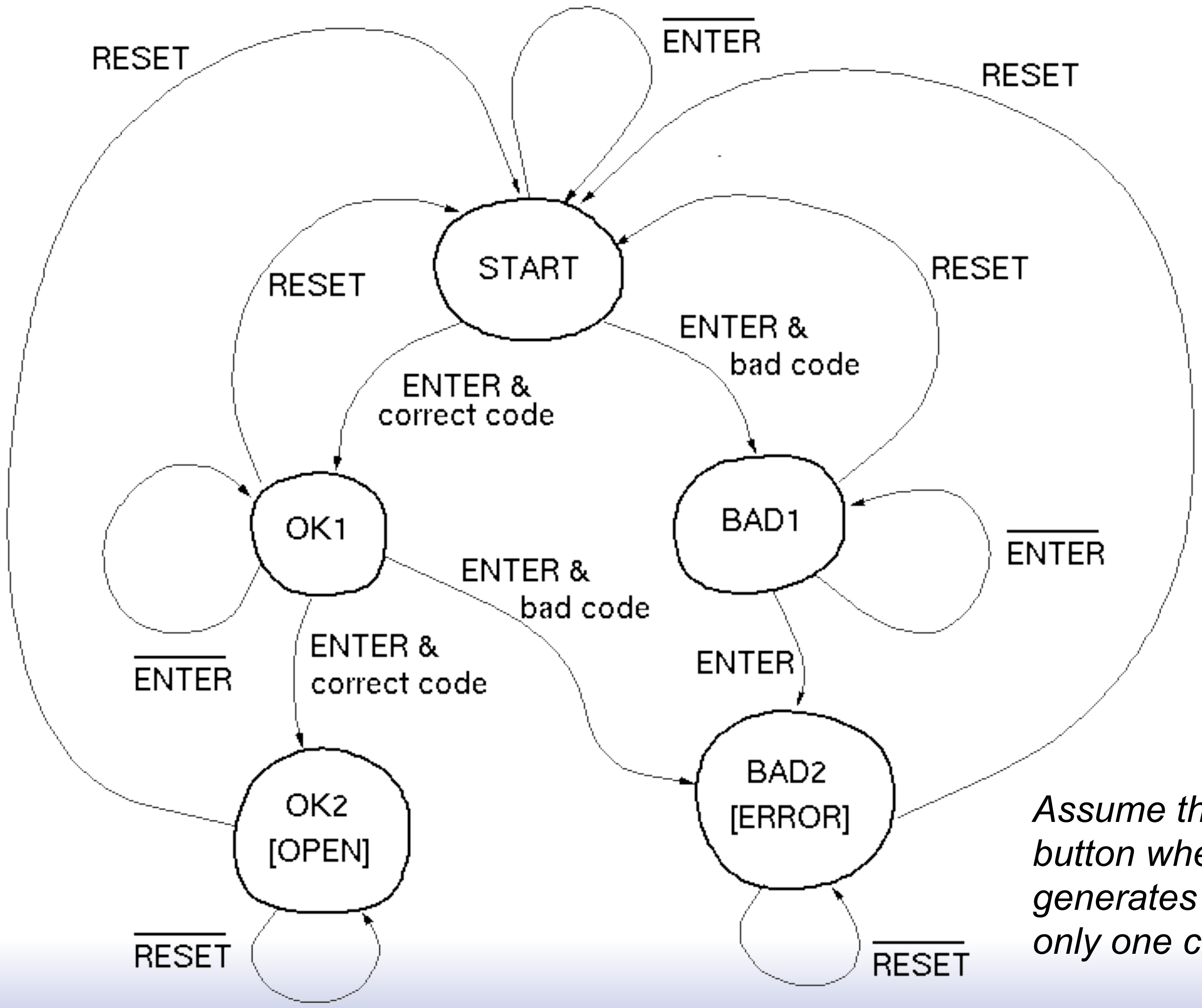
  2-bit serial combination. Example 01,11:

  1. Set switches to 01, press ENTER
  2. Set switches to 11, press ENTER
  3. OPEN is asserted (OPEN=1).

  If wrong code, ERROR is asserted (after second combo word entry).

  Press Reset at anytime to try again.

Combinational Lock STD

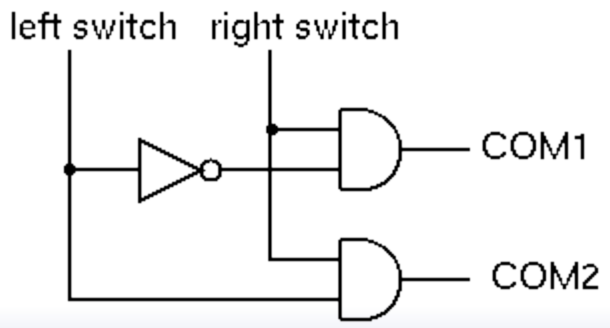


Assume the ENTER button when pressed generates a pulse for only one clock cycle.

Symbolic State Transition Table

RESET	ENTER	COM1	COM2	Preset State	Next State	OPEN	ERROR
0	0	*	*	START	START	0	0
0	1	0	*	START	BAD1	0	0
0	1	1	*	START	OK1	0	0
0	0	*	*	OK1	OK1	0	0
0	1	*	0	OK1	BAD2	0	0
0	1	*	1	OK1	OK2	0	0
0	*	*	*	OK2	OK2	1	0
0	0	*	*	BAD1	BAD1	0	0
0	1	*	*	BAD1	BAD2	0	0
0	*	*	*	BAD2	BAD2	0	1
1	*	*	*	*	START	0	0

Decoder logic for checking combination (01,11):



Encoded ST Table

ENTER	COM1	COM2	PS2	PS1	PS0	NS2	NS1	NS0
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0
1	0	0	0	0	0	1	0	0
1	0	1	0	0	0	1	0	0
1	1	0	0	0	0	0	0	1
1	1	1	0	0	0	0	0	1
0	0	0	0	0	1	0	0	1
0	0	1	0	0	1	0	0	1
0	1	0	0	0	1	0	0	1
0	1	1	0	0	1	0	0	1
1	0	0	0	0	1	1	0	1
1	1	0	0	0	1	1	0	1
1	0	1	0	0	1	0	1	1
1	1	1	0	0	1	0	1	1
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1	1	1	0	1	1	0	1	1
0	0	0	1	0	0	1	0	0
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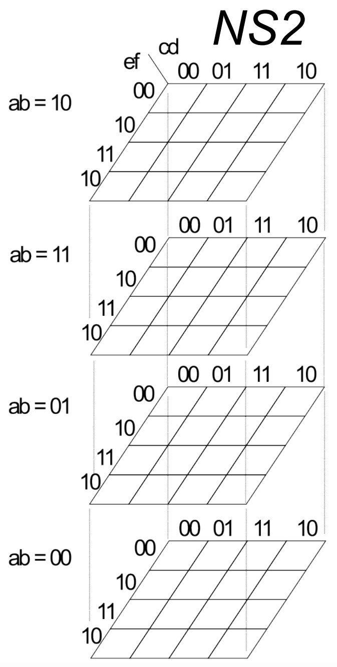
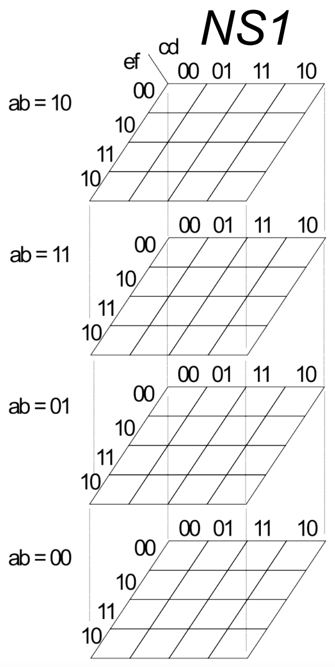
0	1	0	1	0	0	1	0	0
0	1	1	1	0	0	1	0	0
1	0	0	1	0	0	1	0	1
1	0	1	1	0	0	1	0	1
1	1	0	1	0	0	1	0	1
1	1	1	1	0	0	1	0	1
0	0	0	1	0	1	1	0	1
0	0	1	1	0	1	1	0	1
0	1	0	1	0	1	1	0	1
0	1	1	1	0	1	1	0	1
1	0	0	1	0	1	1	0	1
1	0	1	1	0	1	1	0	1
1	1	0	1	0	1	1	0	1
1	1	1	1	0	1	1	0	1

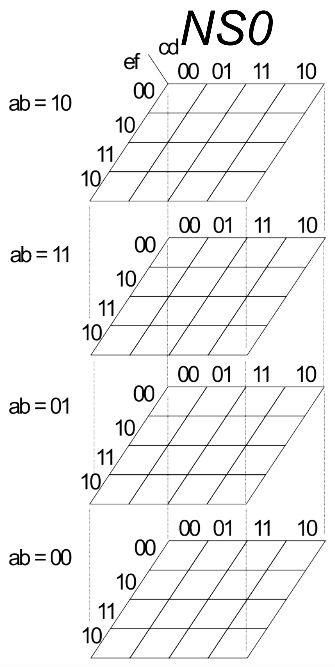
- *Assign states:*

START=000, OK1=001, OK2=011
BAD1=100, BAD2=101

- *Omit reset. Assume that primitive flip-flops has reset input.*
- *Rows not shown have don't cares in output. Correspond to invalid PS values.*

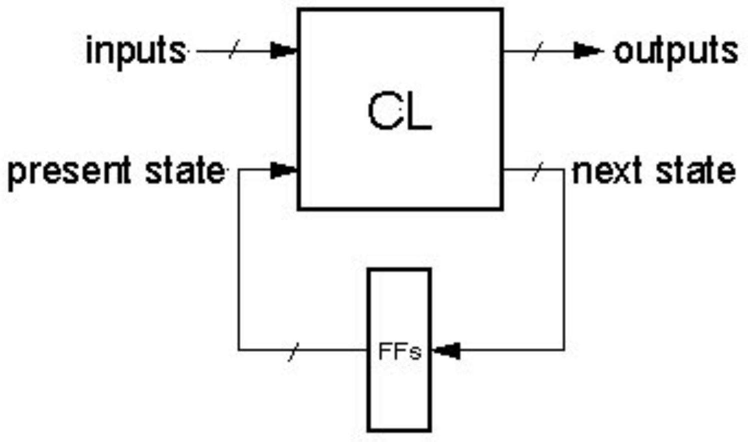






- *What are the output functions for OPEN and ERROR?*

State Encoding



- In general:

  # of possible FSM state = $2^{\text{\# of Flip-flops}}$

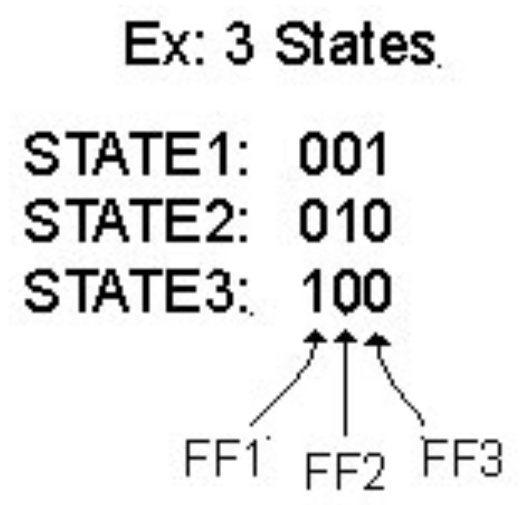
  Example:

  state1 = 01, state2 = 11, state3 = 10, state4 = 00

- However, often more than $\log_2$(# of states) FFs are used, to simplify logic at the cost of more FFs.
- Extreme example is one-hot state encoding.

State Encoding

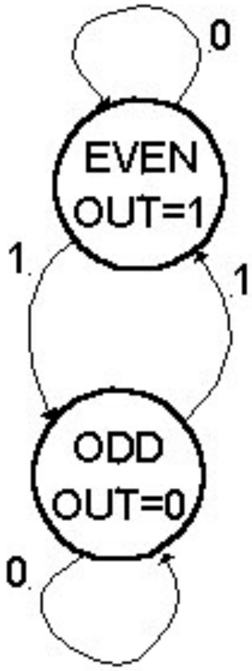
- One-hot encoding of states.
- One FF per state.

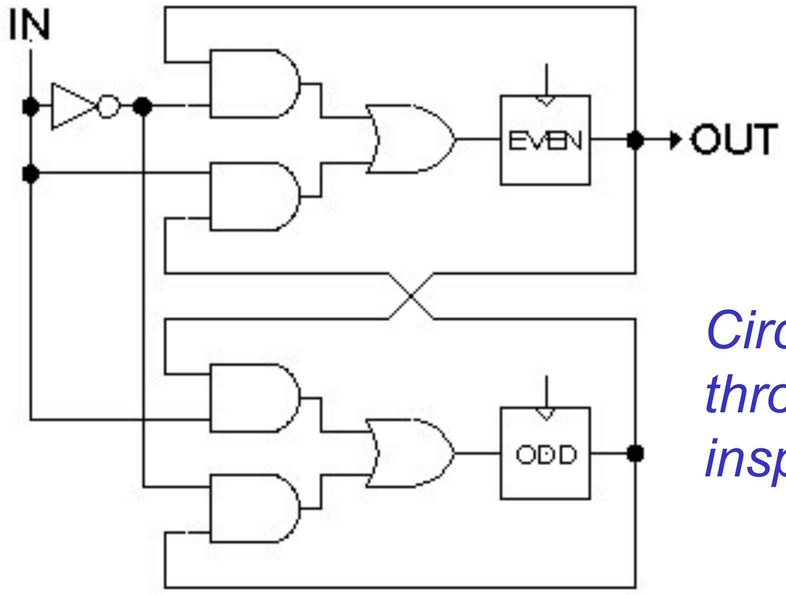


- Why one-hot encoding?
  - Simple design procedure.
    - Circuit matches state transition diagram (example next page).
  - Often can lead to simpler and faster "next state" and output logic.
- Why not do this?
  - Can be costly in terms of Flip-flops for FSMs with large number of states.
- FPGAs are "Flip-flop rich", therefore one-hot state machine encoding is often a good approach.

One-hot encoded FSM

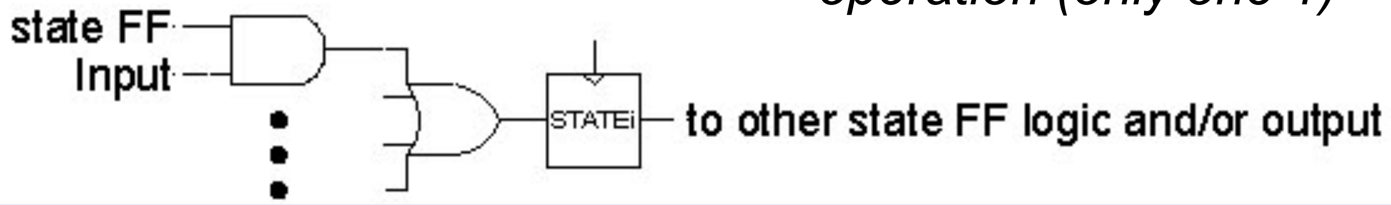
- Even Parity Checker Circuit:





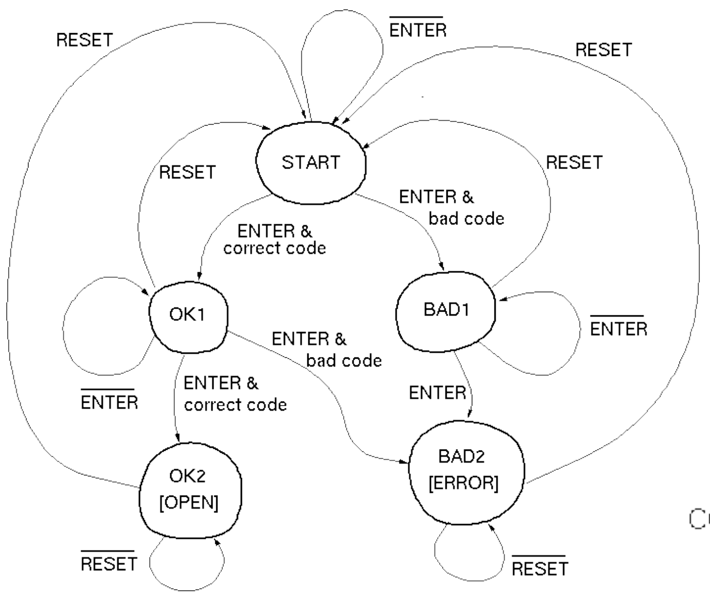
Circuit generated through direct inspection of the STD.

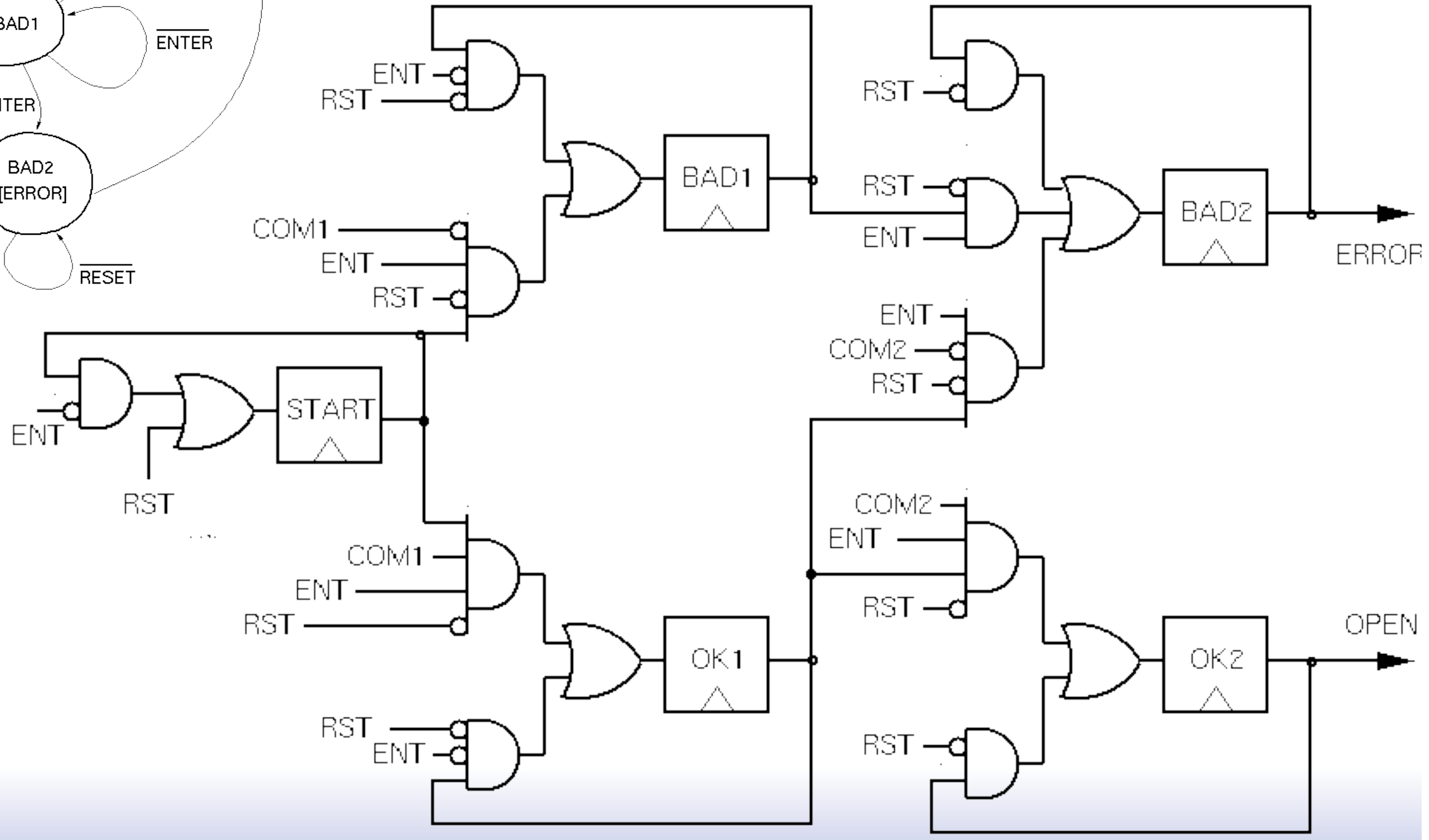
- In General:



- *FFs must be initialized for correct operation (only one 1)*

One-hot encoded combination lock

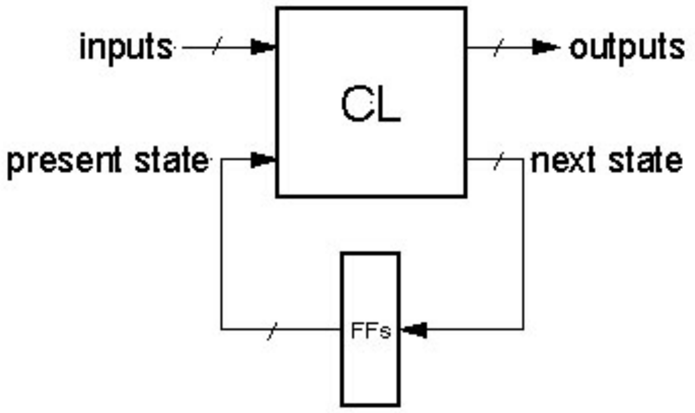




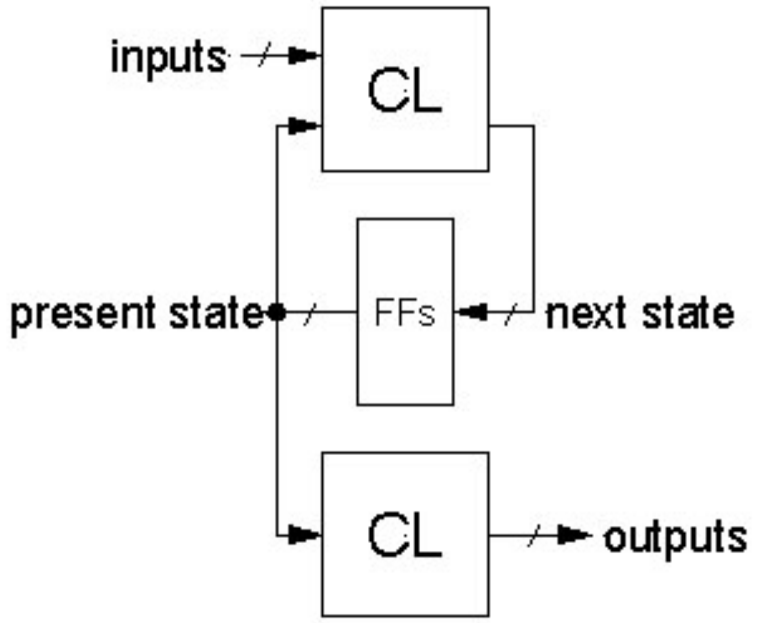
Moore Versus Mealy Machines

FSM Implementation Notes

- General FSM form:



- All examples so far generate output based only on the present state:

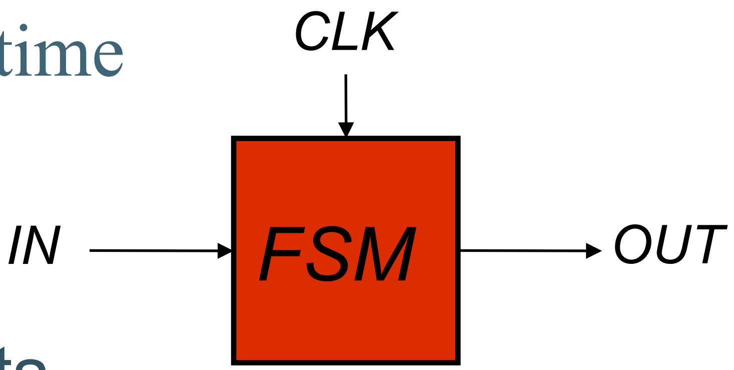


- Commonly name Moore Machine
  (If output functions include both present state and input then called a Mealy Machine)

Finite State Machines

- Example: Edge Detector

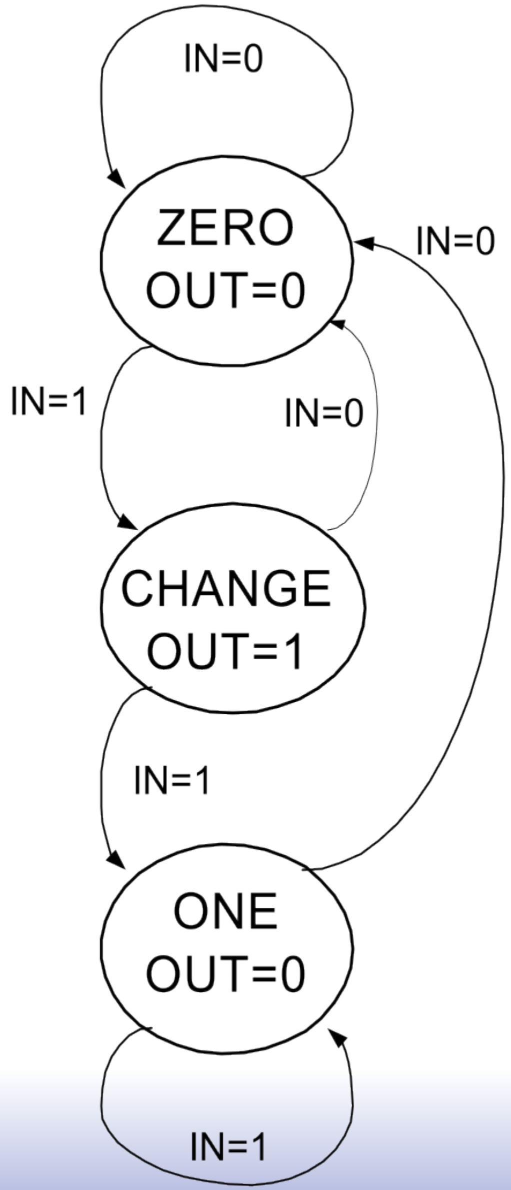
  Bit are received one at a time (one per cycle), such as: 000111010 $\longrightarrow$ time



  Design a circuit that asserts its output for one cycle when the input bit stream changes from 0 to 1.

  We'll try two different solutions.

State Transition Diagram Solution A



	IN	PS	NS	OUT
ZERO	0	00	00	0
	1	00	01	0
CHANGE	0	01	00	1
	1	01	11	1
ONE	0	11	00	0
	1	11	11	0

Solution A, circuit derivation

	IN	PS	NS	OUT
ZERO	0	00	00	0
	1	00	01	0
CHANGE	0	01	00	1
	1	01	11	1
ONE	0	11	00	0
	1	11	11	0

$$\begin{array}{c|cccc} \text{IN} \backslash \text{PS} & 00 & 01 & 11 & 10 \\ \hline 0 & 0 & 0 & 0 & - \\ 1 & 0 & 1 & 1 & - \end{array}$$

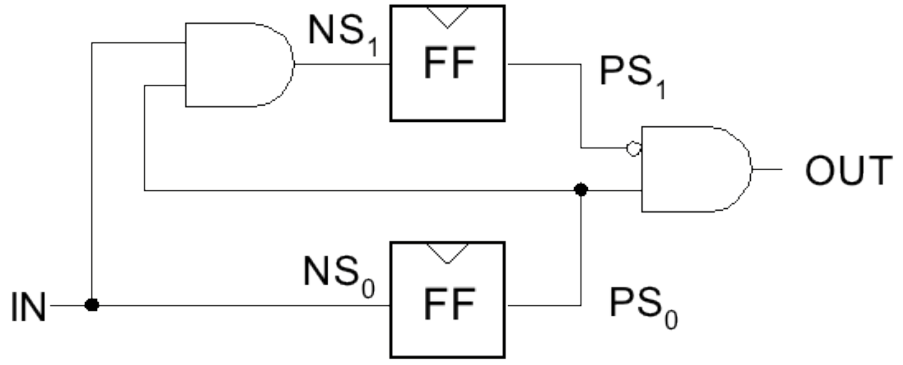
$NS_1 = IN\ PS_0$

$$\begin{array}{c|cccc} \text{IN} \backslash \text{PS} & 00 & 01 & 11 & 10 \\ \hline 0 & 0 & 0 & 0 & - \\ 1 & 1 & 1 & 1 & - \end{array}$$

$NS_0 = IN$

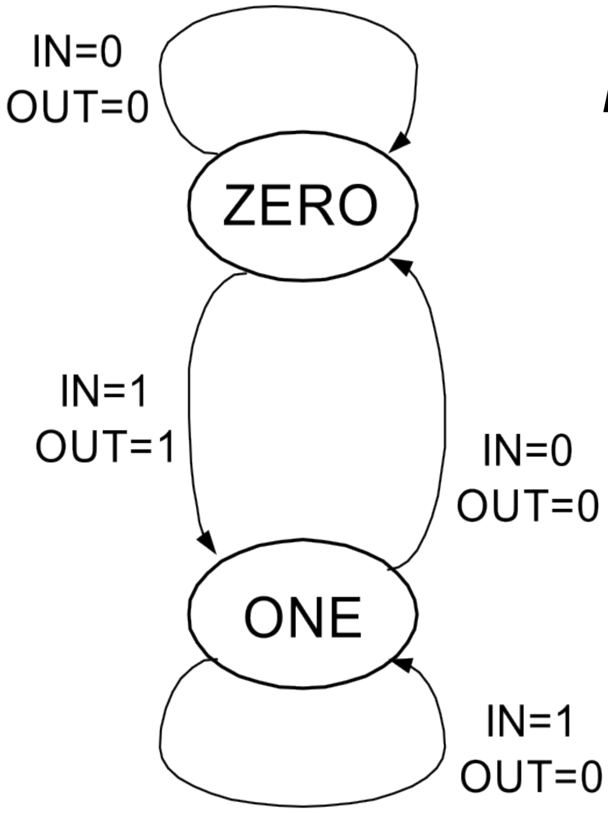
$$\begin{array}{c|cccc} \text{IN} \backslash \text{PS} & 00 & 01 & 11 & 10 \\ \hline 0 & 0 & 1 & 0 & - \\ 1 & 0 & 1 & 0 & - \end{array}$$

$OUT = \overline{PS_1}\ PS_0$



Solution B

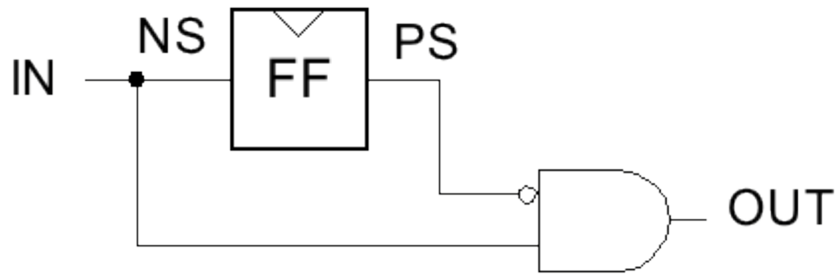
Output depends not only on PS but also on input, IN



Let ZERO=0, ONE=1

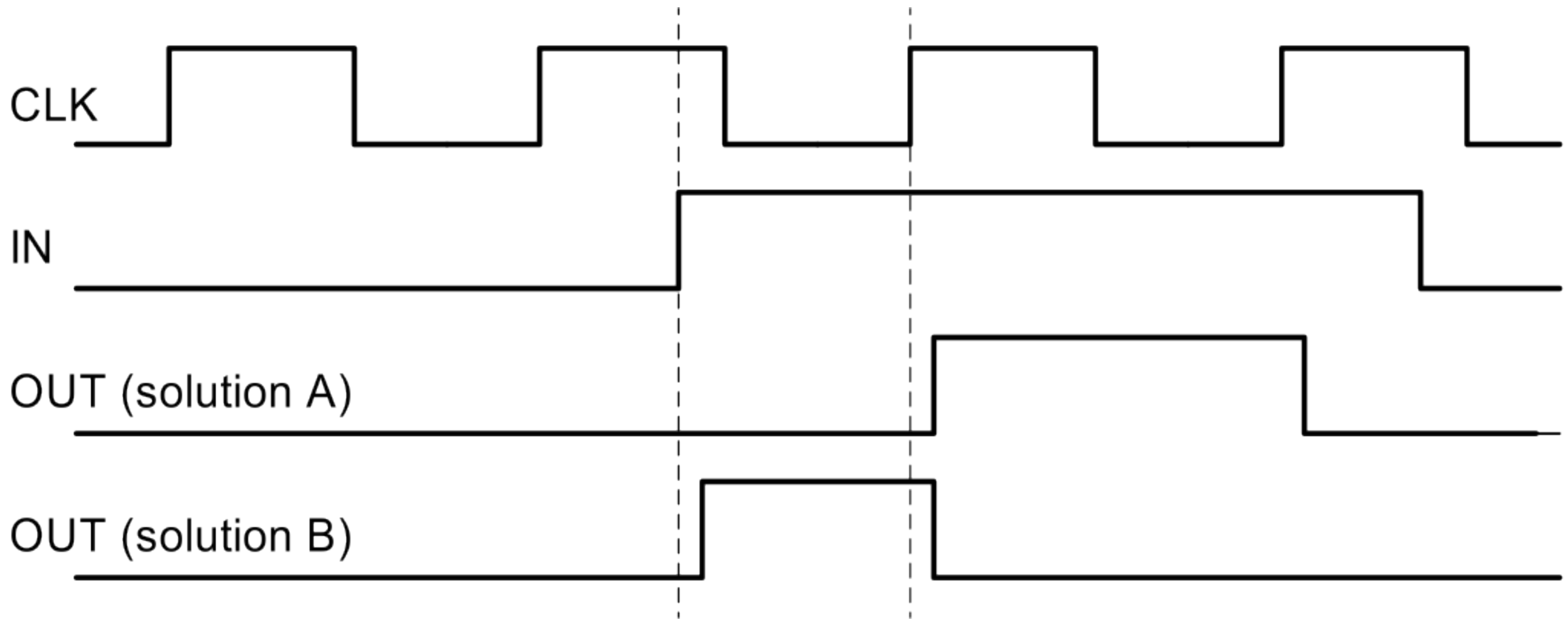
IN	*PS*	*NS*	*OUT*
0	0	0	0
0	1	0	0
1	0	1	1
1	1	1	0

NS = IN, OUT = IN PS'



What's the intuition about this solution?

Edge detector timing diagrams



- *Solution A: output follows the clock*
- *Solution B: output changes with input rising edge and is asynchronous wrt the clock.*

FSM Comparison

Solution A

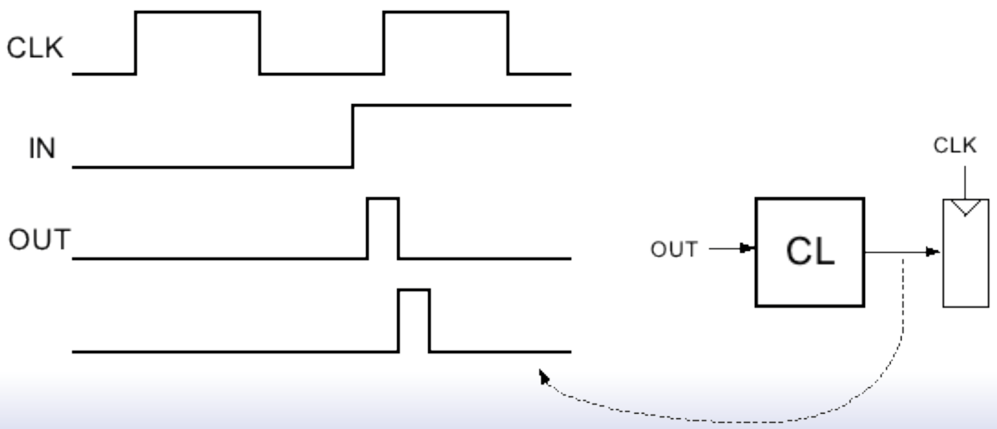
Moore Machine

- output function only of PS
- maybe <u>more</u> states (why?)
- synchronous outputs
  - no glitches
  - one cycle "delay"
  - full cycle of stable output

Solution B

Mealy Machine

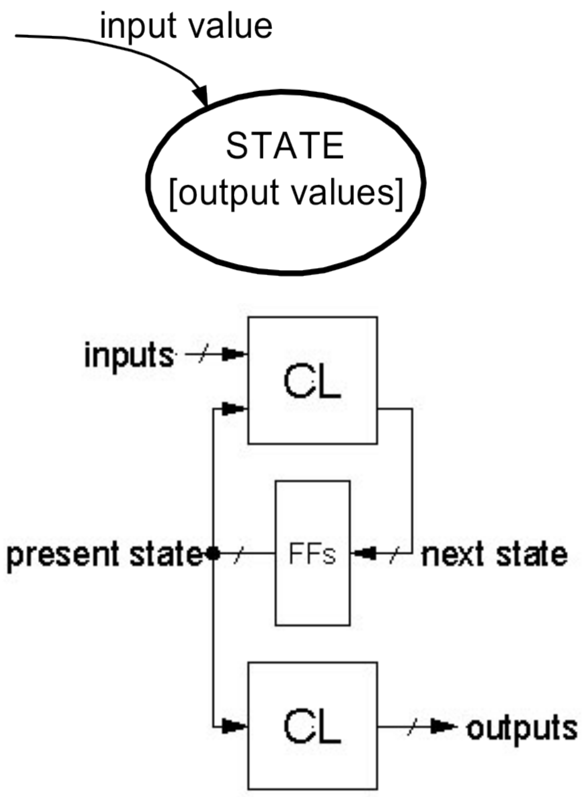
- *output function of both PS & input*
- *maybe fewer states*
- *asynchronous outputs*
  - *if input glitches, so does output*
  - *output immediately available*
  - *output may not be stable long enough to be useful (below):*



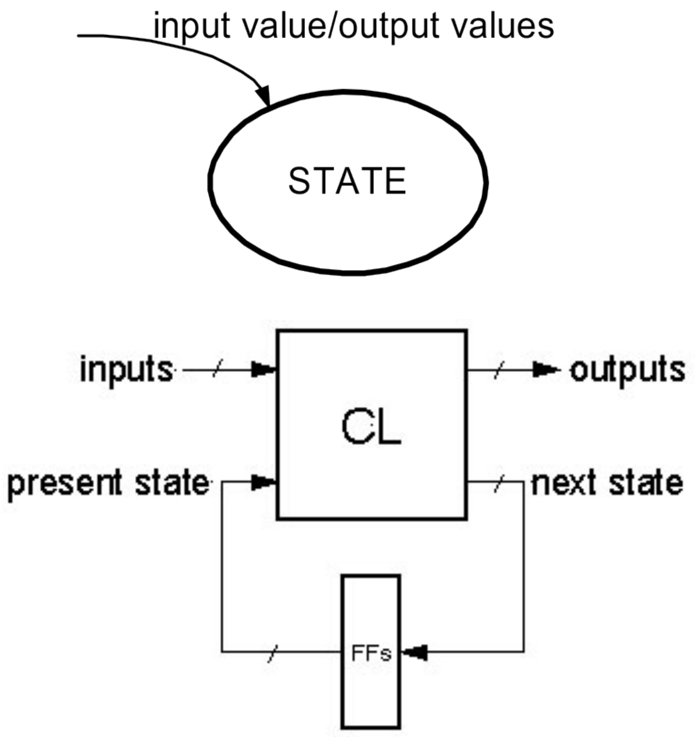
If output of Mealy FSM goes through combinational logic before being registered, the CL might delay the signal and it could be missed by the clock edge.

FSM Recap

Moore Machine



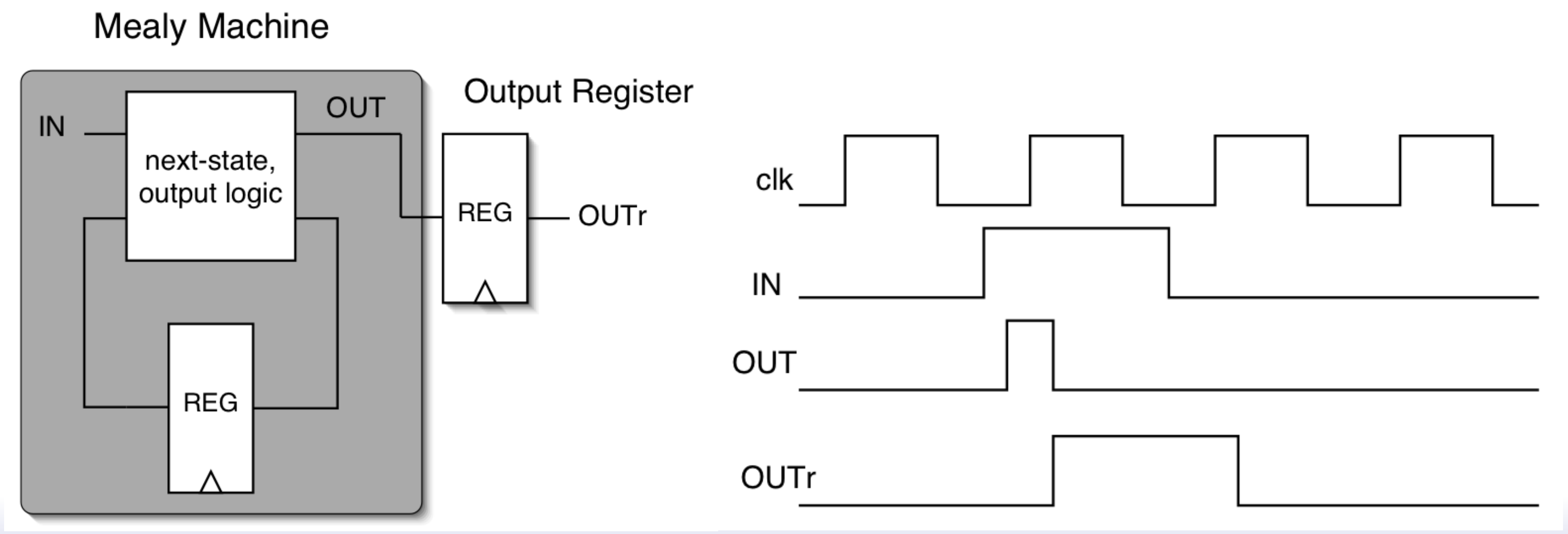
Mealy Machine



Both machine types allow one-hot implementations.

Final Notes on Moore versus Mealy

1. A given state machine could have both Moore and Mealy style outputs. Nothing wrong with this, but you need to be aware of the timing differences between the two types.
2. The output timing behavior of the Moore machine can be achieved in a Mealy machine by “registering” the Mealy output values:



FSMs in Verilog

General FSM Design Process with Verilog Implementation

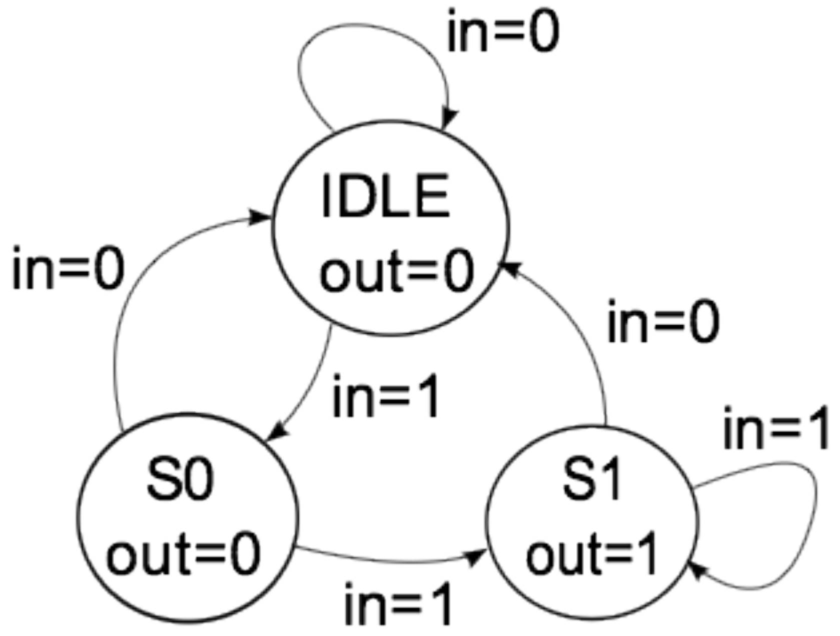
Design Steps:

1. *Specify circuit function (English)*
2. *Draw state transition diagram*
3. *Write down symbolic state transition table*
4. *Assign encodings (bit patterns) to symbolic states*
5. *Code as Verilog behavioral description*

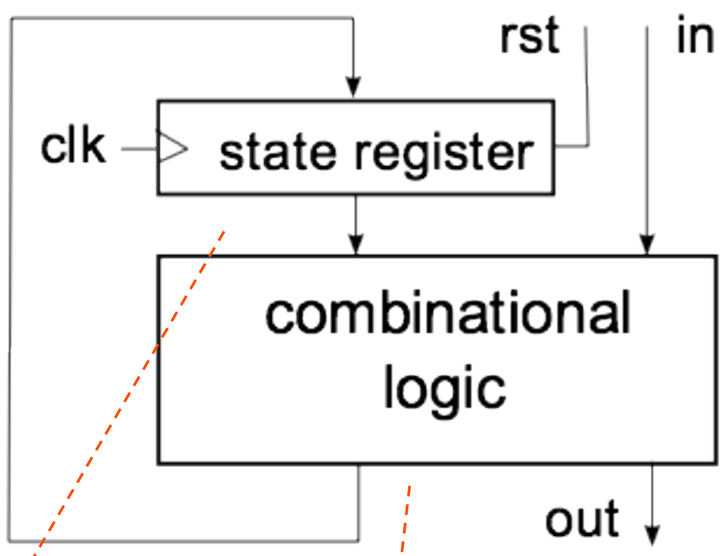
- ✓ *Use parameters to represent encoded states.*
- ✓ *Use separate always blocks for register assignment and CL logic block.*
- ✓ *Use case for CL block. Within each case section assign all outputs and next state value based on inputs. Note: For Moore style machine make outputs dependent only on state not dependent on inputs.*

Finite State Machine in Verilog

State Transition Diagram



Implementation Circuit Diagram



Holds a symbol to keep track of which bubble the FSM is in.

CL functions to determine output value and next state based on input and current state.

out = f(in, current state)

next state = f(in, current state)

What does this one do?

Did you know that every SDS is a FSM?

Finite State Machines

```
module FSM1(clk, rst, in, out);
input clk, rst;
input in;
output out;

// Defined state encoding:
parameter IDLE = 2'b00;
parameter S0 = 2'b01;
parameter S1 = 2'b10;
reg out;
reg [1:0] state, next_state;

// always block for state register
always @(posedge clk)
      if (rst) state <= IDLE;
      else state <= next_state;
```

Must use reset to force to initial state.

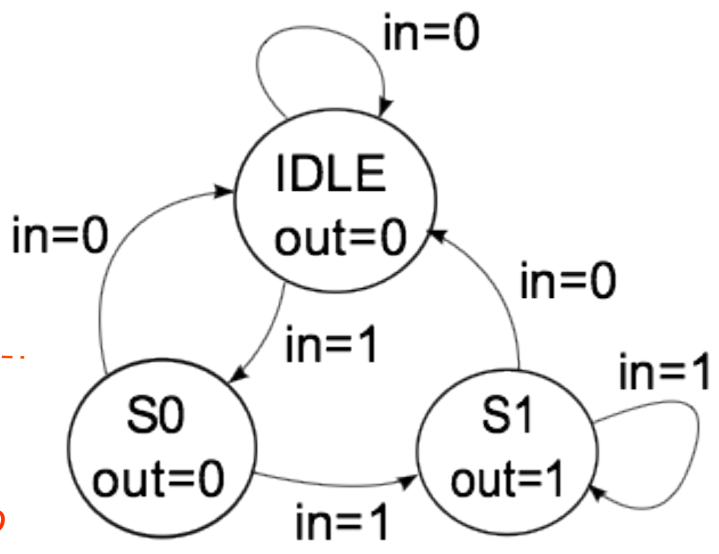
reset not always shown in STD

Constants local to this module.

out not a register, but assigned in always block

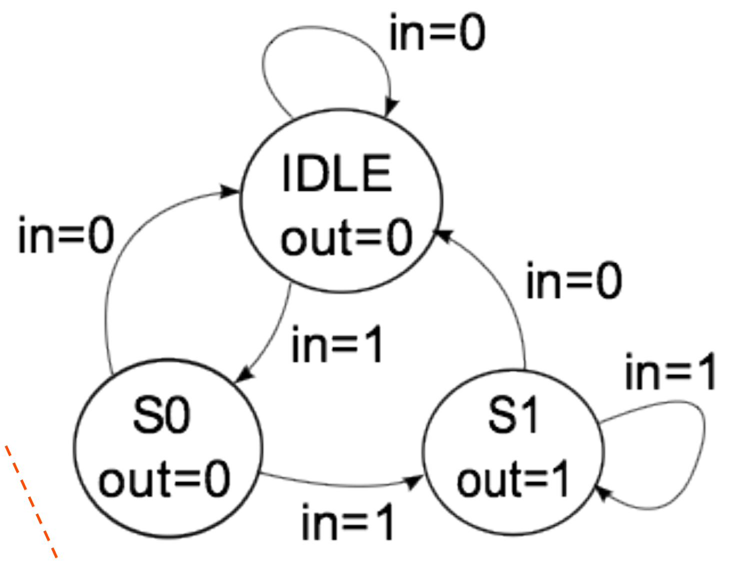
Combinational logic signals for transition.

THE register to hold the "state" of the FSM.



A separate always block should be used for combination logic part of FSM. Next state and output generation. (Always blocks in a design work in parallel.)

FSMs (cont.)



```
// always block for combinational logic portion
always @(state or in)
case (state)
// For each state def output and next
  IDLE    : begin
             out = 1'b0;
             if (in == 1'b1) next_state = S0;
             else next_state = IDLE;
           end
  S0      : begin
             out = 1'b0;
             if (in == 1'b1) next_state = S1;
             else next_state = IDLE;
           end
  S1      : begin
             out = 1'b1;
             if (in == 1'b1) next_state = S1;
             else next_state = IDLE;
         end
  default: begin
              next_state = IDLE;
              out = 1'b0;
            end
endcase
endmodule
```

Each state becomes a case clause.

For each state define:

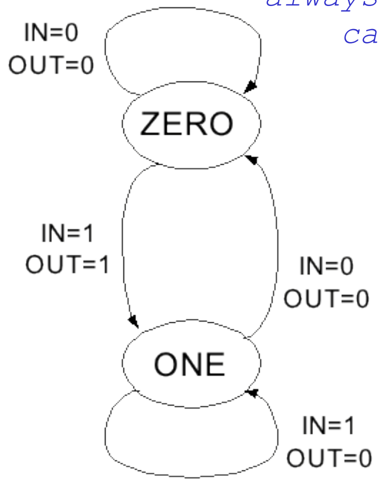
Output value(s)

State transition

Use "default" to cover unassigned state. Usually unconditionally transition to reset state.

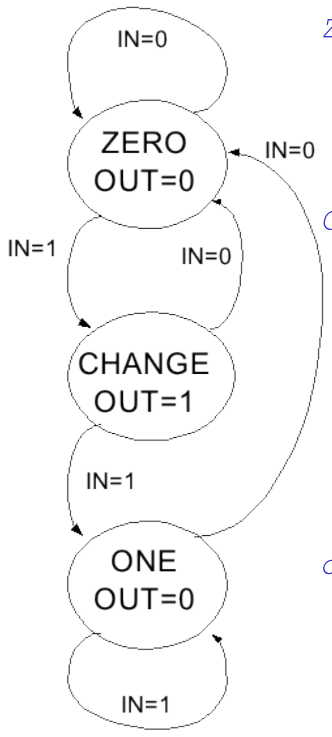
Edge Detector Example

Mealy Machine



```
always @(posedge clk)
        if (rst) ps <= ZERO;
        else ps <= ns;
always @(ps in)
    case (ps)
      ZERO: if (in) begin
              out = 1'b1;
              ns = ONE;
            end
             else begin
               out = 1'b0;
               ns = ZERO;
             end
      ONE: if (in) begin
             out = 1'b0;
             ns = ONE;
           end
           else begin
             out = 1'b0;
             ns = ZERO;
           end
      default: begin
                 out = 1'bx;
                 ns = default;
               end
```

Moore Machine



```
always @(posedge clk)
        if (rst) ps <= ZERO;
        else ps <= ns;
always @(ps in)
    case (ps)
      ZERO: begin
              out = 1'b0;
              if (in) ns = CHANGE;
               else ns = ZERO;
            end
      CHANGE: begin
               out = 1'b1;
               if (in) ns = ONE;
               else ns = ZERO;
              end
         ONE: begin
               out = 1'b0;
               if (in) ns = ONE;
               else ns = ZERO;
      default: begin
               out = 1'bx;
               ns = default;
              end
```