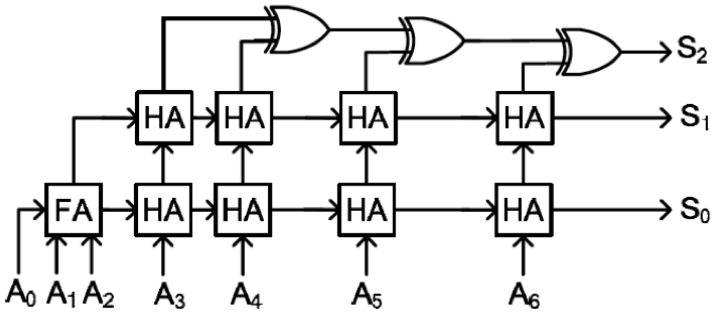
University of California at Berkeley
Department of Electrical Engineering and Computer Science

EECS150/EE141/EE241A, Fall 2014

# Homework 7: Adders and Multipliers

*Due: Friday Oct 31, 5pm*

Please include your name, SID and specify either CS150, EE141 or EE241A at the top of your homework handin. Homeworks must be submitted electronically as a single file in PDF format.




1. (a) Explain the functionality of the circuit shown above. (FA stands for full-adder, HA stands for half-adder)
   (b) What is the critical path of the circuit? You may assume that each of the FA, HA and XOR blocks have a delay equal to $t_{gate}$. Show the critical path on the schematic
   (c) Design a circuit with exactly the same functionality but shorter critical path. You are allowed to use FA, HA and XOR blocks

2. (a) Design the following logic blocks at a gate level. You may draw the gates or write the Boolean functions. Review your notes or the textbook to determine what goes inside each block. There are also numerous resources available online about these logarithmic adders. Use the given inputs and outputs as hints.

   (b) Using the logic blocks you designed in part A, design a 12-bit logarithmic adder with a carry input and a carry output. Use a radix-2 Kogge-Stone implementation. What is the critical path of your design? Give a block-level estimate, assuming that more complex blocks have more delay

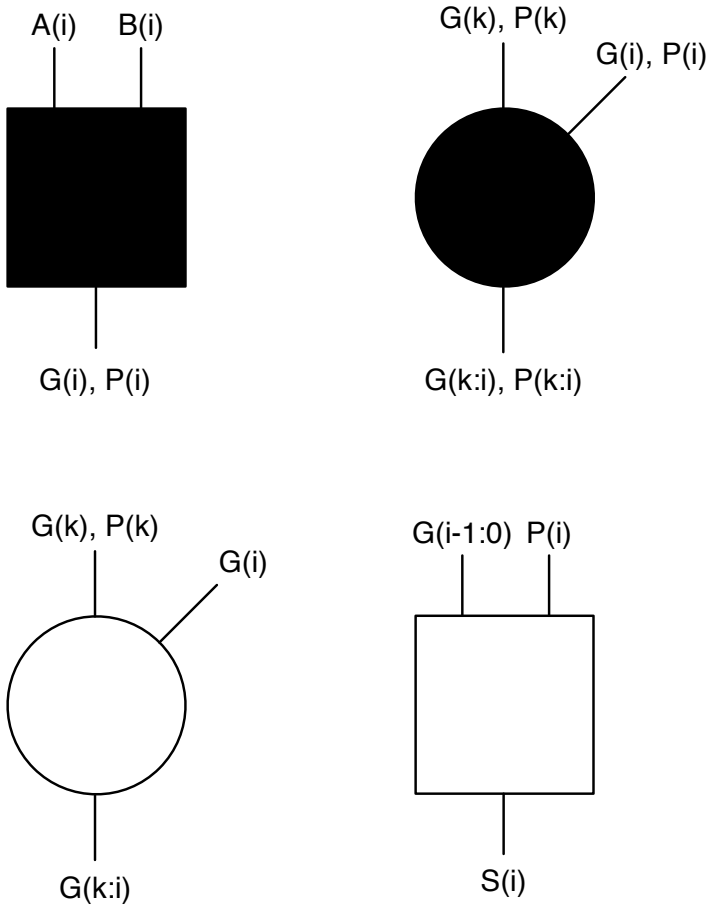



Figure 1: Diagram for question 2

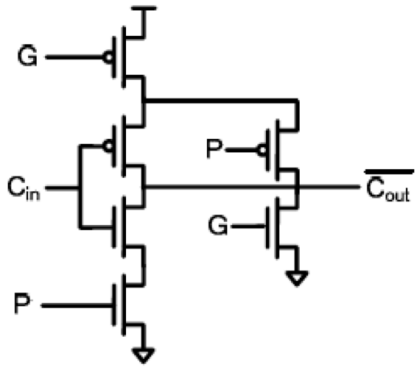
3. For a carry-select adder, assume that the select groups are all of the same number of bits, and the carry delay through a full-adder cell is equal to the delay of a 2-to-1 mux.
   (a) What is the optimal size select group for a 32-bit adder?
   (b) What is the optimal size select group for a 64-bit adder?

4. (a) Draw a wallace tree for a 5 x 5 multiplier, using Full Adder, and Half Adder cells
   (b) Add one pipeline stage to improve the throughput as much as possible. What is the new critical path?

5. Make a table comparing array, sequential, and bit-serial multipliers with respect to cost in terms of FA cells, cost in terms of FFs, and delay, all as a function of n, the number of bits in the inputs. Use "big O" notation.

6. **For EE241A only:**

(a) Shown below is a static CMOS implementation of a gate that computes the carry-out at a particular bit position. If the P signal fed into the gate is calculated using $P = A + B$ (instead of $P = A \oplus B$, which is usually the case) would the output of this gate still be correct? Why or why not? If not, suggest a modification that gives the right output.




(b) Show the static CMOS implementation of a gate that computes the sum at a particular bit position ($S = P \oplus C_{in}$). Again, if the P signal fed into the gate is calculated using $P = A + B$, is the output of the gate correct? Why or why not? If not, suggest a modification that gives the right output.

(c) The gate shown below is a Manchester carry chain implementation that computes the carry-out for two bit positions. Does this gate give the correct output if $P = A + B$? Why or why not?