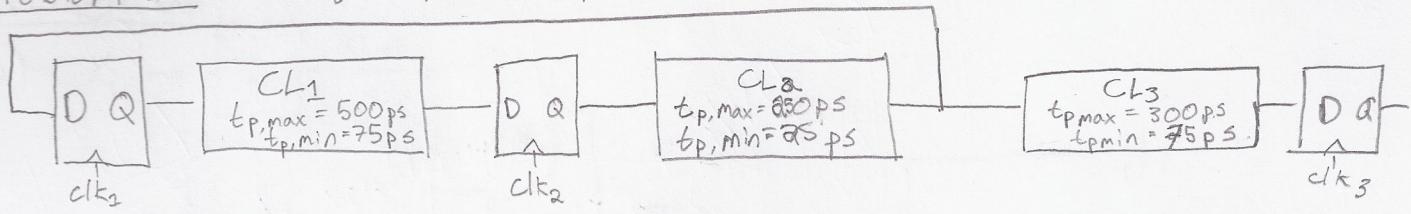


Homework 11

Kevin Chan
23816929
cs150-lbd

Problem 1 $t_{clk-q} = 50\text{ps}$ $t_{setup} = 100\text{ps}$ $t_{hold} = 100\text{ps}$



a) no clock skew

$$T_{clock} > T_{clk-q} + T_{logic,max} + T_{setup} = (50\text{ps}) + (300\text{ps}) + (250\text{ps}) = 700\text{ps}$$

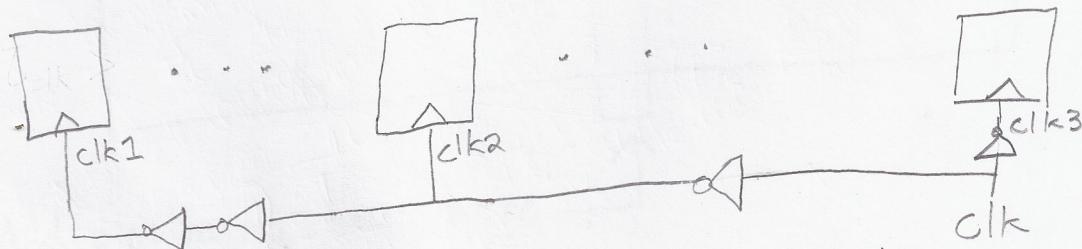
hold time: $T_{hold} < T_{clk-q,min} + T_{logic,min}$ ← condition for no violation

$$\text{since } T_{clk-q,min} + T_{logic,min} = 50\text{ps} + 25\text{ps} = 75\text{ps} \leq T_{hold} = 100\text{ps}$$

there is a hold time violation.

$$T_{hold} \nless T_{cq} + T_{logic,min}$$

b) $T_{inv} = 50\text{ps} \pm 5\text{ps}$



clk2 and clk3 are delayed by at most 55ps each.

clk1 has a maximum delay of 110ps (2 inverters)

$$\begin{aligned} \text{critical path} &= T_{cq} + T_{logic,max} + T_{setup} + T_{skew,max} \\ &= 50\text{ps} + 500\text{ps} + 100\text{ps} + 110\text{ps} = 760\text{ps} \end{aligned}$$

$$T_{clk} > 760\text{ps}$$

c) condition: $t_{hold} + t_{skew} < t_{cq,min} + t_{logic,min}$

$$\text{but } t_{hold} + t_{skew} = 100 + 110 \nless 50\text{ps} + 25$$

so we must add a delay to logic block #2 in order to avoid a race. The minimum delay necessary is

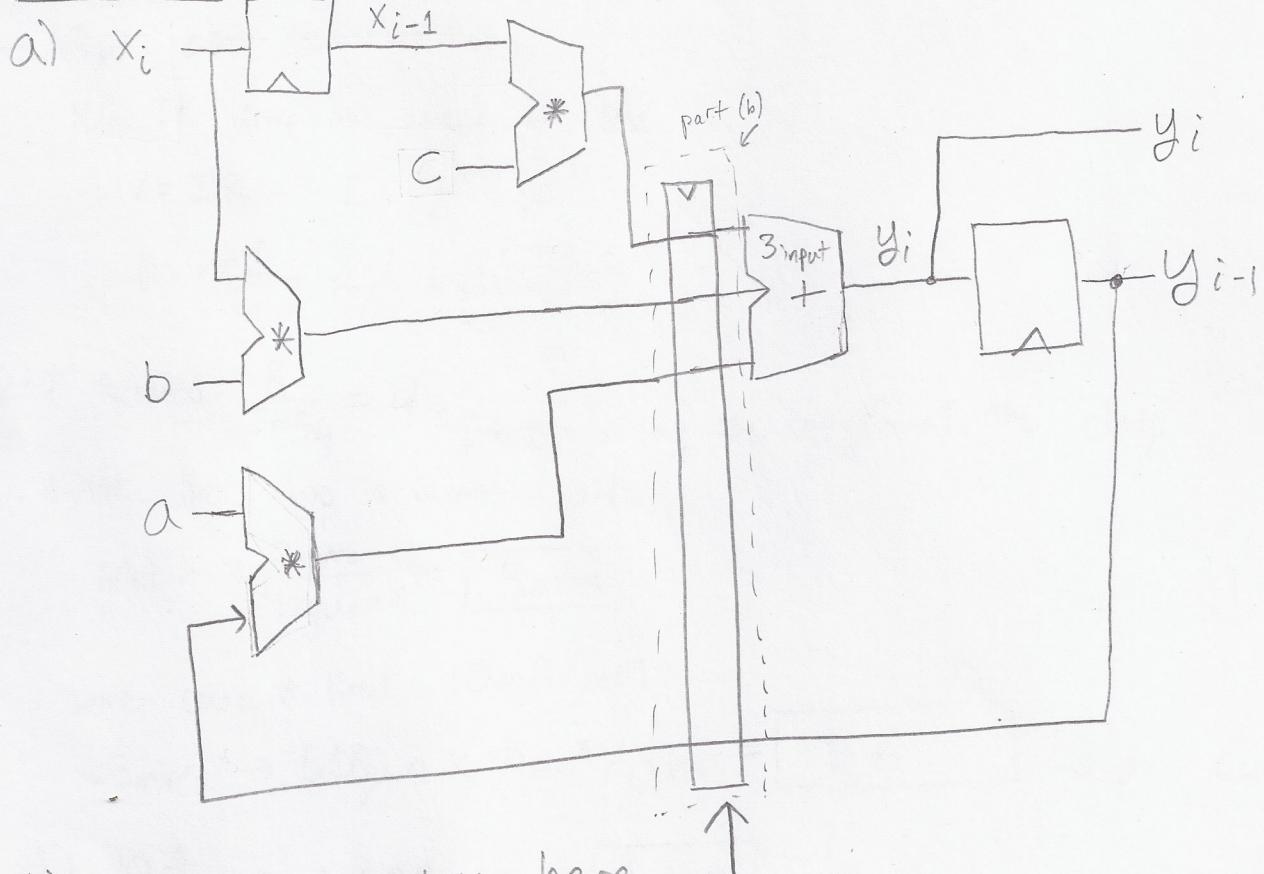
$$\begin{aligned} 210 - 50\text{ps} - 25\text{ps} &= t_{hold} + t_{skew} - T_{cq} - T_{logic,min} \\ &= 135\text{ps} \end{aligned}$$

$$t_{delay} \geq 135\text{ps}$$

Add the delay between register 1 & 2

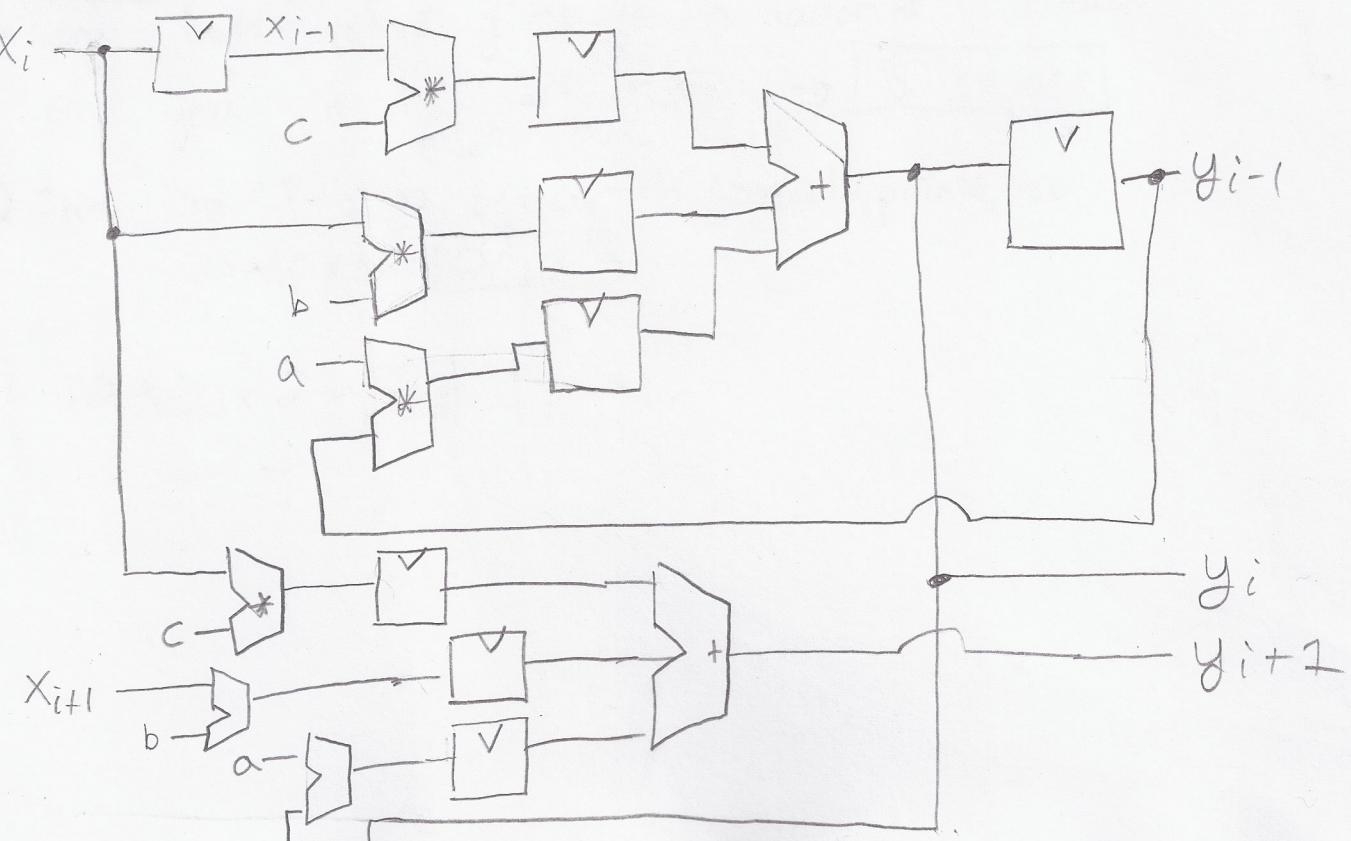
$$y_i = a*y_{i-1} + b*x_i + c*x_{i-1}$$

Problem 2



b) Add pipeline registers here

c) $y_{i+1} = a*y_i + b*x_{i+1} + c*x_i$



Problem 3

a) 12W CPU @ $1.2V = V_{dd}$

$$10\% \text{ IR drop} \rightarrow 1 + 1.2V = 1.2V$$

$$1.2V = IR \quad I = \frac{12W}{1.2V} = 10A$$

$$R = \frac{1.2V}{I} = \frac{1.2V}{10} = 12m\Omega$$

b) # squares = $\frac{R}{3m\Omega/\text{sq}} = 4$ squares along the length of the chip
since the chip is 2mm wide,

$$\text{width} = \frac{2\text{mm}}{4 \text{ squares}} = .5\text{mm}$$

c) wire current limit $10\text{mA}/\mu\text{m}$

$$.5\text{mm} \rightarrow 500\mu\text{m} \times 10\text{mA}/\mu\text{m} = 55\text{A} \rightarrow \text{Max current}$$

$$d) \frac{10A}{10\frac{\text{mA}}{\mu\text{m}}} = 1000\mu\text{m} = 1\text{mm}$$

Problem 4

a) Every buffer stage gives you a factor of 4 increase
so you need $4^5 = 1024 \rightarrow 5 \text{ stages}$

b) There are 8 stages between the diagonal points, so

$$.05 \times 50 \times 8 = 20\text{ps}$$

c) $.05 \times 50 \times 2 = 5\text{ps}$