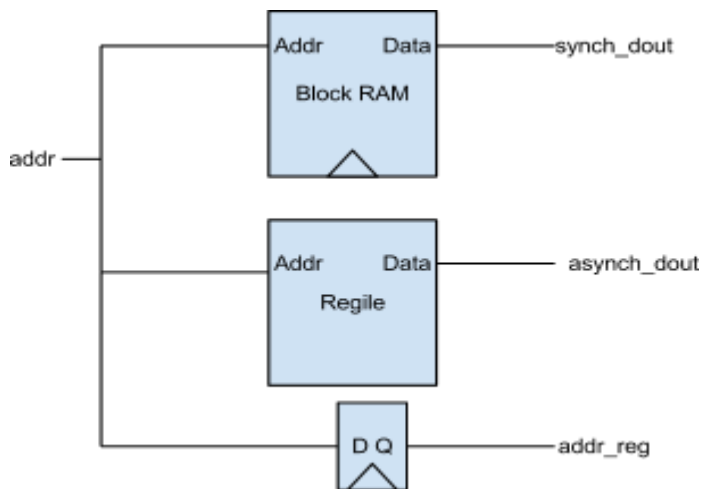**CS 150 Lab 3 Prelab**
Fall 2012
Read section 2 of the lab document and complete these questions before attending your lab section.

1 Synchronous vs. Asynchronous Read

The Block RAMs that you will use in this lab (and throughout the project) are synchronous read and synchronous write. On the other hand, the register file you will build in the project has an asynchronous read and synchronous write. Consider the hypothetical datapath above, where both the register file and the block ram have the same contents and receive the same address. Complete the timing diagram below:
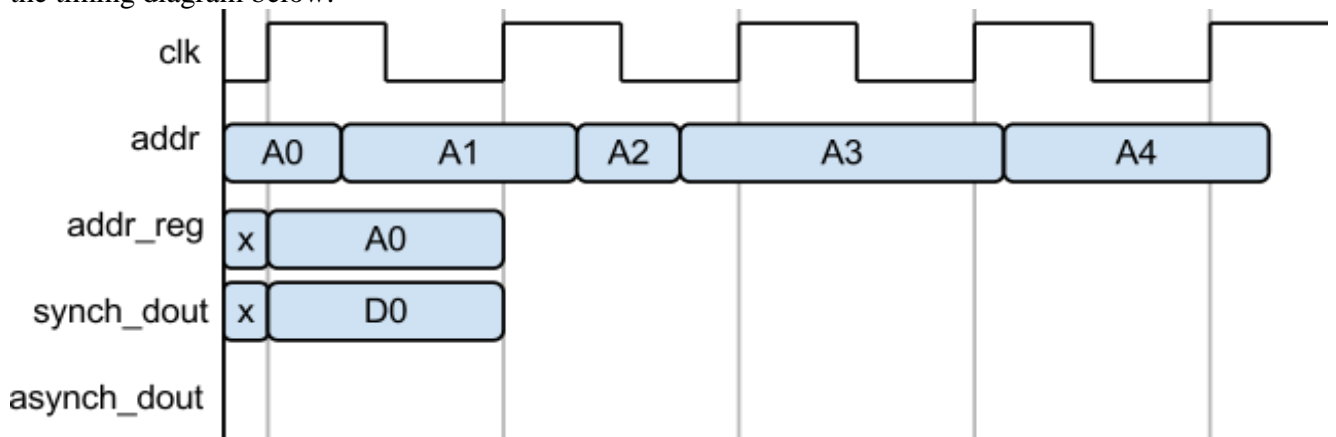
Imagine you need to implement logic that depends on the data and the address it was loaded from. Which address would you use with `synch_dout`? Which with `asynch_dout`?

2 Example List

The skeleton files include a memory initialization vector representing a linked list to use while debugging your processor. The contents of the file are reproduced below (in hexadecimal). What list does this represent, and what is the sum of the elements in the list? In the lab, you will need to use this information to debug and verify your list processor.

```
00000001
00000008
00000004
00000004
00000005
0000000e
00000003
00000002
00000002
00000006
00000007
0000000c
00000008
00000000
00000006
0000000a
```

3 Control Signals

Section 2 of the lab document shows one possible way to store the list {1,2,3} in memory. Fill in the table of control signals and expected data signals to sum this list using the datapath given in section 2.3 of the lab document. Write 'x' when you don't care about the signal and use as few cycles as possible to sum the list.

	rst	addr_sel	wr_en	alu_op	Block RAM dout	accum_result
0	1	x	x	x	x	0x00000000
1	0				0x00000001	
2						
3						
4						
5						
6						
7						