Kevin He

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Education

University of California, Berkeley August 2021 – December 2024

Bachelor of Art, Computer Science *GPA: 3.97/4.0*

- **Coursework**: Data Structures, Algorithms, Operating Systems & System Programming, Programming Languages & Compilers, Computer Architecture, Digital Design & Integrated Circuits, Advanced Digital Circuits & Systems (Graduate), Hardware for Machine Learning (Graduate), Tapeout, Databases, Internet Architecture

Work Experience

Apple Cupertino, CA

CPU Performance Intern *May 2024 – August 2024*

- Annotated major microarchitecture structures and events in Apple's state of the art CPU branch predictors for RTL vs. C++ performance model correlation
- Built new Verilog and performance verification infrastructure for mapping branch predict and train events
- Developed Python tools to parse microarchitecture event logs and quickly extract predictor analytics and identify performance anomalies, significantly reducing initial debugging time to identify issues in waveform dumps

Apple Austin, TX

GPU RTL Design Intern *May 2023 – August 2023*

- Implemented RTL bug fixes in GPU and analyzed performance impacts of fixes
- Designed and formally verified a new, reusable, parameterized, low-area SRAM FIFO module for the IP library
- Analyzed performance and area of GPU IP library blocks and developed Python and TCL scripts to quickly identify configurations and users of library blocks

Amobee Redwood City, CA

Software Engineering Intern *May 2022 – August 2022*

- Developed backend software to record auto-allocated budget data for demand-side digital advertisement bidding
- Built a new data pipeline with Protobuf to serialize and store log records in Hadoop HDFS and Apache Druid database for fast SQL querying. Used Apache Spark on Zeppelin notebooks to analyze the new data.
- Built a new graphical Flask display app with Dash and REST API queries to help engineers and data scientists quickly view the performance of their auto budget allocation machine learning models

Research

Berkeley SLICE Lab *February 2023 – present*

- **uArchDB**: Developing an extensible graph-based microarchitecture event logger for debugging open-source processors
- Designed a CHISEL RTL widget for annotating events and Python parsing script to reconstruct instruction execution traces. Currently integrating tool into Chipyard hardware design framework.
- Annotated Sodor and Rocket in-order CPUs and Gemmini DNN accelerator
- Poster / Slides / github.com/ucb-bar/iris-event-utils
- **DiffSampler**: Investigating gradient descent for circuit SAT solving with applications in design verification

Publications:

- **High-Throughput SAT Sampling**
  Arash Ardakani, Minwoo Kang, **Kevin He**, Qijing Huang, John Wawrzynek
  Design, Automation and Test in Europe Conference 2025
- **DEMOTIC: A Differentiable Sampler for Multi-Level Digital Circuits**
  Arash Ardakani, Minwoo Kang , **Kevin He**, Vighnesh Iyer, Suhong Moon, John Wawrzynek
  Asia and South Pacific Design Automation Conference 2025
- **Late Breaking Results: Differential and Massively Parallel Sampling of SAT Formulas**
  Arash Ardakani, Minwoo Kang , **Kevin He**, Vighnesh Iyer, Suhong Moon, John Wawrzynek
  Design Automation Conference 2024

Projects

RISC-V Vector Core Tapeout *January 2024 – May 2024*

- Integrated a multicore RVV1.0 spec-compliant vector processor on Intel16 FinFET process on a 2x2mm SOC with L2 banks, ring NoC, and machine learning accelerators for tapeout
- Synthesized, placed & routed design at 900 mhz. Produced DRC and LVS clean GDS for vector cores and integrated blocks into top level SoC. Chip arrived and currently bringing up design.
- Developed RISC-V quantized matmul vector kernels for benchmarking and conducted extensive design space exploration of vector core configurations

Teaching

EECS151: Intro to Digital Design Teaching Assistant *January 2024 – May 2024*

- Taught class of 90 students and ASIC design lab section with weekly labs assignments and a final project, where students build a 3-stage RISC-V CPU with L1 cache in Verilog
- Gave presentations, helped students with debugging, office hours, and answering online questions. Managed website.
- Subjects taught include CMOS, Verilog, waveform debugging, digital logic design, power, logic delay, VLSI design flow

Hands on PCB Design DeCal Instructor *August 2022 – December 2023*

- Taught a 75-person introductory electrical engineering course on designing PCBs from schematic to programming
- Topics included component selection, designing schematics, footprints and layouts, microcontrollers, PCB manufacturing, soldering, testing, and programming
- Guided students through weekly hands-on labs and a final project, where students design and assemble their own microcontroller-based PCB from scratch

Skills

Python, C/C++, Java, SQL, Rust, OCaml, HTML/CSS, RISC-V, x86, ARM, Verilog/SystemVerilog, CHISEL, Git