WASHINGTON STATE UNIVERSITY
SCHOOL OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

EE 352, ELECTRICAL ENGINEERING LABORATORY

LAB #3

Operational Amplifier Applications

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Lab Overview

The lab demonstrated several use-cases of operational amplifiers. The first experiment used the OP27 op amp to double the voltage of high frequencies and attenuate low frequencies. Next, cascading amplifiers were used in a design featuring a high gain output, with low output resistance and a high input resistance.

1 First Order High Pass Active Filter

1.1 Purpose

The purpose of this experiment was to implement an active high-pass filter using an OP-27 op-amp and an RC circuit. The circuit would be used to amplify high frequency signals to $6\,\mathrm{dB}$ and attenuate low frequency signals.

1.2 Theoretical background

Op amps are often used in filtering applications, and has several advantages over passive filters. In this experiment, we will construct an active filter using the OP-27 amplifier. The filter will be a high-pass type and is shown below in Figure 1.

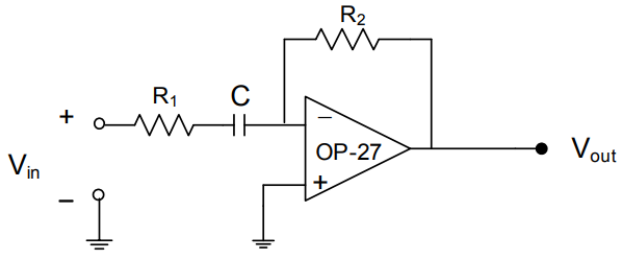


Figure 1: The active filter circuit used in this experiment.

Time domain

In the time domain, we can characterize this circuit using a differential equation. If we assume an ideal op amp and perform KCL along the top current, we can say that the input current across the capacitor is equal to the feedback current, across R_2. The relationship between V_{out} and V_{in} becomes,

$$\frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}t} + \frac{1}{R_1 C} V_{\text{out}} = -\frac{R_2}{R_1}\frac{\mathrm{d}V_{\text{in}}}{\mathrm{d}t} \tag{1}$$

The solution to (1) are a real or complex exponential, depending on the input voltage. For a real exponential, where the input voltage is constant, such as with a step response, the function will have a time constant τ of

$$\tau = R_1 C \tag{2}$$

Phasor domain

Using phasors, we can treat each element with their corresponding impedances and determine the amplitude response. This greatly simplifies the analysis. The input and feedback impedance become

$$Z_{\text{in}} = R_1 + \frac{1}{j\omega C} \tag{3a}$$

$$Z_{\text{fb}} = R_2 \tag{3b}$$

If we again assume an ideal op amp with zero input current, we can simply use KCL and KVL, then would find the amplifier's gain,

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_2}{R_1 + \frac{1}{j\omega C}} \tag{4}$$

For the amplitude only, we can take the magnitude of the gain,

$$\frac{|V_{\text{out}}|}{|V_{\text{in}}|} = \frac{\omega R_2 C}{\sqrt{1 + \omega^2 R_1^2 C^2}} \tag{5}$$

If we take the limits of the frequency, at $\omega = 0$, the low frequency (DC) gain is zero. At higher frequencies, $\omega \to \infty$, the gain is proportional to R_2/R_1. This indicates that the circuit is correctly acting as a high-pass filter with an additional gain.

Cutoff frequency

The cutoff frequency can be determined using both the time and phasor domain. From the time domain, the cutoff frequency is given by the inverse of (2). In the phasor domain, we can determine the cutoff frequency using (4). From inspection, we can see the denominator of the gain must equal $\sqrt{2}$,

$$\begin{aligned} \frac{|V_{\text{out}}|}{|V_{\text{in}}|} &= \frac{1}{\sqrt{2}} \\ 1 + \omega_0^2 R_1^2 C^2 &= 2 \\ \omega_0 &= \frac{1}{R_1 C} \end{aligned} \tag{6}$$

Amplifier design

The amplifier design had three requirements: (1) an input resistance of $R_1 = 10\,\text{k}\Omega$, (2) a high frequency gain of $6\,\text{dB}$, and lastly (3) a cutoff frequency of $300\,\text{Hz}$. In order to meet these requirements, the values of C and R_2 must be chosen accordingly. For a cutoff frequency of $300\,\text{Hz}$, we can use (6) to determine the required capacitance

$$\begin{aligned} \omega_0 &= \frac{1}{R_1 C} = 2\pi\,(300\,\text{Hz}) \\ C &= \frac{1}{2\pi\,(10\,\text{k}\Omega)\left(300\,\text{s}^{-1}\right)} \\ &= 53.1\,\text{nF} \end{aligned}$$

The value of R_1 can be determined from the $6\,\text{dB}$ requirement and by taking the high frequency limit of (5),

$$\begin{aligned} 6\,\text{dB} &= 2\,\text{V/V} = R_2/R_1 \\ R_1 &= 2\,(10\,\text{k}\Omega) \\ &= 20\,\text{k}\Omega \end{aligned}$$

With these values, the circuit can easily be simulated in PSPICE and the requirements can be verified, shown by the Bode plot in Figure 7 (Appendix).

1.3 Procedure

The follow steps were carried out, as instructed by the lab assignment.

1. The circuit shown in Figure 1 was constructed.
   (a) The IC pinout, shown in Figure 8 (Appendix), from the OP27 datasheet was used.
   (b) The Rigol DP832 was used to create a $12\,\mathrm{V}$, $-12\,\mathrm{V}$, and $0\,\mathrm{V}$ ground supply for the OP-27.
   (c) The $12\,\mathrm{V}$ and $-12\,\mathrm{V}$ was attached to pin 7 and 4 of the OP-27 respectively.
   (d) The input signal V_{in} was generated by the function generator and attached to pin 2.
   (e) The circuit was verified correct by the TA.
2. To experimentally see the step response, a $1\,\mathrm{V_{pp}}$ square wave was generated with a $0.5\,\mathrm{V}$ offset and attached to V_{in} of the circuit. The frequency was initially set to $300\,\mathrm{Hz}$ and was reduced to $20\,\mathrm{Hz}$ to view the response until nearly equilibrium.
3. Next, the function generator was set to use $4\,\mathrm{V_{pp}}$ sine wave output with $0\,\mathrm{V}$ offset in order to determine the frequency response. The frequency was swept from $30\,\mathrm{Hz}$ to $1\,\mathrm{MHz}$, with careful attention spent around the expected cutoff frequency of $300\,\mathrm{Hz}$. These data points were recorded in Excel and plotted.

1.4 Results and analysis

Measured component values

The measured component values are shown in Table 1. As $53\,\mathrm{nF}$ capacitors were not available, we instead chose a network of capacitors, with C_1 in series with C_2, then both in parallel with C_3. Using the individual capacitances, one would expect the equivalent capacitance to be $55.8\,\mathrm{nF}$. However, once attached to the breadboard, the capacitance was measured to be $C_{\mathrm{eq}} \approx 53\,\mathrm{nF}$. This is likely due to the stray capacitance. of the board.

Table 1: Experimental and nominal component values.

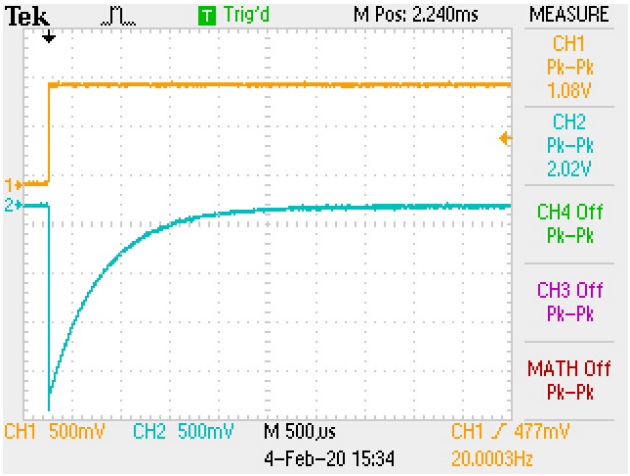
Component	Nominal	Measured	% Error (Tolerance)
R_1	$10\,\mathrm{k\Omega}$	$9.973\,\mathrm{k\Omega}$	2.70% (5%)
R_2	$20\,\mathrm{k\Omega}$	$19.40\,\mathrm{k\Omega}$	3.00% (5%)
C_1	$100\,\mathrm{nF}$	$106\,\mathrm{nF}$	6% (10%)
C_2	$100\,\mathrm{nF}$	$98\,\mathrm{nF}$	2% (10%)
C_3	$4.7\,\mathrm{nF}$	$4.85\,\mathrm{nF}$	3.2% (10%)
C_{eq}[1]	$53\,\mathrm{nF}$	$53\,\mathrm{nF}$	0% (–)

[1] Using the RLC meter, the equivalent capacitance C_{eq} was measured to be $53\,\mathrm{nF}$ on the breadboard.

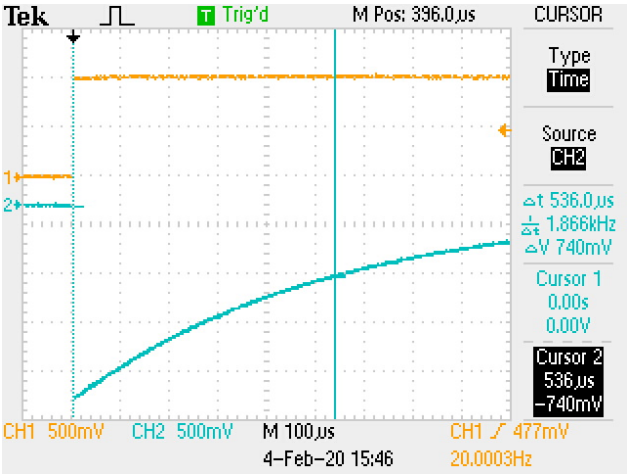
Step response

The square wave input was set to $f = 20\,\mathrm{Hz}$ and the output voltage was found to rise from $-2\,\mathrm{V}$ to $0\,\mathrm{V}$, shown in Figure 2a. Of a $2\,\mathrm{V_{pp}}$ response, the expected voltage at one time constant is $1.260\,\mathrm{V}$. However, as the output wave is inverted and offset $2\,\mathrm{V}$, the output voltage after one time constant would be $-0.740\,\mathrm{V}$. Shown in Figure 2b, cursors were used to determine the time from the trigger ($t = 0$) to reach $-0.740\,\mathrm{V}$, $\Delta t = \tau = 536.0\,\mu\mathrm{s}$.

Using the experimental component values from Table 1, the expected time constant using (2) is $515.7\,\mu\mathrm{s}$, or an expected corner frequency of $308\,\mathrm{Hz}$. The measured time constant deviated by 3.9%. This error was relatively small, but was likely caused by the non-ideal op amp and stray impedances of the breadboard and wires.



(a) A broad (5 ms) view of the step response.



(b) Using cursors to identify the approximate time constant τ.

Figure 2: Step response of the high-pass op amp circuit.

Frequency response

The approximate frequency response was found by measuring the output voltage using the oscilloscope at a range of frequencies, from 30 Hz to 1 MHz. This data was plotted using Excel, shown in Figure 3 below. Around the expected corner frequency of 300 Hz, additional points were taken to find the experimental cutoff frequency. It was found that 312 Hz led to a gain of 2.98 dB. This was 4% from the required cutoff frequency of 300 Hz. This error was likely due to stray impedances of the breadboard.

Additionally, near the limits of the op amp, there is a slight uptick in the gain. It nominally should be 6 dB, however, it experiences nearly 6.5 dB near 125 kHz. This seems to be a second order effect, likely caused by the impedances of the breadboard or oscilloscope probes, or non-ideal characteristics of the function generator.

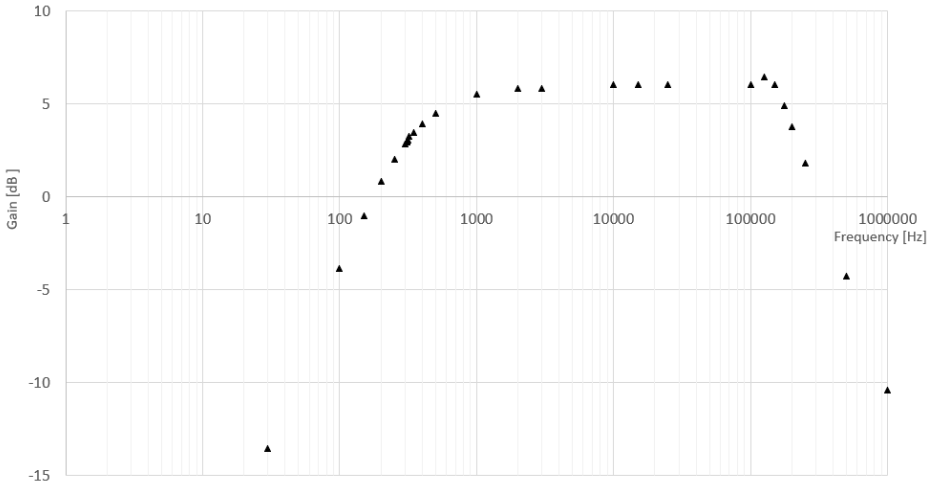


Figure 3: Experimental frequency response of the active high-pass op amp.

1.5 Conclusion

This experiment demonstrated an active high pass filter, enabling high frequencies to be amplified while attenuating lower frequencies. The time constant and cutoff frequency can be determined experimentally using both a step response, as well as the phasor frequency response.

2 High gain amplifier

2.1 Purpose

This experiment involved designing a high gain amplifier using components from the previous experiment. It should have a high input resistance and low output resistance.

2.2 Theoretical background

In this experiment, we are given specifications for an amplifier and our circuit must meet or exceed these specifications:

1. Input: 6–20 mV (peak-to-peak), 10 kHz sine wave.
2. Total gain: $1000\,\mathrm{V/V}$, $\pm 2\%$.
3. Output: $1000\times$ input, 10 kHz sine wave; minimal phase shift.
4. Input resistance: $\geq 1\,\mathrm{M\Omega}$.
5. Output resistance: $\leq 10\,\Omega$.
6. Must use the OP27 op-amp.
7. Must use a single DC power supply.

As the open-loop gain at the required frequency is roughly $1000\,\mathrm{V/V}$[1], it's clear that at least two OP27 op amps must be cascaded. Amplifiers can be cascaded to create a multi-stage amp with mixed characteristics of each amplifier and a total gain equal to the product of individual gains. Figure 4 shows an example of two cascaded amplifiers, each with an individual gain. With these amplifiers, the net gain can be found as the product of each amplifier's gain, $A_1 A_2$.

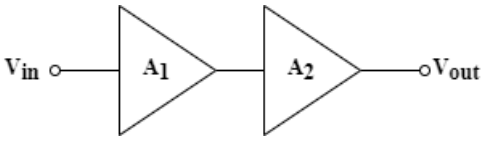


Figure 4: An example of a cascaded amplifier.

Since the phase shift must be minimized, we can either use two inverting amplifiers or simply use non-inverting amplifiers. Additionally, as the input resistance is required to be high ($\geq 1\,\mathrm{M\Omega}$) it seems that a non-inverting amplifier would be the best option, as an ideal non-inverting amplifier configuration has an infinite resistance. There are several combinations of two or three non-inverting amplifiers that can be used to achieve the $1000\,\mathrm{V/V}$ goal. A few options are considered are:

$$
\begin{aligned}
G_1 &= 10 \times 100 \\
G_2 &= 10 \times 10 \times 10 \\
G_3 &= 20 \times 50 \\
G_4 &= 25 \times 40
\end{aligned}
$$

The third option, $A_1 = 20$ and $A_2 = 50$, was chosen as it was used as the example in-class and had a straight-forward calculation. To achieve this, we can use the gain for a non-ideal non-inverting op amps and approximate the gain to

$$
G \equiv \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1 + R_2/R_1}{1 + \frac{1+(R_2/R_1)}{A}} \tag{7a}
$$

$$
G \approx \frac{1 + R_2/R_1}{1 + \frac{R_2/R_1}{A}} \tag{7b}
$$

[1] *Low Noise, Precision Operational Amplifier*. OP27, Rev. F. Analog Devices. April 2006.

In OrCAD, a circuit was built with two non-inverting op amps and simulated using PSPICE, showing an ideal gain of $1000\,\mathrm{V/V}$. This circuit is shown in Figure 5. To accomplish this, four resistors were used: on the first amplifier with gain $20\,\mathrm{V/V}$, $R_1 = 1\,\mathrm{k\Omega}$ and $R_2 = 20\,\mathrm{k\Omega}$. On the second amplifier, $R_3 = 1\,\mathrm{k\Omega}$ and $R_4 = 50\,\mathrm{k\Omega}$, leading to gain of $50\,\mathrm{V/V}$.

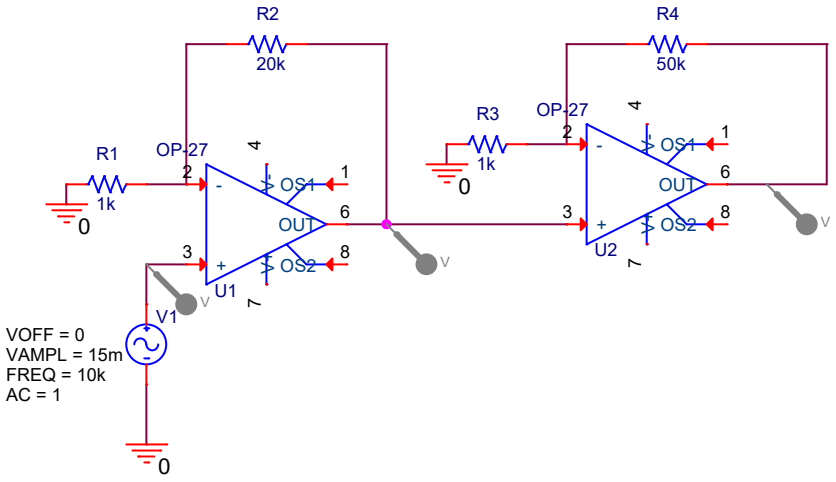


Figure 5: The cascading amplifiers used in Experiment 2.

2.3 Procedure

The follow steps were carried out, as instructed by the lab assignment.

1. The 2-stage amplifier circuit was designed, noted in the theoretical background section above.
2. The expected gains were calculated using (7b), for both the individual amplifier stages and the product of both stages. This was simulated in PSPICE.
3. The circuit was implemented on the breadboard and each amplifier stage was tested individually before they were combined.
4. The gain was tested and recorded using various input voltages within the range of the requirements.
5. The input resistance was measured using a $1\,\mathrm{M\Omega}$ sense resistor across the input. This was done by attaching a 10X probe across the resistor and calculating the current through it.
6. The output resistance was measured by using a $470\,\Omega$ resistor and later, a $10\,\mathrm{k\Omega}$ resistor on the output of the second op amp. This was done by using a similar technique to Step 5.

2.4 Results and analysis

Measured component values

The components of Figure 5 were measured and recorded in Table 2.

Table 2: Experimental and nominal component values.

Component	Nominal	Measured	% Error (Tolerance)
R_1	$1\,\mathrm{k\Omega}$	$0.9724\,\mathrm{k\Omega}$	2.76% (5%)
R_2	$20\,\mathrm{k\Omega}$	$19.454\,\mathrm{k\Omega}$	2.73% (5%)
R_3	$1\,\mathrm{k\Omega}$	$1.0198\,\mathrm{k\Omega}$	1.98% (5%)
R_4	$50\,\mathrm{k\Omega}$	$48.79\,\mathrm{k\Omega}$	2.42% (5%)
$R_{\mathrm{test-in}}$	$1\,\mathrm{M\Omega}$	$0.9827\,\mathrm{M\Omega}$	1.73% (5%)
$R_{\mathrm{test-out1}}$	$470\,\Omega$	$463.3\,\Omega$	1.42% (5%)
$R_{\mathrm{test-out2}}$	$10\,\mathrm{k\Omega}$	$9.719\,\mathrm{k\Omega}$	2.81% (5%)

Amplifier stages and total gain

The gain of the individual amplifiers were tested separately before cascading. This was accomplished using an input $V_{\mathrm{in}} = 1\,\mathrm{mV_{pp}}$ at $10\,\mathrm{kHz}$. Despite some error during the individual amplifier testing, when combined, there was an exact $1000.0\,\mathrm{V/V}$ gain across the entire amplifier, as shown in Figure 6. This could be due to additional impedances in the connecting wire or the breadboard. The values and error of the stages are noted in Table 3 below.

Table 3: Ideal (nominal), predicted, and measured gain. The predicted gains are calculated using (7b) and the actual resistor values from Table 2.

Stage	Ideal	Predicted	Measured	Error
A_1	$20\,\mathrm{V/V}$	$20.77\,\mathrm{V/V}$	$20.4\,\mathrm{V/V}$	$+2.0\%$
A_2	$50\,\mathrm{V/V}$	$47.56\,\mathrm{V/V}$	$49.6\,\mathrm{V/V}$	-0.8%
A_1A_2	$1000\,\mathrm{V/V}$	$1011.84\,\mathrm{V/V}$	$1000.0\,\mathrm{V/V}$	0%

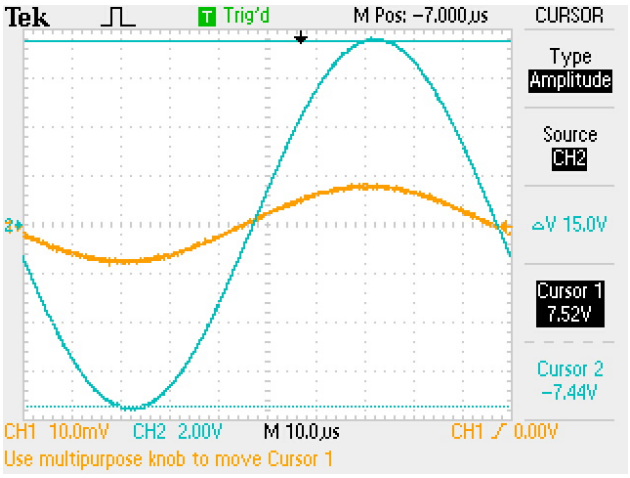


Figure 6: The measurement of the output gain showing an ideal $1000\,\mathrm{V/V}$ gain and minimal phase shift.

Input and output resistances

The voltage across the amplifier was found to be $11.2\,\mathrm{mV}$. Using a voltage divider, with $R_{\mathrm{test-in}}$ in series with the input amplifier, the input resistance can be calculated as,

$$\begin{aligned} V_{\mathrm{div}} &= \frac{R_{\mathrm{in}}}{R_{\mathrm{test-in}} + R_{\mathrm{in}}} V_{\mathrm{in}} \\ R_{\mathrm{in}} &= \frac{R_{\mathrm{test-in}}}{V_{\mathrm{in}}/V_{\mathrm{div}} - 1} = \frac{0.9827\,\mathrm{M\Omega}}{20.0/11.2 - 1} \\ &= 1.25\,\mathrm{M\Omega} \end{aligned}$$

Using the $470\,\Omega$ resistor, the output voltage dropped significantly from the open-circuit voltage $V_{\mathrm{OC}} = 10.0\,\mathrm{V}$ to $9.36\,\mathrm{V}$. This is likely because the op amp was unable to supply the needed current ($\approx 20\,\mathrm{mA}$). This is evident by viewing Figure 24 in the OP27 datasheet (excerpt provided in the Appendix). This figure shows at loads under $1\,\mathrm{k\Omega}$, the op amp is unable to supply the maximum output voltage of $\pm V_s$. Only once it exceeds a load of $1\,\mathrm{k\Omega}$ does the maximum output voltage (and current) become linear and under this load resistance value, the region is non-linear and drops substantially. This demonstrates the need for a higher load resistance.

As recommended during the lecture, this resistor was switched out for a $10\,\mathrm{k\Omega}$. Using the standard voltage divider, we can determine the output resistance R_{out} as

$$\begin{aligned} R_{\mathrm{out}} &= R_{\mathrm{test-out}} \left(\frac{V_{\mathrm{OC}}}{V_{\mathrm{out}} - 1} \right) \\ &= (9.719\,\mathrm{k\Omega}) \left(\frac{10.0}{9.92} - 1 \right) \\ &= 78.4\,\Omega \end{aligned}$$

This output resistance does not meet the required specifications of this project. This is likely additionally due to the internal impedances of the probe, as well as the non-ideal characteristics of the breadboard and OP27 op amps.

2.5 Conclusion

This experiment demonstrated using cascading op amps in a design to exceed the open-loop gain of a single op amp. The OP27 op amp has several limitations that must be accounted for, especially in a design with strict requirements. The low output resistance requirement in this experiment was not met, likely due to the additional impedances of the setup and non-ideal characteristics of the breadboard and probes.

Appendix

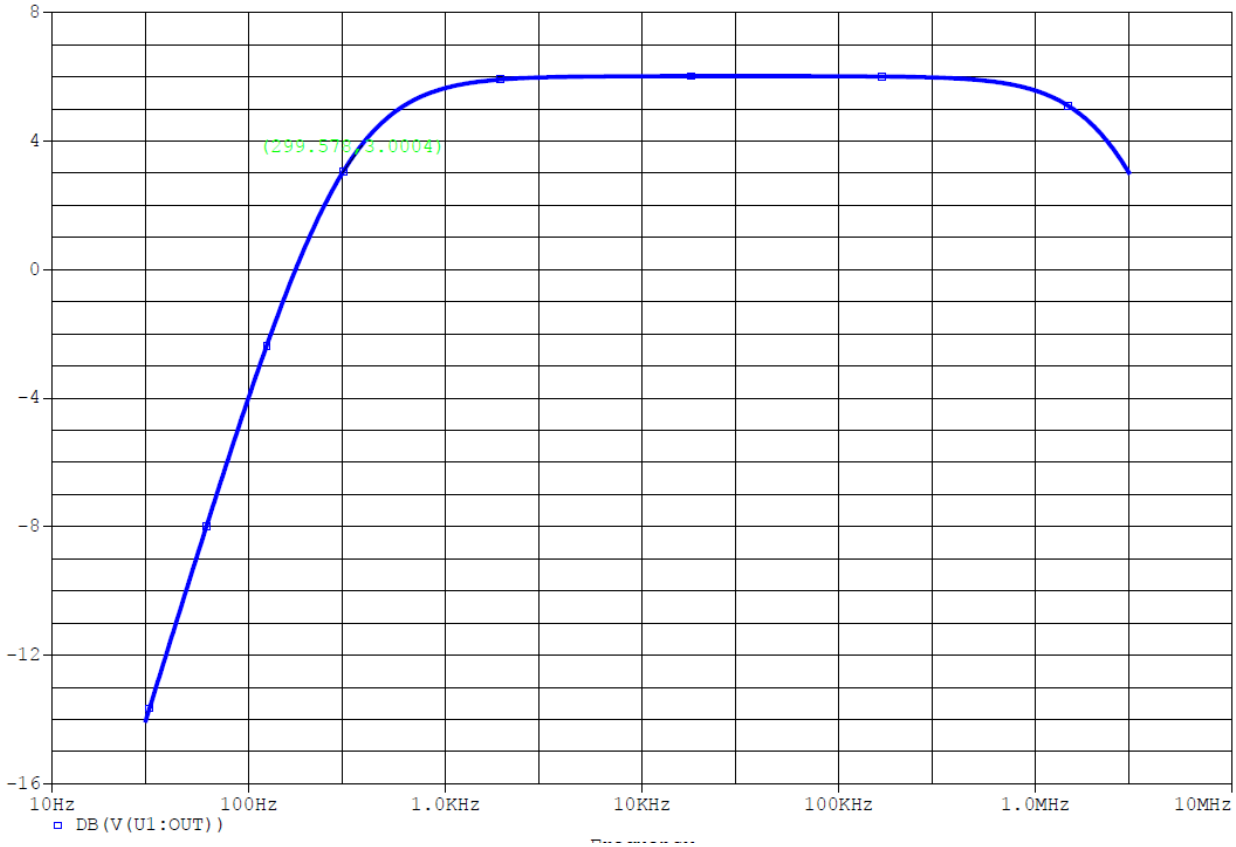


Figure 7: Bode plot of the frequency response of the simulated circuit in Experiment 1.

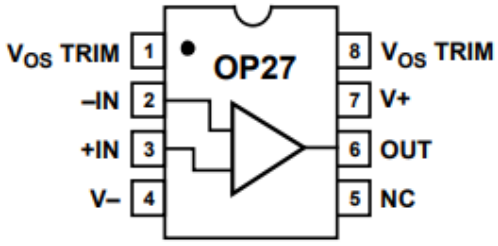


Figure 8: Pinout of the Analog OP27 op amp.

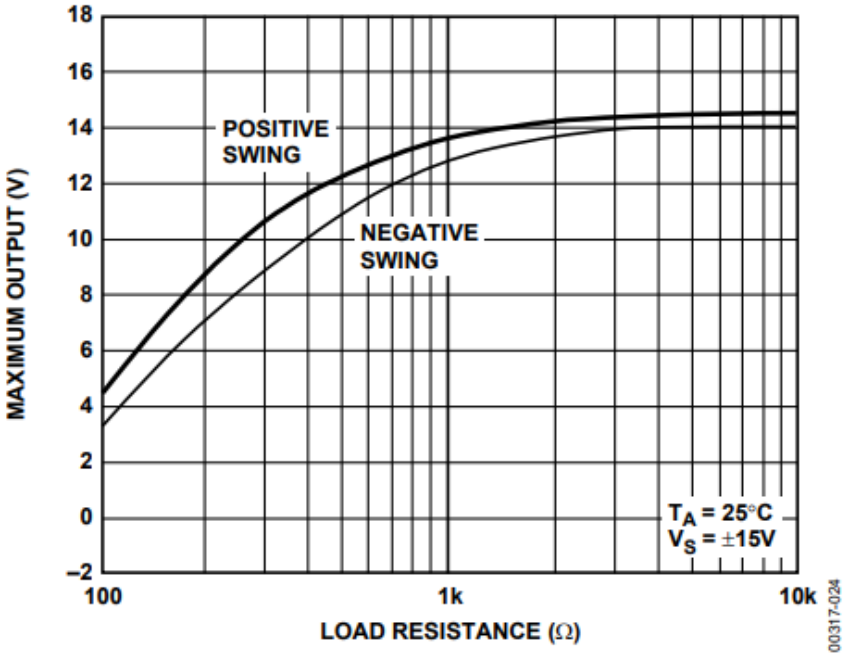


Figure 24. Maximum Output Voltage vs. Load Resistance

Figure 9: Excerpt of the OP27 datasheet.