Lab 10: BJT Amplifier Circuits

EE 352
April 21, 2020

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Experiment 1: Single stage common emitter amplifier

In this experiment, a single stage CE amplifier was built in LTSPICE using the 2N3904 npn transistor. The amplifier was required to follow these specifications,

- Load resistance: $47\,\mathrm{k\Omega}$
- Input resistance: exceeding $1.2\,\mathrm{k\Omega}$
- Mid-band voltage gain: $-85\,\mathrm{V/V}\ \pm 20\%$
- Power supply voltage: $12\,\mathrm{V}$
- Capacitances: $C_B = C_C = 10\,\mu\mathrm{F}$, $C_E = 47\,\mu\mathrm{F}$

DC biasing

This was done by first determining the bias points at DC and analyzing the circuit. Following the suggested base voltage $V_B = V_{CC}/3$, a resistor divider was used to bias the base at $4\,\mathrm{V}$ using $R_1 = 200\,\mathrm{k\Omega}$ and $R_2 = 100\,\mathrm{k\Omega}$. We can now solve for the emitter current by finding the Thevenin equivalent at the base. The base equivalent gives $V_{BB} = 4\,\mathrm{V}$ with a resistance of $R_{BB} = R_1 \parallel R_2$. For the current through the base-emitter junction, if we assume a constant drop of $0.7\,\mathrm{V}$, then the DC emitter current can be found as

$$\begin{aligned} 0 &= V_{BB} - I_E R_{BB} - 0.7 - I_B R_E \\ &= V_{BB} - I_E R_{BB} - 0.7 - (\beta + 1)\, I_E R_E \\ I_E &= \frac{V_{BB} - 0.7}{R_{BB}/(\beta+1) + R_E} \end{aligned}$$

If we choose R_E as $10\,\mathrm{k\Omega}$, the emitter current is approximately $0.3093\,\mathrm{mA}$ and an emitter voltage of $3.093\,\mathrm{V}$, and a base voltage of $3.793\,\mathrm{V}$. At this biasing point, the collector and base current can be found

$$I_C = \alpha I_E = \frac{\beta}{\beta+1} I_E = 0.3063\,\mathrm{mA} \qquad\qquad I_B = \frac{1}{\beta+1} I_E = 3.063\,\mu\mathrm{A}$$

From this, the BJT transconductance and incremental resistance is found at this current as

$$\begin{aligned} g_m &= \frac{I_C}{V_T} = 12.25\,\mathrm{mA/V} \\ r_o &= \frac{V_A}{I_C} = 326\,\mathrm{k\Omega} \\ r_\pi &= \frac{V_T}{I_B} = 8.162\,\mathrm{k\Omega} \end{aligned}$$

AC analysis

The AC equivalent circuit can be found by shorting the capacitors and using the BJT small-signal equivalent. This is shown in Figure 1.

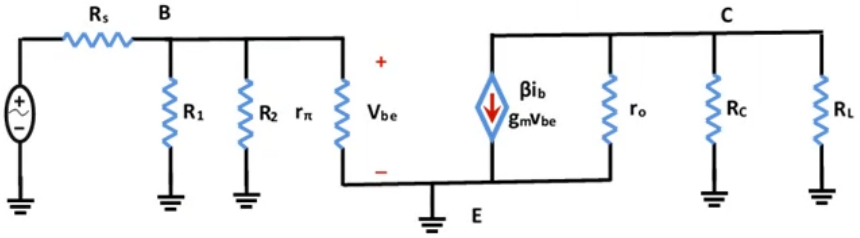

Figure 1: AC equivalent circuit of the CE amplifier.

From the equivalent circuit, the input resistance is determined as

$$R_I = r_\pi \parallel R_1 \parallel R_2 = 7.3\,\text{k}\Omega$$

which exceeds the requirement. The midband gain is required to be $-85\,\text{V/V}$ and will allow the collector resistance to be determined using the equivalent circuit,

$$\begin{aligned} G_v &= -g_m R_o \frac{R_i}{R_s + R_i} \\ -85 &= -0.01225 \times R_o \times 0.993 \\ R_o &= (r_o \parallel R_C \parallel R_L) = 7\,\text{k}\Omega \\ R_C &= 8.44\,\text{k}\Omega \end{aligned}$$

DC simulation and verification

Using the values determined, the DC circuit was built in LTSPICE and a transient analysis was done to verify the voltage, as shown in Figure 2. The transistor voltage and currents were measured as

$$\begin{aligned} V_C &= 9.232\,34\,\text{V} & I_C &= 329.483\,\mu\text{A} \\ V_B &= 3.930\,41\,\text{V} & I_B &= 1.043\,79\,\mu\text{A} \\ V_E &= 3.305\,27\,\text{V} & I_E &= 330.527\,\mu\text{A} \end{aligned}$$

These values were very close to the expected values. The differences are likely due to the changes β, which is roughly 300 in LTSPICE, rather than the 100 used in the calculations. At this bias point, the transconductance was estimated roughly 3.4% from the expected value at

$$g_m = \frac{329.5\,\mu\text{A}}{26\,\text{mV}} = 12.67\,\text{mA/V}$$

Amplifier simulation

The full amplifier circuit was built in LTSPICE, shown in Figure 2, and simulated using a transient analysis for a duration of $1\,\text{ms}$. For an input of $20\,\text{mV}$ (pp) at $20\,\text{kHz}$, the gain was measured as

$$G_v = \frac{-1.76474}{0.020} = -88.2\,\text{V/V}$$

This gain of $-88.2\,\mathrm{V/V}$ is within the specifications, at 3.8% from the expected $-85\,\mathrm{V/V}$. As this is within the requirements, no trimming on R_E or R_C is needed. As we increase the input signal voltage, it begins to clip. The lower bound of the clipping is near the collector voltage at $3.4\,\mathrm{V}$ and the upper bound is near $11.6\,\mathrm{V}$. The maximum voltage swing is $2.4\,\mathrm{V}$ at the emitter, or $66\,\mathrm{mV}$ at the base.

The input resistance by measuring the voltage and current at the base,

$$R_i = \left|\frac{V_b}{i_s}\right| = \frac{20\,\mathrm{mV}}{1.21\,\mu\mathrm{A}} = 16.5\,\mathrm{k\Omega}$$

This input resistance exceeds the specification of $1.2\,\mathrm{k\Omega}$ and exceeded the predicted value. The frequency response was obtained from $10\,\mathrm{Hz}$ to $10\,\mathrm{MHz}$ and is shown in Figure. The cutoff frequencies were measured

$$f_L = 43.0\,\mathrm{Hz} \qquad\qquad f_H = 5.82\,\mathrm{MHz}$$

When the emitter resistor is split into $47\,\Omega$ and $9953\,\Omega$, the new gain and input resistance was measured

$$G_v = \frac{-1.1187}{0.020} = 56\,\mathrm{V/V} \qquad\qquad R_i = \frac{20\,\mathrm{mV}}{863.252\,\mathrm{nA}} = 23.2\,\mathrm{k\Omega}$$

This is a 37% drop from the original gain, and an increase of input resistance. The change in the gain is due to the AC signal dropping across the new $47\,\Omega$ resistor, instead of bypassing the emitter resistors through the capacitor.

Experiment 2: Basic Differential Amplifier

The differential amplifier circuit was created in LTSPICE. Initially, the DC circuit was simulated using a transient analysis to measure the output voltage as

$$V_o = 5.32\,\mathrm{V}$$

The differential gain for this amplifier should be roughly

$$\begin{aligned} A_d &= \frac{1}{2} g_m (r_o \parallel R_2) = -\frac{1}{2}\frac{I_c}{V_T}(r_o \parallel R_2) \\ &\approx 88.9\,\mathrm{V/V} \end{aligned}$$

In LTSPICE, the differential gain was measured, with a test voltage $V_d = 20\,\mathrm{mV}$ (pp) applied across the V_i^+ and V_i^- terminals and the gain was measured as

$$A_d = \frac{1.695}{0.020} \approx 85\,\mathrm{V/V}$$

Then, the common mode gain was measured using a test voltage $V_{cm} = 1\,\mathrm{V}$ (pp) applied to both input terminals. Using a transient simulation, the gain was measured,

$$A_{CM} = \frac{-0.495}{1.000} = -0.495$$

This was fairly close to the expected common mode gain of -0.5. The common mode rejection ratio can now be found as

$$\mathrm{CMRR} = 20\log(A_d/A_{cm}) = 44.7\,\mathrm{dB}$$

Experiment 3: Improved Differential Amplifier

If we assume the current mirror is ideal with matched transistors, then the current across each emitter (and the resistor) is

$$\begin{aligned} I_R = 0.93\,\mathrm{mA} &= \frac{10 - 0.7 - (-10)}{R} \\ \implies R &= 20.75\,\mathrm{k\Omega} \end{aligned}$$

Then, we can determine the DC currents through the original two transistors and determine the new transconductance values,

$$\begin{aligned} I_1 = I_2 &= I_R/2 \\ I_1 = I_2 &= 0.465\,\mathrm{mA} \\ g_m &= 18.6\,\mathrm{mA/V} \end{aligned}$$

In LTSPICE, the circuit was simulated at DC with both inputs grounded. The output voltage was found using a transient analysis as

$$V_o \approx 5\,\mathrm{V}$$

Next, a $20\,\mathrm{mV}$ (pp) sine wave was applied across the differential input and the gain was calculated, quite close to the original amplifier, as

$$A_d = \frac{1.82}{0.02} \approx 91\,\mathrm{V/V}$$

The common-mode gain was tested using the approach as earlier and the common mode gain was calculated as

$$A_{cm} = \frac{915 \times 10^{-6}}{0.02} = 0.046\,\mathrm{V/V}$$

The CMRR was recalculated with these new values as

$$\mathrm{CMRR} = 20\log(A_d/A_{cm}) = 66.0\,\mathrm{dB}$$

The new CMRR is improved substantially compared to the original CMRR, nearly $20\,\mathrm{dB}$ higher. This improvement is due to the fact that there is more control over the current because of the added current mirror. A larger change in the input signal voltage no longer affects the bias current significantly, since the bias current is primarily controlled through the mirror.

Appendix

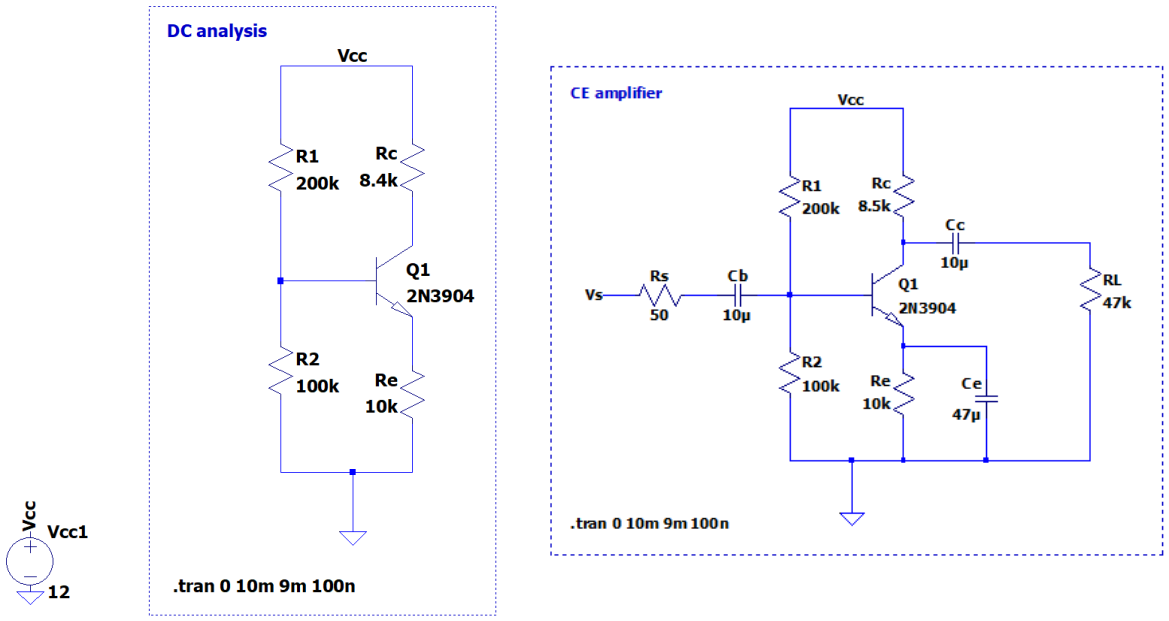

Figure 2: DC and AC circuits built and simulated in LTSPICE.