WASHINGTON STATE UNIVERSITY
SCHOOL OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

EE 352, ELECTRICAL ENGINEERING LABORATORY

LAB #8

MOSFET Amplifier Circuits

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Lab Overview

The purpose of this lab was to explore the various properties of MOSFET transistors and their use in amplifier circuits. We will design and validate the common source amplifier circuit design using the ZVN2110A NFET transistor. Next, we will build the current mirror circuit using matched transistors on the CD4007 IC. Then, we will build an inverter with the same CMOS chip.

1 Single stage common source amplifier

1.1 Purpose

The purpose of this experiment is to design a common source amplifier under the listed requirements. We will use the ZVN2110A NMOS transistor to amplify an AC input signal. The design requirements are listed below in Table 1.

1.2 Theoretical background

In this experiment, we will design a common source amplifier using the ZVN2110A transistor. We are to follow the common source amplifier circuit shown in Figure 1 and to determine the component values to reach the required amplifier specifications, shown in Table 1 below.

Table 1: Required specifications of the amplifier

Specification	Symbol	Value
Load resistance	R_L	$100\,\mathrm{k\Omega}$
Input resistance	R_i	$> 200\,\mathrm{k\Omega}$
Mid-band gain	G_V	$-50\,\mathrm{V/V} \pm 20\%$
Supply voltage	V_{DD}	$15\,\mathrm{V}$
Circuit capacitors	C_G	$10\,\mu\mathrm{F}$
	C_S	$47\,\mu\mathrm{F}$
	C_D	$10\,\mu\mathrm{F}$

In order to achieve these specifications, the resistor values must be chosen appropriately. To accomplish this, we begin by finding the small signal approximation, shown in Figure 2a. In this circuit, both the input resistors R_1 and R_2 are brought to AC ground, as V_{DD} is DC-only. The AC input and output resistances then become

$$R_{\mathrm{in}} = R_1 \parallel R_2 \tag{1}$$

$$R_{\mathrm{o}} = R_D \parallel R_L \parallel r_o \tag{2}$$

The amplifier gain is then specified by the dependent source and the transconductance is parameterized by the specifications of the transistor,

$$G_V = -g_m R_{\mathrm{o}} \tag{3}$$

$$g_m = \sqrt{2k_n I_D} = k_n \left(V_{GS} - V_T\right) \tag{4}$$

At DC, the equivalent circuit is shown in Figure 2b. This is achieved as the capacitors act as an open circuit for a DC input. From the DC circuit, we can determine the DC bias voltage at the gate using a simple voltage divider,

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} \tag{5}$$

From the previous lab, we found approximate values for V_T, K_n, and λ. If we take a drain current $I_D \approx 0.3\,\mathrm{mA}$, we can find the transconductance g_m and equivalent dynamic resistance r_o,

$$g_m = \sqrt{2k_n I_D} \approx 3.464\,\mathrm{mA/V}$$

$$r_o = \frac{1}{\lambda I_D} \approx 333.3\,\mathrm{k\Omega}$$

Then, from (3), the total output resistance can be found, and using (2), we can find R_D

$$R_o = \frac{G_V}{-g_m} = \frac{50}{3.464\,\text{mA/V}} = 14.433\,\text{k}\Omega$$
$$R_D = \left(R_o^{-1} - r_o^{-1} - R_L^{-1}\right)^{-1} = 17.8\,\text{k}\Omega \approx 20\,\text{k}\Omega$$

For this value of R_D, we can determine the voltage drop across the resistor at the current $0.3\,\text{mA}$ and find the drain voltage,

$$V_D = V_{DD} - I_D R_D = 9\,\text{V}$$

Now we can determine the gate voltage using (4) and the transconductance found earlier.

$$\begin{aligned} g_m &= k_n\left(V_{GS} - V_T\right) \\ V_{GS} &= \frac{g_m}{k_n} + V_T \\ V_G &= \frac{g_m}{k_n} + V_T + V_S \end{aligned} \tag{6}$$

If we choose the source voltage V_S of $3\,\text{V}$, we find the source resistance and gate voltage to as

$$R_S = 10\,\text{k}\Omega$$
$$V_G = 4.873\,\text{V}$$

Then, if we choose R_1 to be $1\,\text{M}\Omega$, we can use (5) to find $R_2 \approx 470\,\text{k}\Omega$.

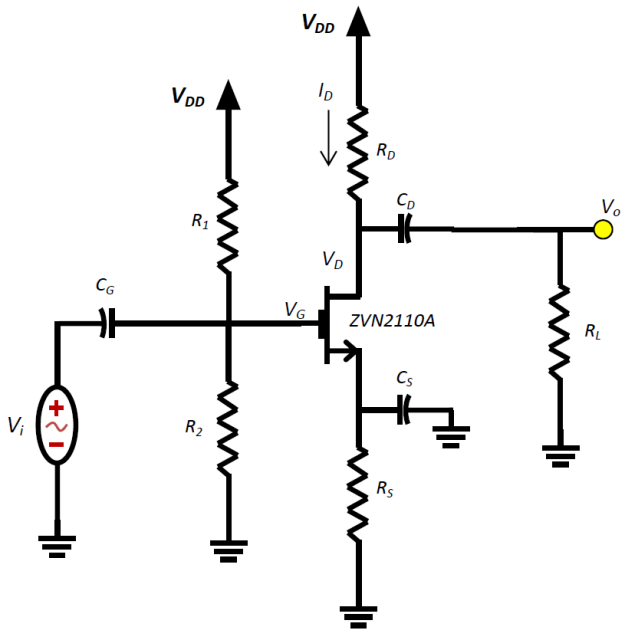
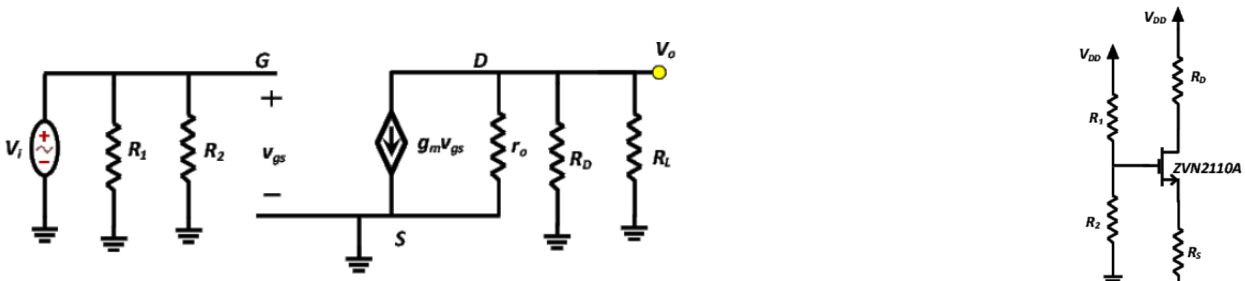


Figure 1: The common source amplifier circuit used in Experiment 1.

The amplifier circuit was simulated using PSPICE within OrCAD using the component values found previously. The circuit drawn is shown in Figure 3 with the NMOS transistor modeled using $V_T \approx 1.7$, $K_n \approx 0.02$, and $V_A \approx 100$. An AC sweep simulation was done from $100\,\text{Hz}$ to $10\,\text{MHz}$ with the plot of the results shown in Figure 4. This resulted in a mid-band gain of approximately $57\,\text{V/V}$, within the 20% margin in the specifications.



(a) (b)

Figure 2: Equivalent circuits for (a) small AC signals and (b) DC signals.

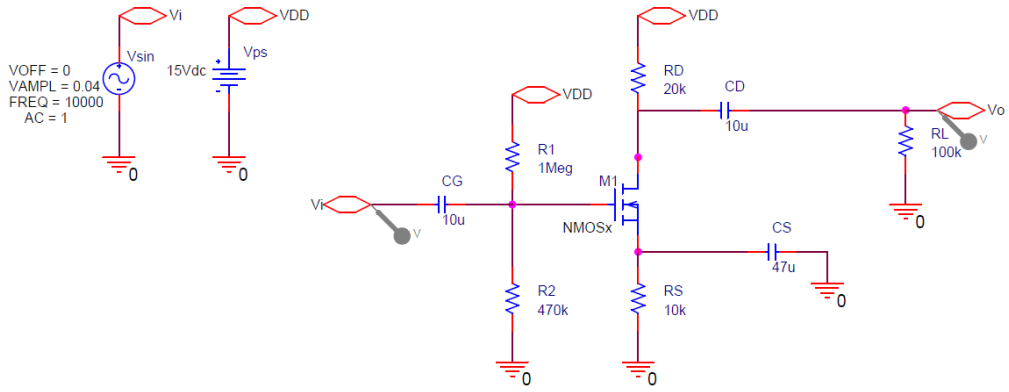


Figure 3: Circuit in OrCAD for use in the AC sweep simulation.

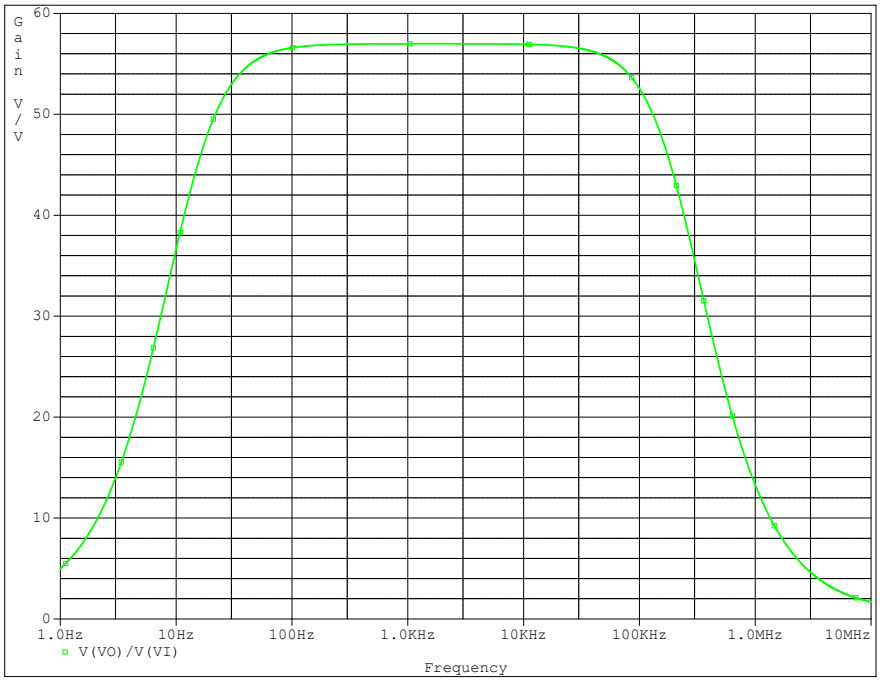


Figure 4: Result of the PSPICE simulation using the modeled components.

1.3 Procedure

The follow steps were carried out, as instructed by the lab assignment.

1. Using the chosen component values, the resistors were chosen and their resistances were measured using the DMM. The RLC meter was used to measure the capacitor values.
2. The circuit was constructed and the DC power supply was attached. The capacitors were temporarily disconnected during this step. The terminal voltages were measured using the DMM. The transconductance was estimated using these values.
3. A $20\,\mathrm{mV}$ peak-to-peak sine input signal was applied using the function generator at $20\,\mathrm{kHz}$. The output voltage was measured using the oscilloscope. The midband gain was calculated. The resistance was adjusted to adjust the current, affecting the gain of the amplifier.
4. The low and high cutoff frequencies were found by calculating $0.707\times$ the midband gain.
5. The frequency response of the amplifier was plotted using Excel.
6. The amplitude of the input signal was increased until clipping was observed and snapshots were taken of the oscilloscope. The drain voltage was measured using the oscilloscope with DC coupling.

1.4 Results and analysis

Component and DC measurements

The resistors were measured using the DMM and the capacitors were measured with the RLC meter. These values were recorded in Table 2.

Table 2: Experimental and nominal component values.

Component	Nominal	Experimental	% Error
R_1	$1\,\mathrm{M\Omega}$	$1.01\,\mathrm{M\Omega}$	1%
R_2	$470\,\mathrm{k\Omega}$	$465\,\mathrm{k\Omega}$	1%
R_D	$20\,\mathrm{k\Omega}$	$19.47\,\mathrm{k\Omega}$	2.6%
R_S	$10\,\mathrm{k\Omega}$	$9.75\,\mathrm{k\Omega}$	2.5%
C_D	$10\,\mu\mathrm{F}$	$9.77\,\mu\mathrm{F}$	2.3%
C_G	$10\,\mu\mathrm{F}$	$9.56\,\mu\mathrm{F}$	4.4%
C_S	$47\,\mu\mathrm{F}$	$38.4\,\mu\mathrm{F}$	18.3%
R_L	$100\,\mathrm{k\Omega}$	$97.3\,\mathrm{k\Omega}$	2.7%

With no AC input signal, the transistor terminal voltages were measured using the DMM. The source, gate, and drain voltages were respectively,

$$V_S = 3.195\,\mathrm{V}$$
$$V_G = 4.568\,\mathrm{V}$$
$$V_D = 8.622\,\mathrm{V}$$

With these component values, the input signal was applied and the output voltage was measured as $1.4\,\mathrm{V}$ with an input voltage of $20\,\mathrm{mV}$ peak-to-peak sine wave. The gain was calculated to be $70\,\mathrm{V/V}$, roughly 20% higher than the maximum allowed voltage. Adjusting R_S to $20\,\mathrm{k\Omega}$ dropped the gain below the minimum, at $35\,\mathrm{V/V}$. Choosing a resistance between these, R_S was trimmed up to $16.8\,\mathrm{k\Omega}$. With an input peak-to-peak voltage of $20.4\,\mathrm{mV}$, the output voltage was measured at $912\,\mathrm{mV}$—a gain of $-44.7\,\mathrm{V/V}$. With the new resistance, the DC voltages were remeasured,

$$V_S = 3.220\,\mathrm{V}$$
$$V_G = 4.566\,\mathrm{V}$$
$$V_D = 10.69\,\mathrm{V}$$

This change brought the drain current and transconductance to

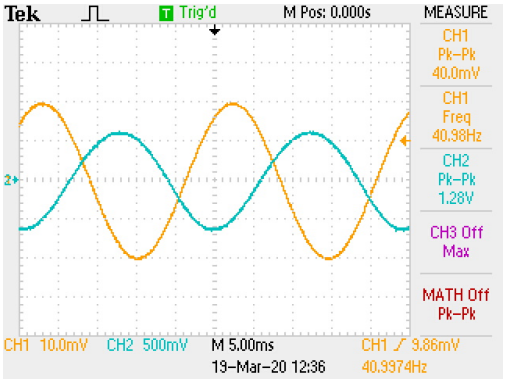
$$I_D = \frac{3.220\,\mathrm{V}}{16.4\,\mathrm{k\Omega}} = 0.196\,\mathrm{mA}$$
$$g_m = \sqrt{2k_n I_D} = 2.8\,\mathrm{mA/V}$$

The cutoff frequencies were found by sweeping the frequency until the output voltage reached $0.707 \times 912\,\mathrm{mV}$. Using the oscilloscope, the output voltages were measured and shown in Figure 5. The low and high cutoff frequencies were determined to be $f_L = 41\,\mathrm{Hz}$ and $f_H = 260\,\mathrm{kHz}$. Additional points were collected at various frequencies, sweeping from $20\,\mathrm{Hz}$ to $500\,\mathrm{kHz}$. This data was collected using Excel and plotted in Figure 6.

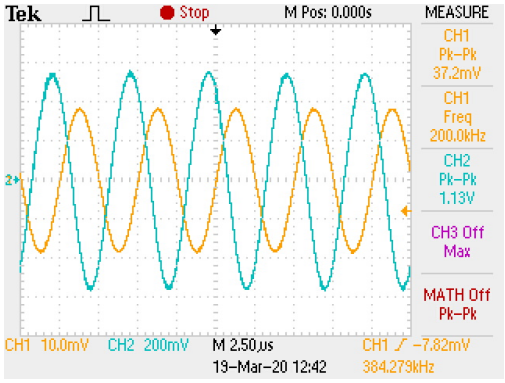
Next, the clipping was investigated by varying the amplitude of the input signal at $10\,\mathrm{kHz}$. It was found that the bottom of the output signal was clipped first, albeit the entire waveform was distorted. Using cursors, the clipping was measured at $V_{\min} = 3.6\,\mathrm{V}$ and $V_{\max} = 14.2\,\mathrm{V}$.

1.5 Conclusion

We achieved the required gain for the single stage common source amplifier. The overall error in the midband gain was roughly 10.6% lower than expectation, but within the 20% tolerance. The amplifier designed in the experiment had a usable bandwidth of roughly $260\,\mathrm{kHz}$. The input resistance exceeded the requirement of only $200\,\mathrm{k\Omega}$. The measured values roughly fit the expected response, found using the PSPICE simulation.



(a) Low frequency cutoff.



(b) High frequency cutoff.

Figure 5: Cutoff frequencies measured using the oscilloscope.

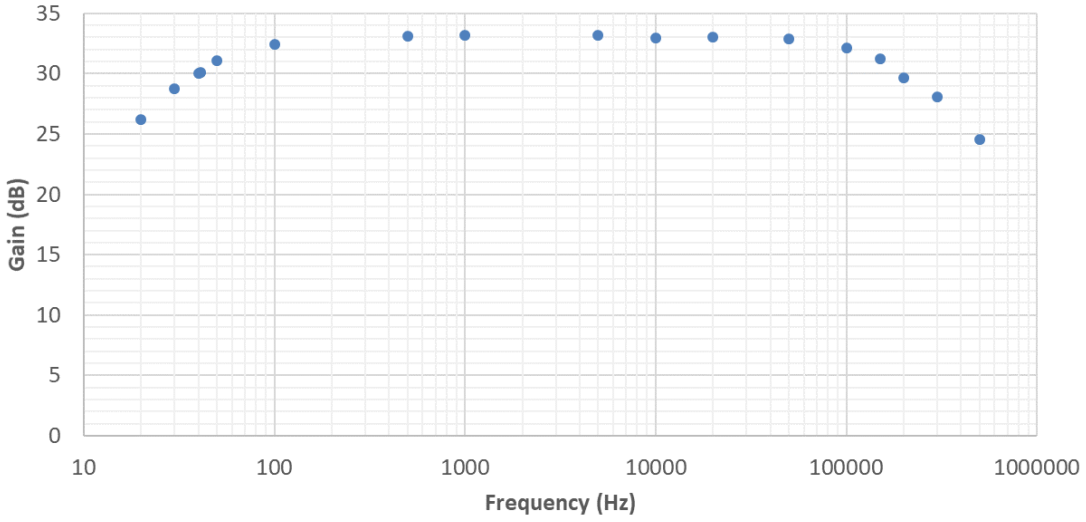


Figure 6: The frequency response of the amplifier.

2 Current mirror circuit

2.1 Purpose

The purpose of this experiment is to design and implement a current circuit mirror using a matched NMOS transistors on the CD4007 IC. This circuit produces an equal current across a matched transistor with a connected gate. This experiment demonstrates a use-case for matched transistors.

2.2 Theoretical background

A current mirror circuit creates a current source that mirrors the current through a matched transistor. In this experiment, we will use matched NMOS transistors using the CD4007 chip. The current mirror circuit used in this experiment is shown in Figure 7 below.

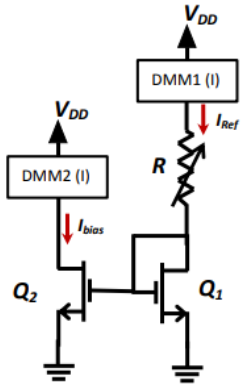


Figure 7: The current mirror circuit used in Experiment 2.

In order to achieve a reference current of $1\,\mathrm{mA}$ through Q_1, the resistor value needs to be calculated. As the transistor will be operating within the saturation region, we can determine the gate-source voltage required.

$$\begin{aligned} I_D &\approx \frac{k_n}{2}\left(V_{GS} - V_t\right)^2 \\ 1\,\mathrm{mA} &\approx \frac{0.08}{2}\left(V_{GS} - 1.7\,\mathrm{V}\right)^2 \\ V_{GS} &\approx 1.86\,\mathrm{V} \end{aligned}$$

As the source is connected to ground, the gate-source voltage is equivalent to the gate and drain voltages. From this, the resistance can be calculated as

$$\begin{aligned} R &= \frac{V_{DD} - V_G}{I} = \frac{5 - 1.86\ \mathrm{V}}{1\ \mathrm{mA}} \\ &= 3.14\,\mathrm{k\Omega} \end{aligned}$$

2.3 Procedure

The follow steps were carried out, as instructed by the lab assignment.

1. The circuit shown in Figure 7 was constructed using the CD4007 IC and a decade box as the variable resistor. The DC power supply was set to $5\,\mathrm{V}$ and the DMMs were attached to measure currents across each transistor.
2. Pin 7 of the CD4007 was attached to ground, as it is attached to the bodies of each of the NFETs housed within the IC.
3. The decade box was initially set to the resistance found in the prelab ($3.14\,\mathrm{k\Omega}$) and was varied until the reference current reached $1\,\mathrm{mA}$.
4. Both currents were measured with the DMM and recorded.

2.4 Results and analysis

The decade box achieved a reference current of $1\,\mathrm{mA}$ around $3.38\,\mathrm{k\Omega}$, about 8% higher than the expected value. This error is likely due to an inaccurate k_n or V_T value used in the prelab calculations. However, it was still in the rough order of magnitude.

At a reference current of $1\,\mathrm{mA}$, the mirrored bias current was found to be $2.110\,\mathrm{mA}$, around 5.5% error from the expected $2\,\mathrm{mA}$. This amount of error is fairly low and is due to defects in the manufacturing tolerances of the transistor aspect ratio of each transistor. The transistors are not perfectly matched and have some variances to them.

2.5 Conclusion

The current mirror circuit is used to create a current source through a transistor, equal to that of a matching and connected transistor. In this experiment, we were able to create this with roughly 5% error, within the expected tolerance of the matched NMOS transistors in the CD4007 IC.

3 CMOS Inverter

3.1 Purpose

This experiment uses a CMOS chip, containing an NMOS and PMOS, to create a logic inverter. We use these transistors to invert a signal from 'off' to 'on' and vice-versa. In between these boolean regions, one or both may operate in the saturation region and can act as a CMOS inverting amplifier with a relatively high gain.

3.2 Theoretical background

On a CMOS chip, it will contain two complementary transistors: one PMOS and one NMOS transistor. Here, we will each transistor with the gates connected to a common node. If we use discrete logic levels, containing a logic low ($0\,\mathrm{V}$) and logic high ($5\,\mathrm{V}$), each transistor acts as a switch in the triode region. However, at transitioning voltages, each transistor goes through the saturation region and acts as an amplifier circuit.

In this experiment, we will build the inverter circuit shown in Figure 8a below. As we increase the input voltage V_i, it will cycle through the five regions shown in Figure 8b. At an output voltage half of the supply voltage, in region 3, the inverter can act as an inverting amplifier. We will explore this using the function generator in this experiment.

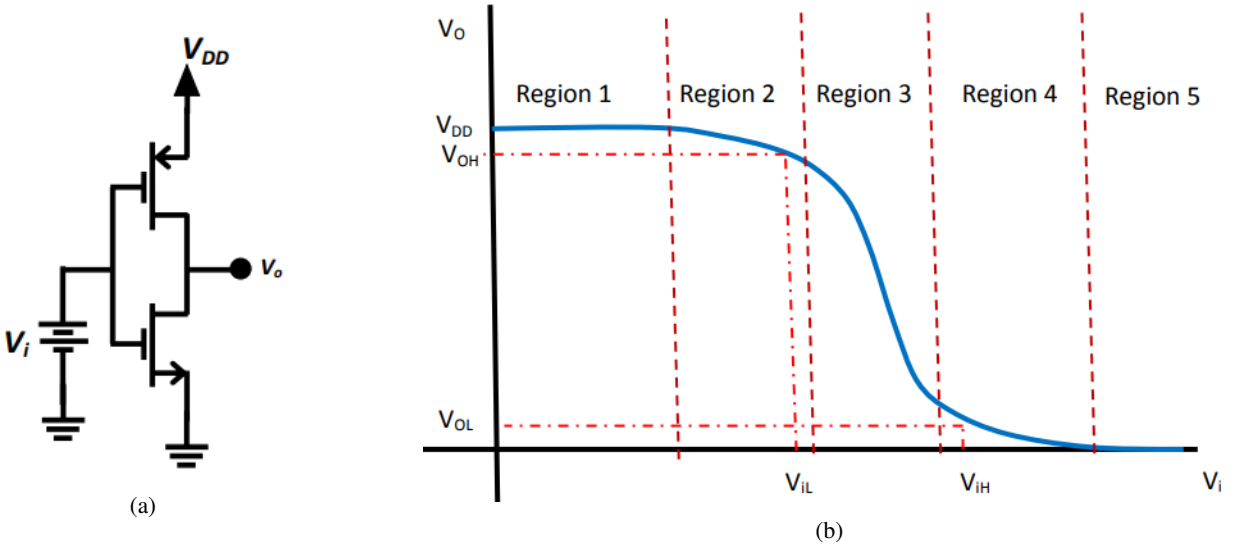


Figure 8: The CMOS inverter (a) circuit and (b) the corresponding operating regions.

3.3 Procedure

The follow steps were carried out, as instructed by the lab assignment.

1. The circuit shown in Figure 8a was constructed using the CMOS pair Q2 within the CD4007 IC. One DC power supply V_{DD} was set to $5\,\mathrm{V}$. The other will be used as the input gate voltage.
2. The NFET base pins were grounded using Pin 7, and the PFET bases were tied to V_{DD}.
3. The input voltage V_i was swept from 0 to $5\,\mathrm{V}$. DMMs were used to measure the input and output voltages. These points were recorded in Excel and the output-input voltage characteristics were plotted.
4. The five transition regions were determined on the plot.
5. The input voltage at an output voltage of $V_{DD}/2 = 2.5$ was recorded. The function generator was enabled with an offset voltage of this value using $10\,\mathrm{mV}$ peak-to-peak sine waves at $1\,\mathrm{kHz}$.
6. Using the oscilloscope with AC coupling, the output voltage was measured and the gain was calculated. A screenshot was taken at this point.

3.4 Results and analysis

After sweeping the input voltage from $0\,\mathrm{V}$ to $5\,\mathrm{V}$, the data was recorded and plotted. We can estimate the regions by using a threshold voltage of $V_{tn} \approx 1.6\,\mathrm{V}$ and $V_{tp} \approx -2.25\,\mathrm{V}$ and applying the cutoff/triode/saturation conditions to each transistor to determine the region transitions. The results of this are shown in Figure 9 below.

In region 3, at an input voltage $V_i \approx 2.0574\,\mathrm{V}$, the output voltage is roughly $V_{DD}/2 = 2.50\,\mathrm{V}$. At this point, the CMOS pair acts as an amplifier as both transistors are in the saturation region. We can apply a $10\,\mathrm{mV}$ sine wave using the function generator at this voltage offset to calculate the gain. For an input of $6.96\,\mathrm{mV}$, the output was $320\,\mathrm{mV}$, shown in Figure 10 below. This was a gain of $45.98\,\mathrm{V/V}$.

3.5 Conclusion

In this experiment, we successfully used the CMOS inverter to invert a $5\,\mathrm{V}$ input. By sweeping the input voltage, we verified the five regions which the inverter can operate as one or both transistors run through the triode and saturation region. When both transistors are within the saturation region, we found the inverter can act as an inverting amplifier, with a gain of nearly $50\,\mathrm{V/V}$.

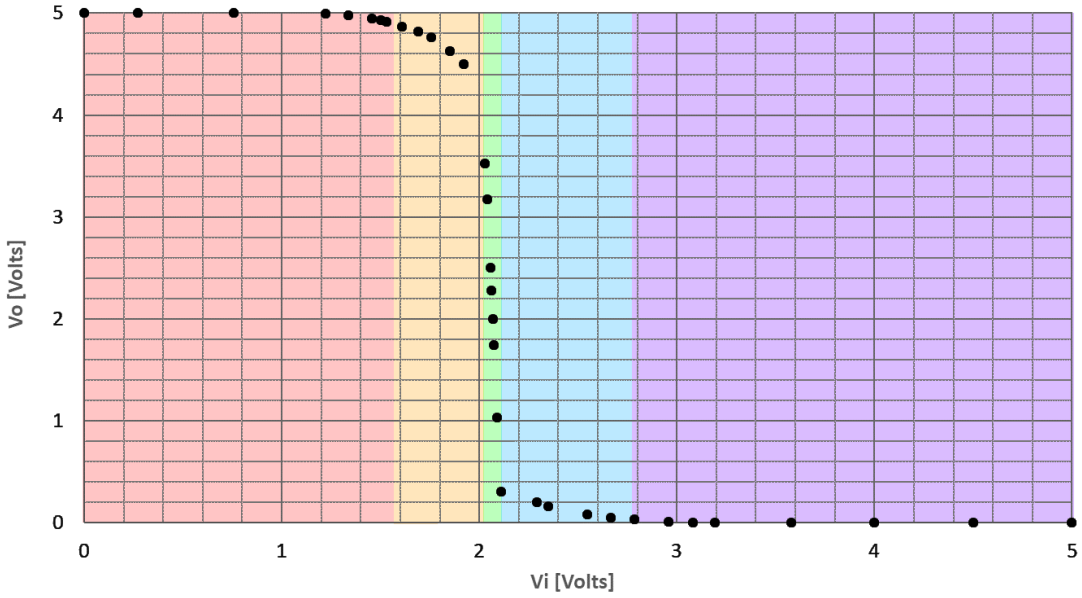


Figure 9: The regions of the CMOS inverter. (1) red, (2) orange, (3) green, (4) blue, (5) purple.

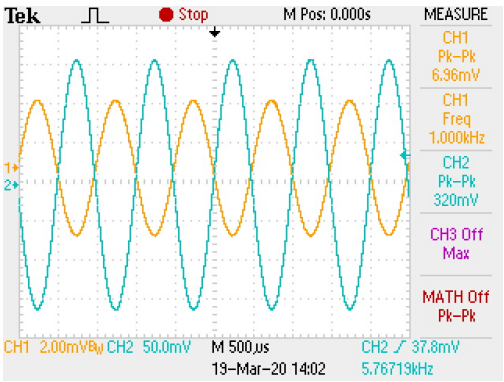


Figure 10: CMOS inverter acting as an amplifier with a gain of nearly $50\,\mathrm{V/V}$.