# Simulation 2

EE 311
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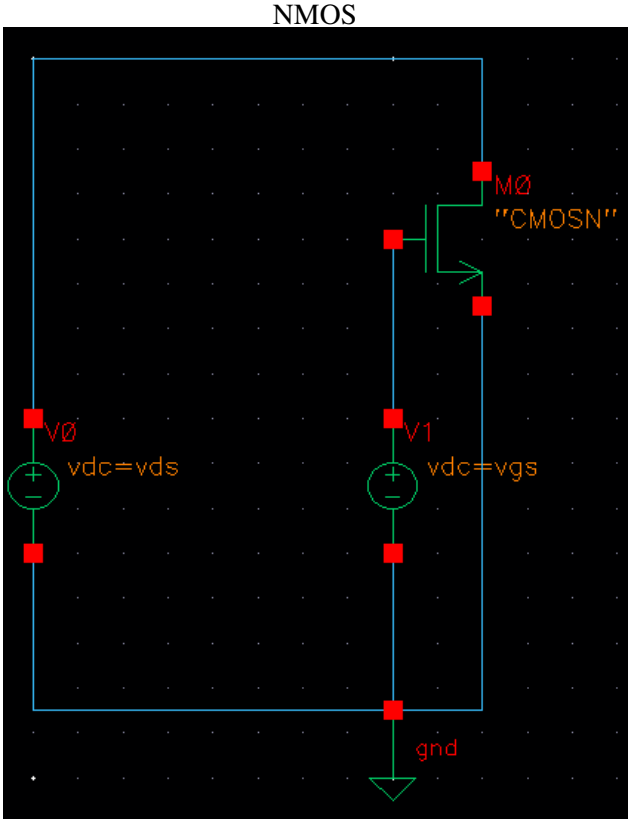
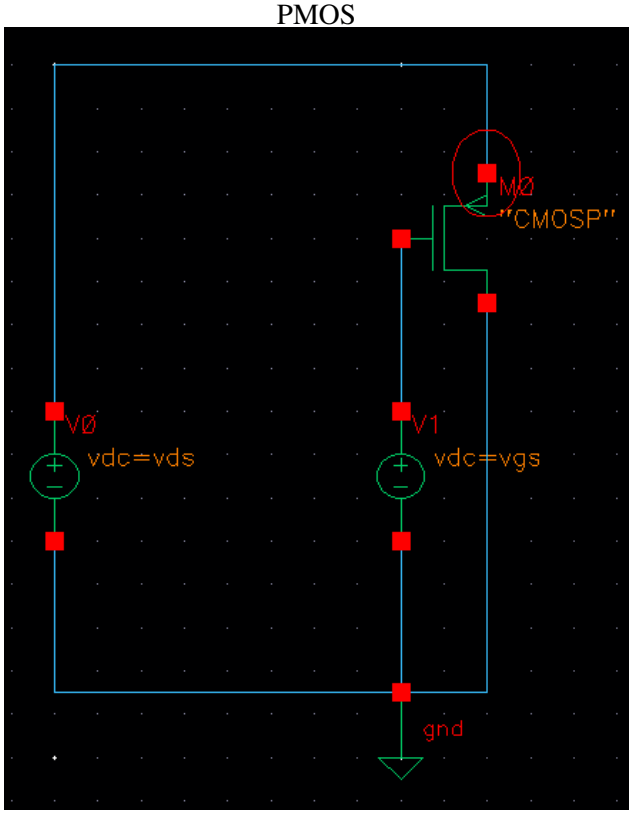
**(a) Circuit in Virtuoso**

NMOS

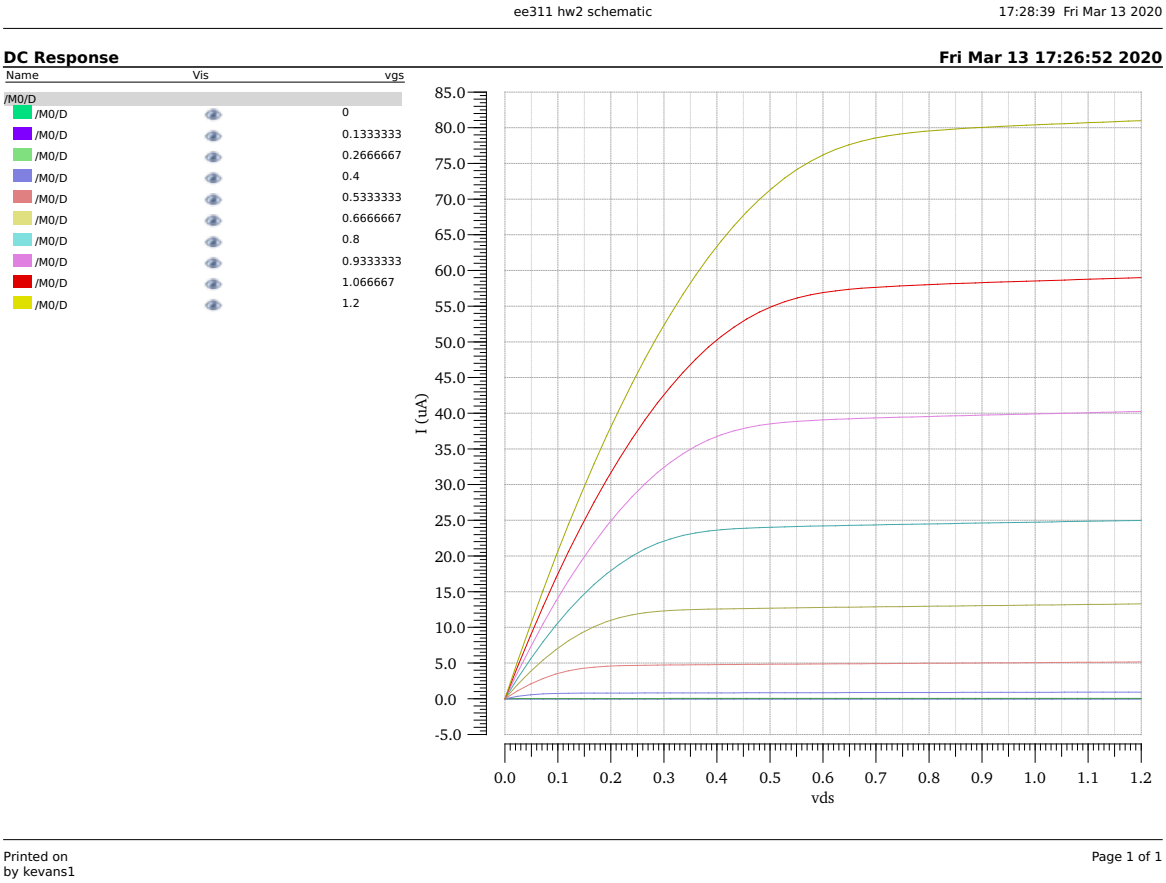



PMOS




Was I supposed to sweep $V_{gs}$ through negative voltages or flip the polarity of the dc supply? The instructions didn't mention it and I thought that was a little strange...

## (b) NMOS $I$-$V_{ds}$


ee311 hw2 schematic
17:28:39 Fri Mar 13 2020
DC Response
Fri Mar 13 17:26:52 2020
Name
Vis
vgs
/M0/D
/M0/D 0
/M0/D 0.1333333
/M0/D 0.2666667
/M0/D 0.4
/M0/D 0.5333333
/M0/D 0.6666667
/M0/D 0.8
/M0/D 0.9333333
/M0/D 1.066667
/M0/D 1.2
I (uA)
85.0
80.0
75.0
70.0
65.0
60.0
55.0
50.0
45.0
40.0
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2
vds
Printed on
by kevans1
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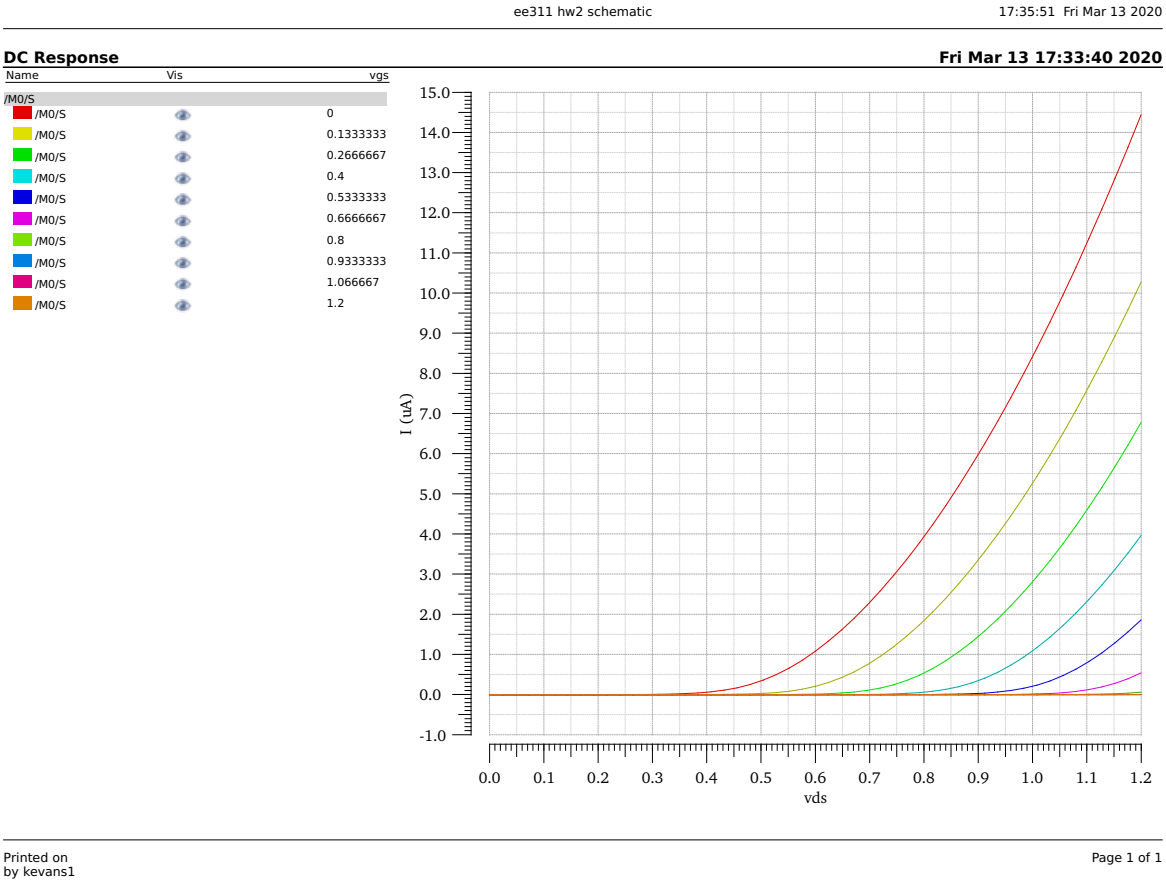
## (c) PMOS $I$-$V_{ds}$


ee311 hw2 schematic
17:35:51 Fri Mar 13 2020
DC Response
Fri Mar 13 17:33:40 2020
Name
Vis
vgs
/M0/S
/M0/S 0
/M0/S 0.1333333
/M0/S 0.2666667
/M0/S 0.4
/M0/S 0.5333333
/M0/S 0.6666667
/M0/S 0.8
/M0/S 0.9333333
/M0/S 1.066667
/M0/S 1.2
I (uA)
15.0
14.0
13.0
12.0
11.0
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2
vds
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**(d) Discussion**

i. The NMOS operates in the cutoff–triode–saturation region as $V_{ds}$ increases. Current runs from the top terminal (drain) to the lower (bottom). The PMOS operates in the cutoff–saturation region as $V_{ds}$ increases and is operating "flipped", as the current is running from the lower terminal up to the top. As the PMOS is acting in reverse, the current plots are flipped.

ii. The NMOS curve family experiences all three regions:

- The lower $V_{gs}$ curves are in the cutoff region, where $V_{GS} < 0.4\,\text{V}$. The threshold voltage $V_{tn}$ is around $0.267$ to $0.4\,\text{V}$.
- For the upper curves ($V_{gs} \geq 0.4$), the left-side is in the triode region, the right-side is in the saturation region.
- For example: the orange curve ($V_{gs} = 1.2$), it is in the triode region from $V_{DS} \approx 0$ to $0.7$. After $0.7$, it is in the saturation region.

For the PMOS:

- All the plots are in the cutoff region until current begins to flow. For $V_{gs} > 0.5$ or so, the transistors barely exit from the cutoff region.
- It only operates at saturation afterwards, as the drain-source terminals are flipped in this situation.

iii. The plots are the showing the expected current behavior. For the NMOS, the curves go through the cutoff–triode–saturation regions. The PMOS goes from the cutoff to the saturation as the transistor as the threshold voltage is negative and the drain-source voltage is negative as well.

iv. If you double the transistor width, the $k_n$ and $k_p$ values are doubled, so the current through the drain/source will double as $i_D \propto k \propto W$. As an example, if you have an NMOS in both the triode/saturation region (red dashed line) and double the width, you would expect the current to double (blue solid line):