Homework 5, Simulation

EE 311
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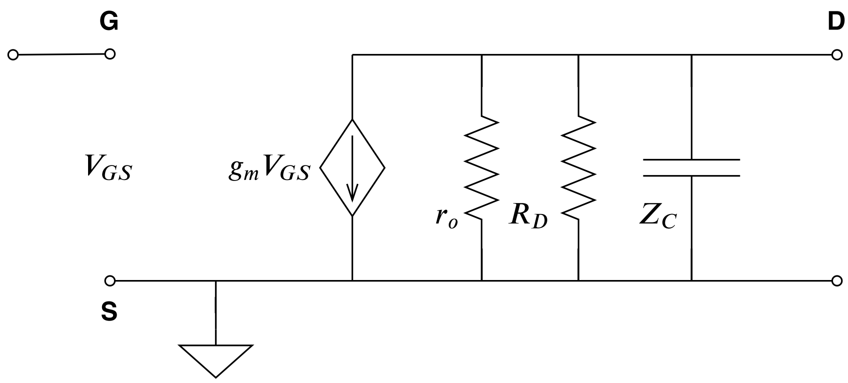
Kevin Evans
ID: 11571810

The amplifier specifications are given as:

- Low frequency gain: exceeding $12\,\mathrm{dB}$ $(4\,\mathrm{V/V})$
- Bandwidth: exceeding $500\,\mathrm{MHz}$
- VDD: $1.2\,\mathrm{V}$

For this circuit, the small-signal equivalent is:



From this, the amplifier gain G_v is given as

$$\begin{aligned} G_v &= g_m \left(r_o \parallel R_D \parallel Z_C \right) \\ &= g_m R_{eq} \end{aligned}$$

As the capacitor has a fairly tiny value, this will be fairly neglible at lower frequencies. Nearing the bandwidth frequency, its impedance will affect the output fairly significantly,

$$Z_C \bigg|_{500\,\mathrm{MHz}} = \frac{1}{j\omega C} \approx 6.4\,\mathrm{k\Omega}$$

Knowing this, we must choose a drain resistance R_D value that is less than Z_C. The transconductance and dynamic resistance is given as

$$\begin{aligned} g_m &= \sqrt{2\,k_n \frac{W}{L} I_D} \\ r_o &= \frac{1}{\lambda I_D} \end{aligned}$$

From this, we can calculate R_D for any I_D and aspect ratio for a target gain of 4 V/V,

$$\begin{aligned} R_D &= \left(R_{eq}^{-1} - r_0^{-1} \right) \\ &= \left(\frac{g_m}{4} - r_0^{-1} \right) \end{aligned}$$

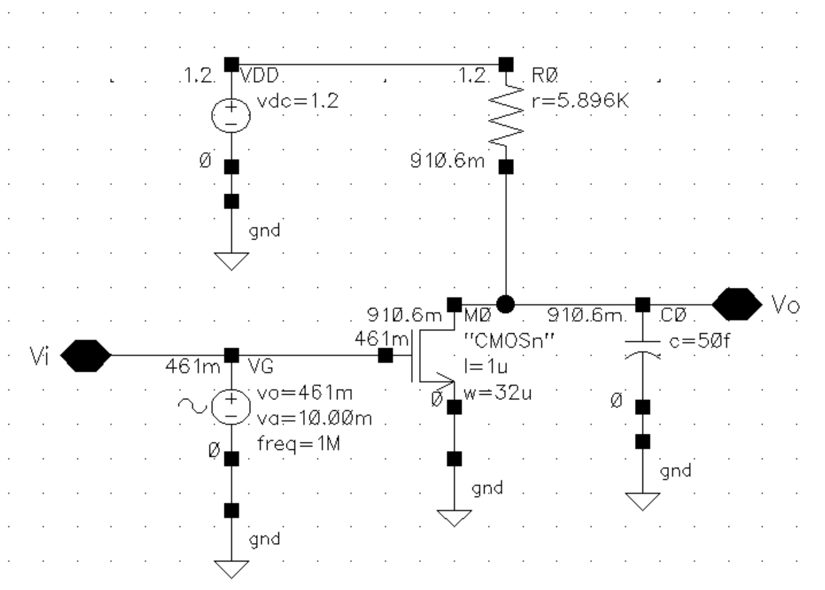
From the last simulation assignment (HW 2), we obtained the I_D-V_{ds} characteristics for this NMOS transistor at its default W/L ratio. From these curves, we can somewhat arbitrarily choose a bias current of $I_D = 80\,\mu\text{A}$. If we use MATLAB to simply calculate the resistance, we can iterate through potential values of W/L until we find a resistance R_D that is near Z_C at higher frequencies.

```
% parameters to try out
I_d   = 80e-6;                     % drain current (A)
WL    = 32;                        % aspect ratio (um/um)

% const params, given in modelfile
Kn    = 210.88e-6;                 % (A/V^2)
L     = 1.127257;                  % lambda
Av    = 4;                         % gain (V/V)
Vtn   = 0.3074;                    % threshold voltage (V)
Vdd   = 1.2;                       % PS voltage (V)

% intermediate calculations
g_m   = sqrt(2*Kn*I_d*WL);         % transconductance
r_o   = 1 / (L*I_d);               % dynamic resistance
R_eq  = Av / g_m;                  % total output resistance

% target values
R_d   = 1/(1/R_eq - 1/r_o);        % omitting the Zc
V_ov  = sqrt(2 * I_d / (Kn * WL)); % overdrive voltage
V_g   = V_ov + Vtn;                % gate voltage
V_d   = Vdd - I_d * R_d;           % drain voltage @ I_d

disp("----------------------------------");
disp("Resistance    = " + R_d + " ohm"   );
disp("Gate voltage  = " + V_g + " V (DC)");
disp("Drain voltage = " + V_d + " V (DC)");
```

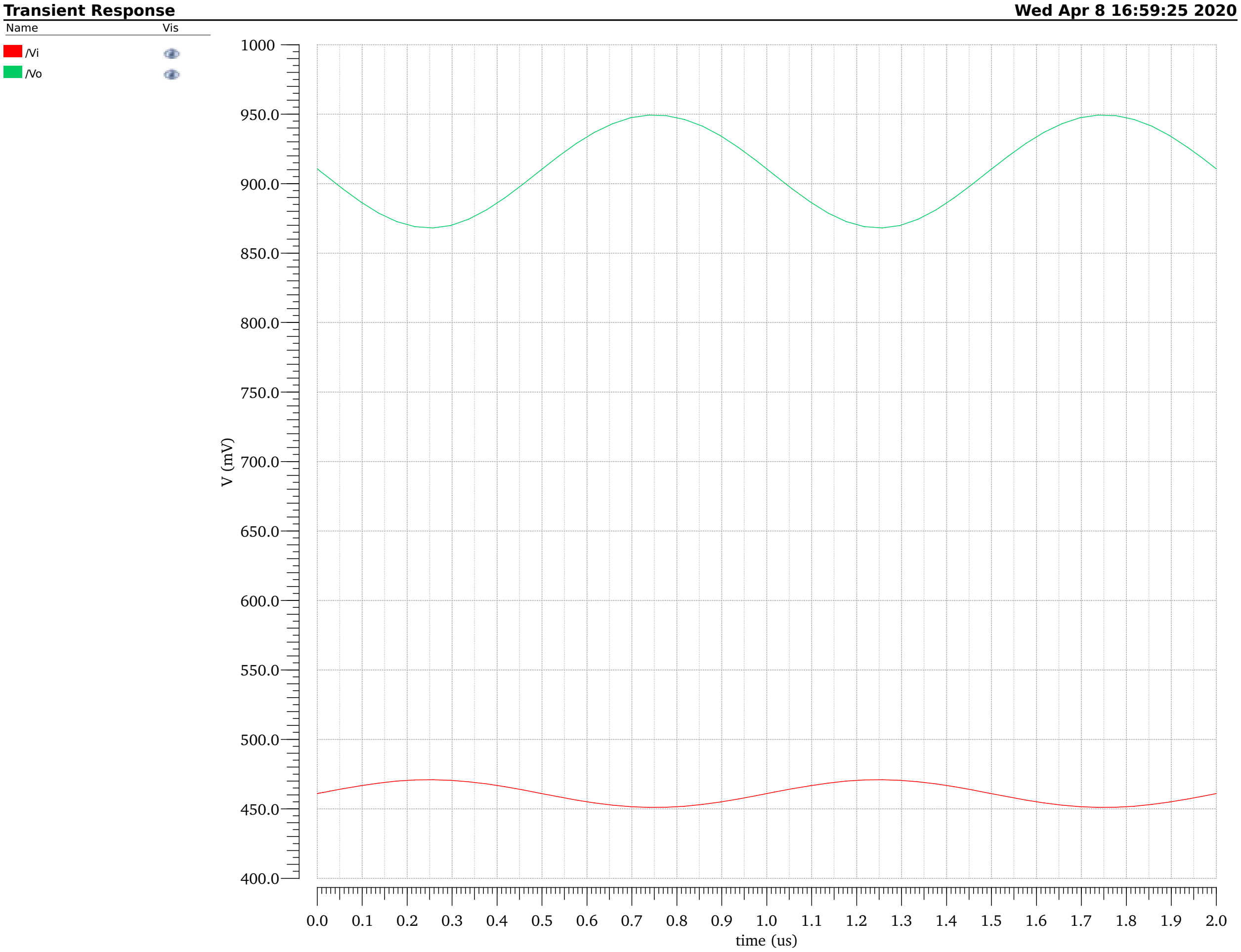
MATLAB output:

```
Resistance    = 5896.5168 ohm
Gate voltage  = 0.46138 V (DC)
Drain voltage = 0.72828 V (DC)
```

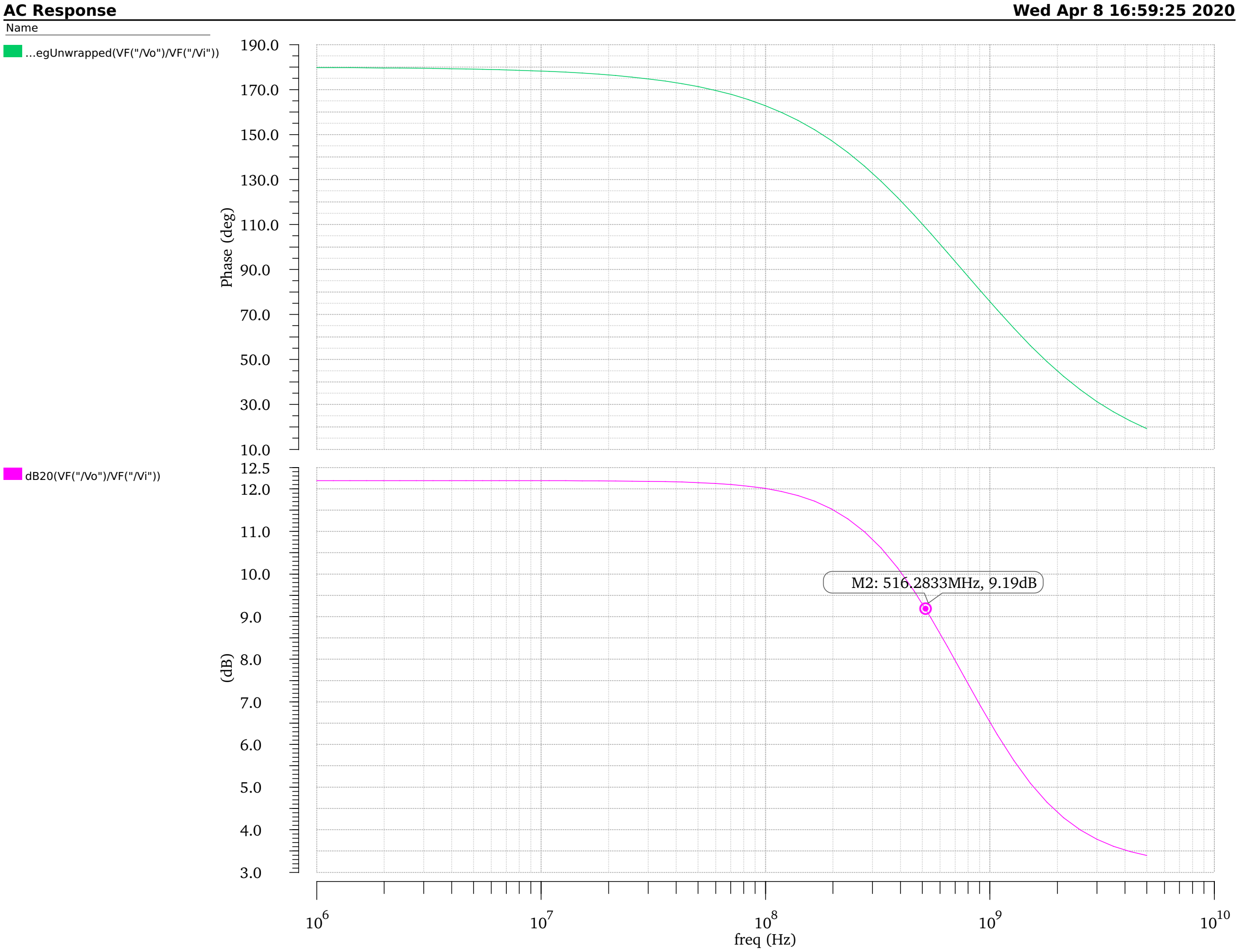
At $80\,\mu\text{A}$, a W/L ratio of $32\,\mu\text{m}/\mu\text{m}$ should produce a gain of $4\,\text{V}/\text{V}$ with a drain resistance of $5.9\,\text{k}\Omega$, which is less than the impedance of the capacitor at the upper-bandwidth frequencies. At this bias current, the gate voltage will need to be biased at $461\,\text{mV}$. In Cadence, the circuit was built with these values:



Running the simulation, the low frequency gain is $12.2\,\text{dB}$ with a 3dB frequency around $516\,\text{MHz}$. This exceeds the specifications.



Transient Response
Wed Apr 8 16:59:25 2020
Name
Vis
/Vi
/Vo
V (mV)
1000
950.0
900.0
850.0
800.0
750.0
700.0
650.0
600.0
550.0
500.0
450.0
400.0
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5
1.6
1.7
1.8
1.9
2.0
time (us)


AC Response
Wed Apr 8 16:59:25 2020
Name
...egUnwrapped(VF("/Vo")/VF("/Vi"))
dB20(VF("/Vo")/VF("/Vi"))
Phase (deg)
190.0
170.0
150.0
130.0
110.0
90.0
70.0
50.0
30.0
10.0
(dB)
12.5
12.0
11.0
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
M2: 516.2833MHz, 9.19dB
10^6
10^7
10^8
10^9
10^10
freq (Hz)