WASHINGTON STATE UNIVERSITY
SCHOOL OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

EE 352, ELECTRICAL ENGINEERING LABORATORY

LAB #7

MOSFET circuits

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Lab Overview

In this lab, we experimentally determined the characteristics of metal-oxide-semiconductor field-effect transistors (MOSFETs) for two types of transistors: the NMOS and PMOS. Throughout the lab, we saw various applications of MOSFETs, including a voltage-controlled resistor and a buffer amplifier. These applications use the unique characteristics and operating regions of MOSFETs.

1 MOSFET I-V characteristics

1.1 Purpose

In this experiment, we used the Tek 571 curve tracer and found the current-voltage (I-V) curves for the ZVN2110A (NMOS) and ZVP2110A (PMOS) transistor. From these curves, we determined the threshold voltage and other attributes of each transistor.

1.2 Theoretical background

In this experiment, we will use both NMOS and PMOS transistors. Each of these transistors require a minimum threshold voltage V_t across the gate to operate. Below this voltage, current is virtually unable to flow across the transistor as the channel is not established. Above this, we can vary the drain-source voltage relative to the gate-source voltage. Changing these parameters will affect how the current flows, depending on whether the transistor is operating in the triode or saturation region. These regions and their respective currents are shown in Table 1 below.

Table 1: Equations for currents through the drain terminal for both the NMOS and PMOS transistors.

Transistor Type	Conditions		Region	Current
NMOS	$V_{GS} < V_t$		Cutoff	$I_D = 0$
	$V_{GS} \geq V_t$	$V_{DS} < V_{OV}$	Triode	$I_D = k_n \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} (V_{DS})^2 \right]$
		$V_{DS} \geq V_{OV}$	Saturation	$I_D = \frac{k_n}{2} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$
PMOS	$V_{SG} < \lvert V_t \rvert$		Cutoff	$I_D = 0$
	$V_{SG} \geq \lvert V_t \rvert$	$V_{SD} < \lvert V_{OV} \rvert$	Triode	$I_D = k_n \left[(V_{SG} - \lvert V_t \rvert) V_{SD} - \frac{1}{2} (V_{SD})^2 \right]$
		$V_{SD} \geq \lvert V_{OV} \rvert$	Saturation	$I_D = \frac{k_n}{2} (V_{SG} - V_t)^2 (1 + \lambda V_{SD})$

In the saturation region, the transconductance g_m is defined as

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{I_D} \approx \frac{\Delta I_D}{\Delta V_{GS}}$$

We can use the equations from Table 1 and evaluate the derivative to find the transconductance as

$$\begin{aligned} g_m &= \frac{\partial}{\partial V_{GS}} \left[\frac{k_n}{2} (V_{GS} - V_t)^2 (1 + \lambda V_{DS}) \right] \\ &= k_n (V_{GS} - V_t) (1 + \lambda V_{DS}) \end{aligned} \tag{1}$$

Additionally, the transconductance can be estimated as

$$g_m = \sqrt{2 K_n I_D} \approx \frac{2 I_D}{V_{GS} - V_t} \tag{2}$$

From the datasheet of the ZVN2110A and ZVP2110A, the threshold voltages were in the range of

$V_t = 0.8$ to $2.4\,\mathrm{V}$ at $1\,\mathrm{mA}$	ZVN2110A
$V_t = -1.5$ to $-3.5\,\mathrm{V}$ at $-1\,\mathrm{mA}$	ZVP2110A

1.3 Procedure

The follow steps were carried out, as instructed by the lab assignment.

A. Obtain the current-voltage curve for the NMOS transistor.

1. Using the Tek 571 curve tracer, the I_D-V_{GS} curve was obtained for the ZVN2110A NMOS transistor. From this plot, the experimental threshold voltage can be obtained.
2. The transistor was attached to the curve tracer with both the drain/gate terminals shorted in the drain socket.
3. The curve parameters were set to:

Function:	Acquisition
Type:	NFET
V_{DS} max:	$5\,\mathrm{V}$
I_S max:	$10\,\mathrm{mA}$
V_g/step:	$0.2\,\mathrm{V}$
Offset:	$0\,\mathrm{V}$
Steps:	1
R_{load}:	$0.25\,\Omega$
P max:	$0.5\,\mathrm{W}$

   Then, the acquisition was started.
4. A diode curve plot was obtained and the threshold voltage V_t was found using a cursor on the plot. A photo was obtained of the screen as well.

B. Obtain current-voltage curves at multiple steps for the NMOS.

1. The NMOS transistor was connected in the normal configuration on the socket on the curve tracer.
2. The curve tracer was configured to step through several gate-source voltages.
3. The curve tracer parameters were set to:

Function:	Acquisition
Type:	NFET
V_{DS} max:	$10\,\mathrm{V}$
I_S max:	$50\,\mathrm{mA}$
V_g/step:	$0.1\,\mathrm{V}$
Offset:	$V_t + 0.1\,\mathrm{V}$
Steps:	5
R_{load}:	$0.25\,\Omega$
P max:	$0.5\,\mathrm{W}$

   And the acquisition was started.
4. Six curves were obtained for several values of V_{GS}.
5. Several photos were taken of these curves.

C. Obtain the current-voltage curve for the PMOS transistor.

Step A(1–4) was repeated for the PMOS transistor.

D. Obtain current-voltage curves at multiple steps for the PMOS.

Step B(1–5) was repeated for the PMOS transistor.

E. Estimating transistor parameters from obtained graphs

1. The pictures of the curve tracer screens were transferred onto a computer, so that the transconductance and threshold voltages could be estimated.
2. The threshold voltages were measured from the pictures, as well as the cursor feature.
3. The transconductance g_m was estimated using the slope of I_D-V_{GS} curve for the NMOS transistor. From this g_m value, the parameter k_n was estimated.
4. Step 3 was repeated for the PMOS transistor.
5. The channel modulation index λ was estimated for each transistor.
6. On the NMOS I-V_{DS} family of curves, six different points were chosen with three points in the saturation and three in the triode region. These points were recorded and used to calculate an average value of k_n.
7. Step 6 was repeated for the PMOS transistor.

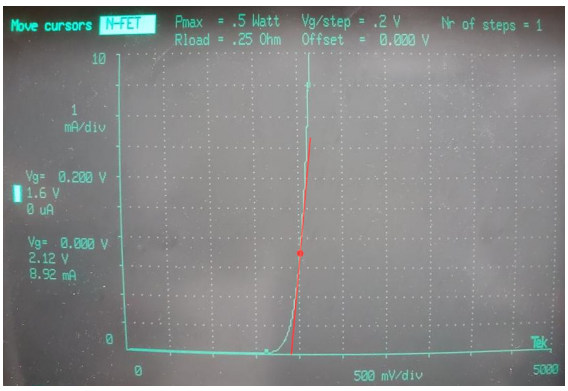
Post lab: OrCAD PSPICE simulation

Using the parameters estimated, the i_D-v_{DS} curves were obtained for both the n- and p-channel MOSFETs. These were compared to the experimental curves. The results of the simulation are shown in the appendix, closely matching the I-V curves near the threshold voltage, later departing the measured curves as the gate voltage increases.

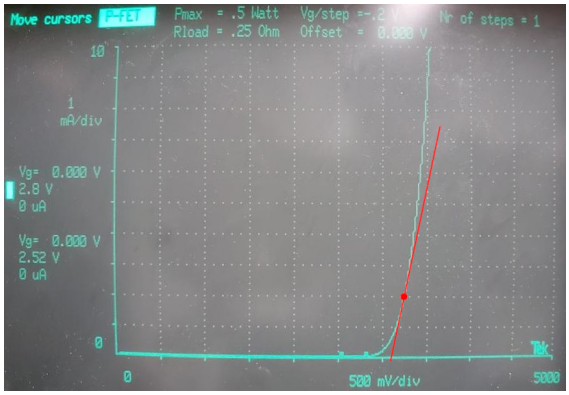
1.4 Results and analysis

For both transistors, the threshold voltage was captured using the on-screen cursors. From the curves, a transconductance were obtained using the slope at an arbitrary point in the forward-biased "on" region, as shown in Figure 1. The process transconductance k was found using equation (1). These values are noted below in Table 2.

From the I-V_{DS} family of curves, six points were taken for both the NMOS and PMOS transistors, from both the triode and saturation region. These screens are shown in Figure 2. From this, the process transconductance values k were calculated for each by taking points from both regions and using their respective equation from Table 1 and solving for k. These values are shown in Table 3. There is some variation between the k values and the error could be due to the inaccuracies when measuring using the curve tracer, as the rounded screen could lead to some imprecise measurements when eyeballing it.

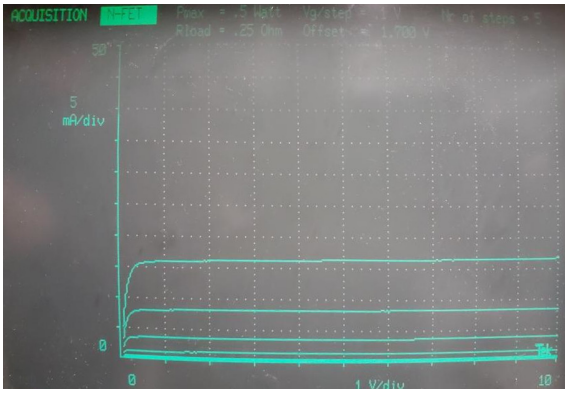


(a) NMOS I-V characteristics.

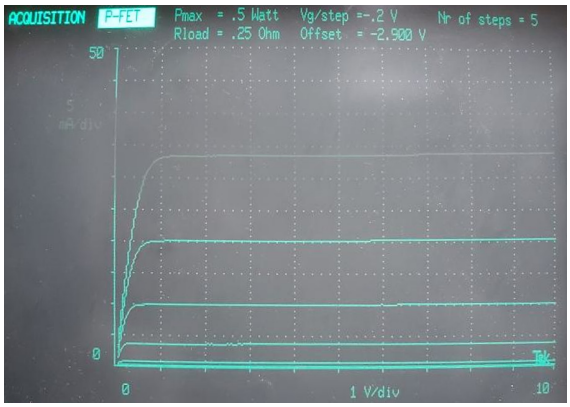


(b) PMOS I-V characteristics.

Figure 1: The I-V characteristics for each transistor in the diode configuration.



(a) NMOS I-V characteristics.



(b) PMOS I-V characteristics.

Figure 2: The I-Vds family of curves for both transistors.

Table 2: Experimental threshold and transconductance values of the NMOS and PMOS transistors in Experiment 1.

	Symbol	Transistor		Unit
		NMOS	PMOS	
Threshold voltage	V_t	1.60	2.80	V
Transconductance	g_m	0.0278	0.01364	Ω^{-1}
Process transconductance	k	0.1104	0.0465	$\mathrm{A\,V^{-2}}$
Channel modulation index	λ	0.00523	0.001472	$\mathrm{V^{-1}}$

Table 3: Experimental k values calculated using the family of curves in both the triode and saturation regions.

	I_D [mA]	V_{GS} [V]	V_{DS} [mV]	k [$\mathrm{A/V^2}$]	Region
NMOS	2.0	2.1	50	0.084	Triode
	5.7	2.2	100	0.104	
	9.0	2.3	100	0.138	
	4.2	2.1	10000	0.032	Saturation
	9.0	2.2	10000	0.048	
	17.60	2.3	10000	0.068	
PMOS	7.5	−3.5	200	0.063	Triode
	11	−3.7	200	0.069	
	13	−3.9	200	0.065	
	10	−3.5	1400	0.040	Saturation
	20	−3.7	1400	0.049	
	32.5	−3.9	1400	0.053	

1.5 Conclusion

In this experiment, we determined the various parameters that define both NMOS and PMOS MOSFETs. We first experimentally found the threshold voltage needed to turn the transistor 'on' at the gate. Then, we determined the transconductance g_m and process transconductance k values for both the ZVN2110A NMOS transistor and ZVP2110A PMOS transistor, as well as the channel modulation index λ. These values are the essential when modeling the transistor and will later be used in Experiment 2.

2 FET as a voltage-controlled resistor

2.1 Purpose

In this experiment, a transistor was operated in the deep triode region, allowing for a voltage-controlled resistor across the drain and source terminals. Here, we use a variable power supply to vary resistance in a circuit.

2.2 Theoretical background

In the circuit shown in Figure 3, we used the ZVN2110A NMOS transistor as a voltage controlled resistor. The gate voltage V_{GS} is allowed to vary from 0 to $5\,\mathrm{V}$ and the output voltage V_O is required to output a range $0.1\,\mathrm{V}$ to $0.02\,\mathrm{V}$. To accomplish this, we used a process transconductance of

$$k_n = 0.1104\,\mathrm{A\,V^{-2}}$$

This value was experimentally determined from Experiment 1. Using a voltage divider with the transistor as the lower resistor, we can determine an ideal resistance value for R. This was accomplished by using an initial gate voltage of $3.5\,\mathrm{V}$, allowing for some room in both directions. At this gate voltage, the transistor has an approximate resistance of

$$r_{DS} = \frac{1}{k_n\,(V_{GS} - V_t)} \approx 4.76\,\Omega$$

Through the the voltage divider, we can determine R at the minimum output voltage,

$$\begin{aligned} 0.02 &= \frac{4.76}{R + 4.76}(0.2) \\ R &= 42.84\,\Omega \end{aligned}$$

With this resistance fixed, we can now determine the gate voltage required for a half-attenuated output, where the output voltage is maximum at $0.1\,\mathrm{V}$. Again, using the voltage divider, it is clear that the resistance must be equal and the gate voltage is given as

$$\begin{aligned} 42.84 &= \frac{1}{(0.1104)(V_{GS} - 1.60)} \\ V_{GS} &= 1.81\,\mathrm{V} \end{aligned}$$

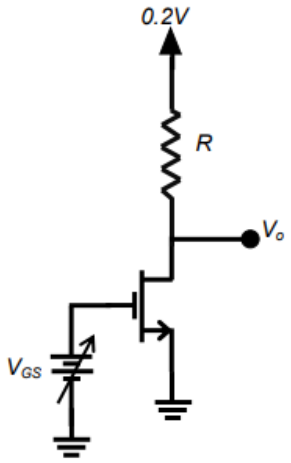


Figure 3: The circuit used in Experiment 2.

2.3 Procedure

The follow steps were carried out, as instructed by the lab assignment.

1. Using the same NMOS circuit, construct the circuit shown in Figure 3.
2. Using the DC power supply, apply the calculated V_{GS} values obtained earlier and use the DMM to measure the corresponding output voltage V_o. Calculate the error and record the data in the lab notebook.
3. Vary V_{GS} until the output voltage V_o reaches the nominal values and record the error between the expected and measured gate voltage.

2.4 Results and analysis

In this lab, we required a nominal resistance R of $42.84\,\Omega$. Using several resistors in series, the measured resistance was

$$R = 42.61\,\Omega \quad (0.54\%\text{ error})$$

Using the k_n value found in the last experiment and the gate voltages from the prelab, there was a high percent error, as shown in Table 4. Our estimations for the gate voltages did not accurately reflect the measured output voltage, with an average error of 60%. This high error is likely due to inaccuracies when measuring the k_n-value in the triode region.

Table 4: Measured output voltages using ideal input gate voltages.

V_{GS}	Expected V_o	Measured V_o	% error
3.50 V	0.02 V	0.0141 V	29.5%
1.81 V	0.1 V	0.191 V	91.0%

Next, we varied the gate voltage until the measured output voltage reached $0.1\,\text{V}$ and $0.02\,\text{V}$. The gate voltages are shown in Table 5. During this part of the experiment, it was noted that minor changes in the gate voltage significantly impacted the measured output voltage. The transistor was very sensitive to changes across the gate and source. Here, we measured the error between the expected gate voltage and measured gate voltage. Again, the high error is likely due to a high error from Experiment 1 when determining the k_n value for this transistor in the triode region.

Table 5: Measured output voltage with the gate voltage varied.

V_{GS}	Expected V_o	Measured V_o	% error
2.62 V	0.02 V	0.019 96 V	25.1%
2.00 V	0.1 V	0.103 10 V	10.5%

2.5 Conclusion

This experiment utilized the NMOS transistor as a voltage-controlled resistor. While our expected voltages were roughly in the same order as the measured values, there was some significant deviation. This error was likely due to the imprecision when initially determining the k_n values in Experiment 1, as noted earlier. Despite this, when we found the *correct* values, the difference between the expected and measured gate voltage was only roughly 10–30% off. Even if the k_n were precisely accounted for, even a small difference in gate voltage would lead to significantly different output voltages, as noted by the difference in error between both parts of the experiment.

3 MOSFET as a buffer amplifier

3.1 Purpose

In this experiment, we explore using a MOSFET as a buffer amplifier. This amplifier is used to isolate an input signal source, which is unable to supply a load with a large current. With a MOSFET, the input signal can use the transistor as a buffer, allowing the transistor to drive the output load with a voltage proportional to the input.

3.2 Theoretical background

Shown in Figure 4, we will build a buffer amplifier, which will be used to drive a load with an equivalent voltage as the input V_I. We will use the IRF510 NMOS power transistor, in a TO220 package, and drive a decade box load with $50\,\Omega$ of resistance. If we determine the power utilized by the source, we can see that the power is minuscule, relative to the load power. This is shown below in Table 6. This is due to the input current only being drawn by the resistor R_G and only minimal (zero) current going into the transistor itself.

Table 6: Power supplied by the source and power supplies at three input voltages.

Input V_I (V)	Input P_I (W)	Power Supply P_{dd} (W)
0	0	0
15	0.10	4.5
25	0.28	12.5

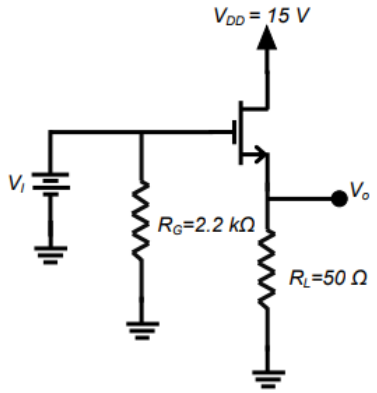


Figure 4: The buffer amplifier circuit, utilized in Experiment 3. Note: V_{DD} is set to 15 volts in this figure, however, it was changed to 25 volts on the day of the experiment.

3.3 Procedure

The follow steps were carried out, as instructed by the lab assignment.

1. Construct the circuit shown in Figure 4 using an IRF510 NMOS transistor. Use a decade box as the load resistor, set to 50 ohm. Measure and record the resistor values using the DMM. Use a DC power supply to supply $V_{DD} = 15$ V and the other amplifier at the gate of the transistor.
2. Use DMM1 and DMM2 to measure the input and output voltage simultaneously. Determine the threshold voltage by starting V_I at zero and slowly increasing the voltage until V_O departs from zero. Record this voltage.
3. In increments of a volt, we increased the gate voltage to 25 V and recorded this data in a table and calculate the power supplied by the input, and determine the regions.
4. Using Excel, this data was recorded and plotted.

3.4 Results and analysis

Using the DMM, the resistor voltages were measured as,

$$R_G = 2.1941\,\text{k}\Omega \qquad (2.2\,\text{k}\Omega \text{ nominal, } 0.3\% \text{ error})$$
$$R_L = 50.26\,\Omega \qquad (50\,\Omega \text{ nominal, } 0.5\% \text{ error})$$

Next, the threshold voltage was found to be roughly $2.25\,\text{V}$,

$$V_I = 2.25\,\text{V} \rightarrow V_O = 1 \times 10^{-6}\,\text{V}$$
$$V_I = 2.5\,\text{V} \rightarrow V_O = 9 \times 10^{-6}\,\text{V}$$

In increments of a volt, we measured the corresponding output voltages and determined the regions using the NMOS equations from Table 1. This data was collected in Excel (shown in the Appendix), then plotted in Figure 5. The power supplied by the input was calculated, as well as the power delivered to the load, then plotted in Figure 6. Note that the power delivered to the load is not supplied by the input source, but rather is supplied by the power supply V_{DD}. Ideally, zero current (and power) from the source is delivered across the gate of the transistor.

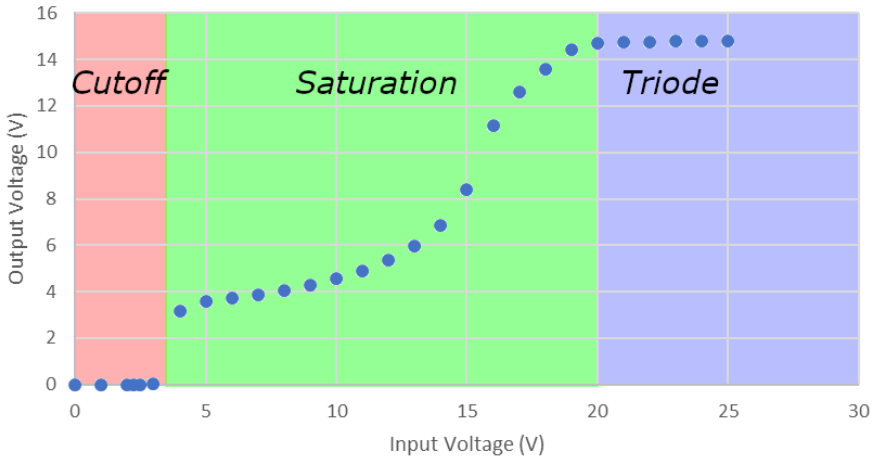


Figure 5: The input/output voltages of the buffer amplifier and their corresponding regions.

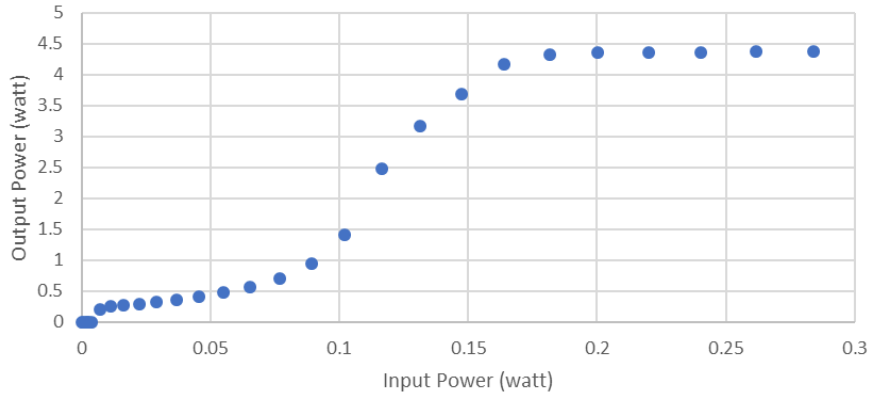


Figure 6: The input power vs the output power.

3.5 Conclusion

In this last experiment, we used the NMOS transistor as a buffer amplifier, allowing an low-current input to drive a high-current output. This application takes advantage of the zero-input-current characteristics of the transistor gate. Rather, the power supplied to the load is coming from the power supply at V_{DD}. In this part, the transistor is operated under each: the cut-off region, saturation, then lastly, the triode region. The transistor behaves differently in each region, where the transistor is off until the threshold current is reached.

Appendix

Table 7: Data collected during Experiment 3.

V_i (V)	V_o (V)	Region	P_i (W)	P_o (W)
0	0	cutoff	0	0.00
1	0	cutoff	0.000454545	0.00
2	0	cutoff	0.001818182	0.00
2.25	0.00001	cutoff	0.002301136	0.00
2.5	0.00009	cutoff/saturation	0.002840909	0.00
3	0.01187	cutoff/saturation	0.004090909	0.00
4	3.17	saturation	0.007272727	0.20
5	3.57	saturation	0.011363636	0.25
6	3.70	saturation	0.016363636	0.27
7	3.86	saturation	0.022272727	0.30
8	4.05	saturation	0.029090909	0.33
9	4.28	saturation	0.036818182	0.37
10	4.56	saturation	0.045454545	0.42
11	4.90	saturation	0.055	0.48
12	5.35	saturation	0.065454545	0.57
13	5.96	saturation	0.076818182	0.71
14	6.87	saturation	0.089090909	0.94
15	8.42	saturation	0.102272727	1.42
16	11.14	saturation	0.116363636	2.48
17	12.60	saturation	0.131363636	3.17
18	13.57	saturation	0.147272727	3.68
19	14.43	saturation	0.164090909	4.16
20	14.71	triode	0.181818182	4.33
21	14.75	triode	0.200454545	4.35
22	14.77	triode	0.22	4.36
23	14.78	triode	0.240454545	4.37
24	14.79	triode	0.261818182	4.37
25	14.79	triode	0.284090909	4.37