# Lab Assignment 10: BJT Amplifier circuits

Revision: April 9, 2020


**Summary**

This lab assignment is the continuation of lab assignment number 9 in the sense that you obtained BJT characteristics in the previous lab and in this lab you will design and study a common emitter amplifier with a given set of specifications. You will also study differential amplifiers with a common emitter resister as well a current mirror. An improvement in common mode rejection ratio (CMRR) is observed in the differential amplifier when a common emitter resistor is replaced by a current mirror.


**Learning Outcomes:** After completing this lab, you should be able to:

- Design and simulate a common emitter amplifier with a given set of specifications.
- Build and design a differential BJT amplifier with an emitter resistor to bias it.
- Do differential and common mode gain measurements.
- Design and simulate an improved differential amplifier with current mirror replacing an common emitter resistor.

**Required Equipment**

- EE352 analog parts kit
- Breadboard
- Function generator, oscilloscope
- DMM
- DC power supplies

 

## I. Single Stage Common Emitter Amplifier

In this part of the lab, you will design a common emitter BJT amplifier as shown in Figure 1 using a 2N3904 npn transistor from your parts kit,. The design specifications are:

a) Load Resistance, $R_L$: 47KΩ
b) Input Resistance, $R_i$> 1.2KΩ
c) Mid-band voltage gain, $G_V = V_o/V_s$: -85 +/- 20%
d) Power Supply Voltage: $V_{CC}$ = +12 Volts
e) Coupling and bypass capacitors: $C_B$ =10uF ; $C_C$=10uF and $C_E$=47uF

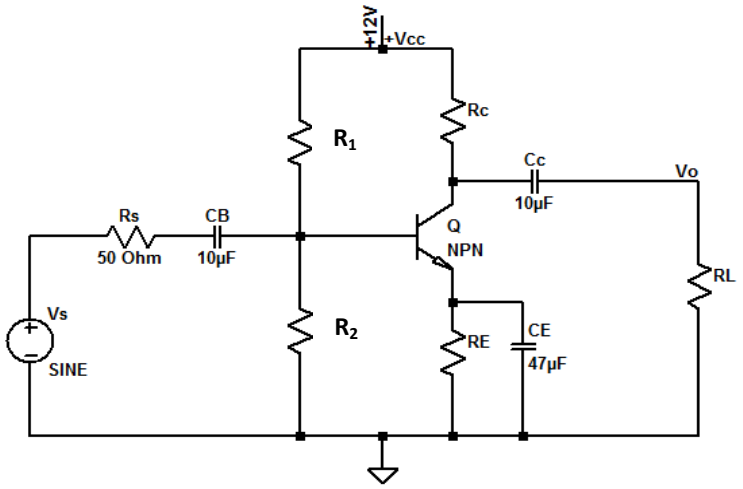


Figure 1. Single stage Common Emitter Amplifier

*Pre-lab:*

(a) Begin the design by choosing an appropriate value for the bias current $I_E$ to meet the gain, input and output resistance requirements. Assume $\beta = 100$ and $V_A$= 100 V (λ=0.01 $V^{-1}$). The input resistance is given as:

$$R_i = R_1 \text{ II } R_2 \text{ II } r_\pi \quad (1)$$

where $r_\pi = V_T / I_B = V_T (\beta+1) / I_E$ (2)

and the small signal mid-band output resistance at the collector is:

$$R_0 = R_C \text{ II } R_L \text{ II } r_0 \quad (3)$$

where $r_0 = V_A / I_C$

and voltage gain is: $G_v = -g_m R_{0,}$ (4)

and $g_m = I_C / V_T$ (5)

For a design one may consider:

(i) $R_C . I_C = V_{CC}/3$, for maximum symmetrical swing at the output.
(ii) Collector and emitter currents are approximately equal and, i.e β=100.
(iii) Assume $V_A$ =100 Vis large.

 

(iv) current through $R_1$ and $R_2$ is ~ $I_E/10$ and
(v) for DC biasing base voltage is ~ 1/3 $V_{CC}$

Based on these equations and considerations calculate the values for $R_1$, $R_2$, $R_E$ and $R_C$.

*Lab Procedures:*

1. Simulate the circuit given in Figure 1 using PSPICE use Q2N3904 available in the npn library.
2. **Validate DC bias points:** With no AC signal applied to the circuit, connect the DC supply voltage as shown in Figure 1. Run DC operating point to determine the DC bias point of the transistor. Compare the DC values to your design values. Then, estimate the value of $g_m$ from your DC measurements.

3. **Validate the gain at 20 kHz.** Using Transient analysis, apply a 20 mV peak-to-peak, 20KHz sinusoidal input signal at the input. Set the simulation stop time to include at least 10 complete cycles and resolution to be at least 1000 samples per one complete cycle. Measure the output voltage across the load. Compute the mid-band voltage gain. If the gain is not within the specs of -85V/V ±20%, then adjust $R_E$ and /or $R_C$ as needed.

4. **Find the clipping voltages at the collector**. Set the frequency to be 20KHz sinusoidal signal and increase its input level voltage to 1V, Measure and record this voltage at the collector. The collector's voltage should be clipping. Find Its the maximum and minimum voltage swing.

5. **Measure the resistance:** To measure the input resistance, measure the current leaving the voltage source using current sensor and the input voltage at the base. Then,

$$\boldsymbol{R_I \cong \frac{|V_b|}{|i_s|}}$$

6. **Obtain Frequency Response:** Using LTSPICE, apply 1 AC voltage for AC sweep. Determine the low cutoff frequency and the high cutoff frequency $f_H$. You need to investigate the range of AC sweep (frequency sweep).

7. **Common Emitter with Resistance in the Emitter:** Divide RE into RE1 = 47Ω and RE2= RE-47Ω as shown in Figure 2. Calculate and measure new mid-band voltage gain and input resistance.

 

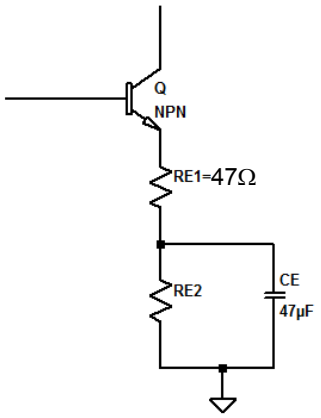


Figure 2. Un-bypassed Emitter Resistance Circuit of a BJT Common Emitter Amplifier

 

## II. Differential Amplifier

In this part of the lab, you will simulate a basic differential amplifier and differential mode ($A_d$) and common mode ($A_C$) voltage gains are measured at 1KHz. You will use 2N3904 npn transistors mimic the matched transistors to build the differential amplifier.

*Lab Procedures:*

1. **DC Circuit Only:** Using LTSPICE, build the basic differential amplifier circuit as shown in Figure 3. For the two transistors Q1 and Q2 use readily available npn 2N3904 model. Ground both inputs ($V_i$+ and $V_i$-) use transient analysis and measure (plot) $V_{out.}$

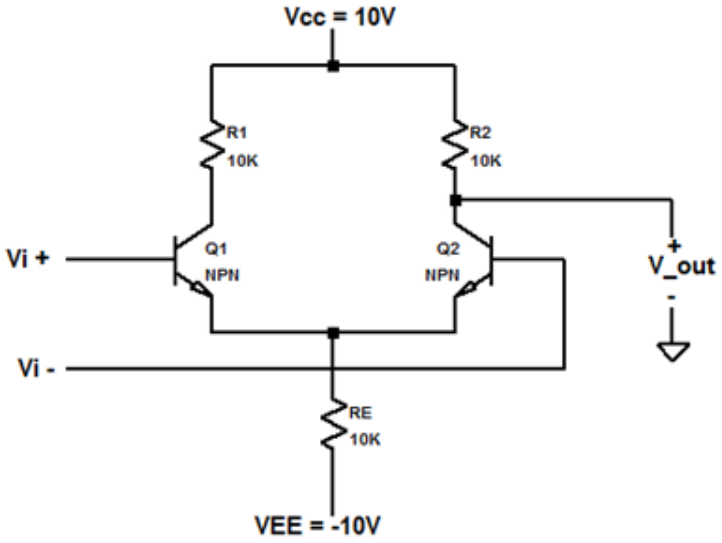


Figure 3. Basic Differential Amplifier

2. **Testing Differential Gain:** Add the differential input voltage ($v_d$) across the inputs ($V_i$+ and $V_i$-) of 20 mA peak-to-peak sine wave at 1kHz. Make sure the $V_i$- is grounded. Measure the peak to peak output voltage. Calculate the gain and record it on your summary. The theoretical gain is given as $\frac{V_{out}}{v_d} = A_d = -\frac{1}{2} g_m R_2$. Where $g_m = \frac{I_C}{V_T}$. Adjust the transient analysis to simulate few cycles (Stop time = 10ms, Maximum step size = 1us).

3. **Testing the Common Mode Gain:** Common mode voltage gain is measured by using Figure 4, where the box represents the basic amplifier of figure 3. Add the common mode input voltage of 1KHz, 1V peak to peak sinusoidal signal to both + and - inputs. Measure the peak-to-peak) output voltage $V_{out}$. Record the input and output voltages and calculate common mode gain $A_C = (V_o/V_{in})$. The common mode gain $\frac{V_{out}}{v_{CM}} = A_{CM} = -\alpha \frac{R_2}{2R}$. Record the common mode gain in your summary.

 

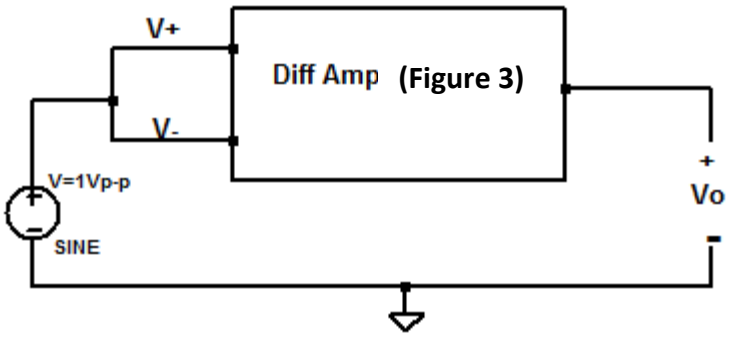


Figure 4 Measurement set-up for common mode gain measurement

4. Compute common mode rejection ratio (CMRR) in dB as CMRR=20log$_{10}$($A_d/A_C$). Include the CMRR in your summary.

### III. Improved Differential Amplifier

The differential amplifier circuit of Figure 3 suffers from poor CMRR as the biasing current is affected by the common mode voltage. As the common mode voltage affects the current through the biasing resistor (R). In this part of the lab, an improved differential amplifier is built by replacing the biasing resistor by a current mirror circuit. The bias current in this circuit is designed to have the same as the same current as in the basic differential amplifier of part II. The differential and common mode gains are measured and the CMRR is computed. A very low common mode gain is expected for this configuration.

Pre-Lab:

(a) Refer to the circuit of Figure 5. Design the value of R that leads to the same biasing current of part II (0.93 mA). The currents in Q3 and Q4 are assumed to be the same as they are matched transistors. By assuming β is very large, the collector currents in Q3 and Q4 are calculated as:

$$I = \frac{V_{CC} - V_{BE4} - V_{EE}}{R}$$

$$R = \frac{10 - 0.7 - (-10)}{0.93\ mA}$$

Find R so as to make the collector currents in Q3 and Q4 equal to the sum of the emitter currents in Q1 and Q2.

Lab Procedure:

1. **DC Circuit Only:** Using LTSPICE, build the improved differential amplifier circuit as shown in Figure 5. Use readily available npn 2N3904 model for the four transistors, and use the calculated prelab value for R. Ground both inputs ($V_i$+ and $V_i$-) use transient analysis and then measure (plot) $V_{out.}$

 

2. **Testing Differential Gain:** Add the differential input voltage ($v_d$) across the inputs ($V_i$+ and $V_i$-) of 20 mA peak-to-peak sine wave at 1kHz. Make sure the $V_i$- is grounded. Measure the peak to peak output voltage. Calculate the gain and record it on your summary.

3. **Testing the Common Mode Gain:** Add the common mode input voltage of 1KHz, 1V peak to peak sinusoidal signal to both + and - inputs. Measure the peak-to-peak) output voltage $V_{out}$. Measure common mode gain.

4. Compute the CMRR and compare it to the value obtained from part II

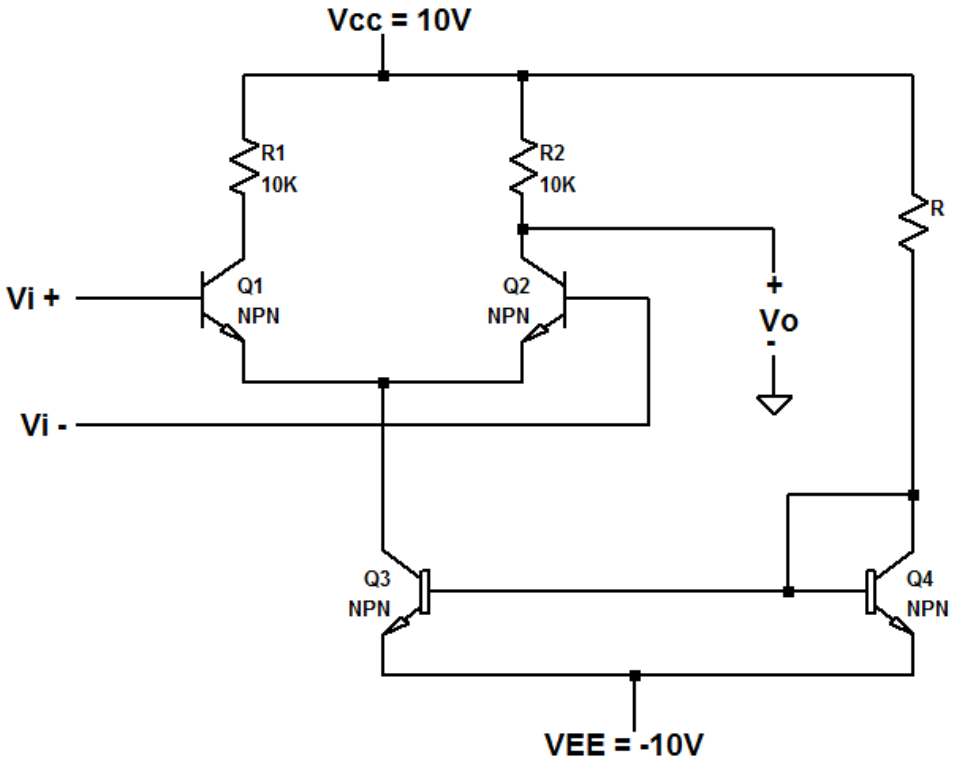


Figure 5. Improved Differential Amplifier with current mirror

 