Lab Assignment 8: MOSFET Amplifier Circuits

Revision: October 25, 2018

Summary

Practical MOSFET circuits are not only used in discrete electronic circuits, they are also the driving force behind digital and analog VLSI design. In this lab, you will design, simulate and experimentally validate a single stage common source MOSFET amplifier as an example of a discrete amplifier circuit. Then, you will design a current mirror source using CD4007 matched transistors IC chip; current mirrors are used as biasing circuits within analog VLSI systems. Then, you will build a CMOS inverter using complementary NMOS and PMOS transistors within the CD4007 to determine its voltage transfer curve, and finally you will properly bias the inverter to make it work as a single stage CMOS amplifier.

Learning Outcomes: After completing this lab, you should be able to:

- Design, simulate and analyze single stage common source MOSFET amplifiers.
- Design and build a CMOS current mirror source.
- Build and test a CMOS inverter.
- Properly bias the CMOS inverter to work as a single stage CMOS amplifier.

Required Equipment

- EE352 analog parts kit
- Breadboard
- Function generator, oscilloscope
- DMM
- DC power supplies

I. Single Stage Common Source Amplifier

Figure 1 shows a single stage common source MOSFET amplifier circuit. We wish to design the circuit to meet the following design specifications:

Load Resistance: R_L= 100 K Ω
Input Resistance: R_i > 200 KΩ
Mid-band Gain: G_v= V_o/V_i = -50 ± 20%
Supply Voltage: +15 Volts
Circuit Capacitors: C_G = 10 μF; C_S = 47 μF; C_D = 10 μF

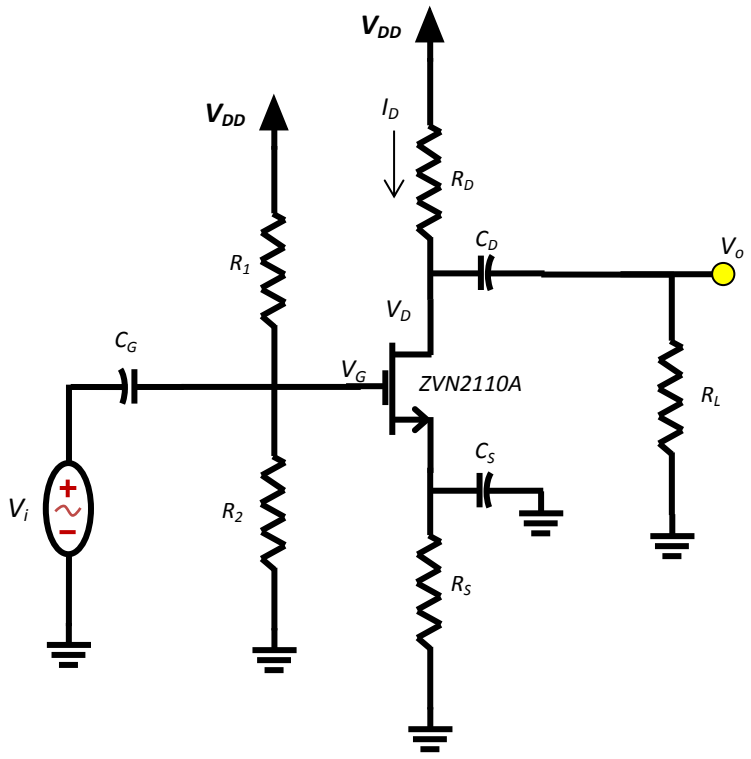

Figure 1. Common Source MOSFET Amplifier

Pre-lab:

(a) Design the amplifier to meet the specifications above by choosing values for resistors R_1, R_2, R_D and R_S. Begin your design by choosing an appropriate value for the bias current I_D. If $I_D \approx 0.3$ mA, assume $V_T \approx 1.7$ V, $K_n \approx 0.02$ A/V^2 and V_A= 100 V (λ=0.01 V^{-1}). Find the small signal approximation of the input resistance R_{in} where

$$R_{in} = R_1 \,||\, R_2. \quad (1)$$

Find the small signal approximation of the output resistance R_o, where R_o is given as

$$R_o = R_D \,||\, R_L \,||\, r_o. \quad (2)$$

The small signal mid-band gain of the amplifier is given by

$$G_v = -g_m R_o \quad (3)$$

where

$$g_m = \sqrt{2k_n I_D} = k_n(V_{GS} - V_T). \quad (4)$$

Once you choose I_D the DC biasing of the transistor can be found using simple rules of thumb. The voltage V_G should be approximately equal to $V_{DD}/3 > V_T$. For maximum symmetry, V_D should be biased at the midpoint between V_D (Max) and V_D(Min). Clearly, the maximum V_D is V_{DD} and the minimum $V_D > V_G - V_t$. For example, if V_t =1.7 V and V_G=1/3 V_{DD}=5 V, then $V_D \approx 9$ V for maximum symmetry.

(b) Using PSPICE (LTSPICE or Orcad), simulate the circuit using $V_T \approx 1.7$ V, $K_n \approx 0.02$ V/A and V_A= 100 V (λ=0.01 V^{-1}). The simulation should include an AC sweep of the gain in dB and the simulation should show the low cut-off frequency, the midband gain (100 Hz to 10Meg Hz). In you simulation, you may adjust the values of R_S and R_D until the gain is -50 V/V.
Hint: When using MOSFETs, decreasing the current by increasing R_S allows you to increase R_D, which increases the gain of the amplifier.

Lab Procedures:

1. Measure all resistors with your DMM and record their values in your lab notebook. Use the RLC meter to measure the exact capacitance values.

2. With no AC signal applied to the circuit, apply the DC supply voltage. Then measure and record all DC voltages in the circuit with your DMM. At this point, your DC measurements should be very close to your expected DC values. Then, estimate the value of g_m from your DC measurements, using equation (4) above.

3. Apply a 20 mV peak-to-peak sinusoidal input signal at 20 kHz. Measure the output voltage with your oscilloscope. Compute the midband gain. If the gain is not within the specs of -50V/V ±20%, then adjust R_S and R_D as needed. To increase the gain, increase both R_S and R_D by a factor of α in order to increase the gain by $\sqrt{\alpha}$ and vice versa.

4. *Demonstrate your circuit to the TA and have him or her initial your lab checklist.*

5. Determine the low cutoff frequency (f_L) and the high cutoff frequency (f_H) of the amplifier. To determine f_L, measure V_o at the midband (20 kHz), then decrease the frequency until the output voltage is 0.707 $(1/\sqrt{2})$ of V_o at the midband. This is the low cutoff frequency; record this frequency in your notebook. To determine f_H, increase the frequency until the output voltage is 0.707 $(1/\sqrt{2})$ of V_o at the midband. This is the high cutoff frequency; record this frequency in your notebook.

6. Plot the frequency response of your amplifier (i.e., plot the gain in dB vs. log10 of the frequency). Start from two decades below f_L up to two decades after f_H. Make sure to have enough pts around f_L *and* f_H to capture the curve smoothly. It is recommended that you plot the data on Matlab or MS Excel as you collect the data. This shows the smooth curve as you are collecting the data. Include the frequency response plot in your lab report.

7. *Demonstrate your frequency response plot to the TA and have him or her initial your lab checklist.*

8. Increase the amplitude of the input signal until the output voltage is clipping at the top and the bottom. Measure the clipping voltage at the drain of the transistor, using DC coupling. Include the plot of the clipping voltage in your report.

II. Current Mirror Circuit

In analog VLSI design, amplifiers are biased using current mirror sources due to their efficient structure in terms of area and power consumption. In this experiment, you will build a current mirror source to supply constant DC current using matched NMOS transistors within the CD4007 IC chip. The circuit diagram for the current mirror source is shown in Figure 2. It contains two transistors Q1 and Q2 that are ideally identical as they have the same processing parameters (V_t, K_n, γ, …) Typically, VLSI designers adjust the W/L ratio for each transistor to provide desired bias current. In the circuit shown, Q1 acts as a reference transistor that provides I_{Ref} through R which biases the gate voltage to some determined value V_G. The gate voltage is reflected to Q2 which acts as the biasing current source that biases the circuit. The current of Q2 (the bias current) is adjusted by designing the proper W/L ratio of Q2. The current in Q_2 is determined by the following equations

$$\frac{I_2}{I_1} = \frac{\frac{1}{2}K_n'\left(\frac{W}{L}\right)_2 (V_{GS}-V_T)^2(1+\lambda V_{DS2})}{\frac{1}{2}K_n'\left(\frac{W}{L}\right)_1 (V_{GS}-V_T)^2(1+\lambda V_{DS1})} = \frac{\left(\frac{W}{L}\right)_2 (1+\lambda V_{DS2})}{\left(\frac{W}{L}\right)_1 (1+\lambda V_{DS1})} \approx \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1},$$

which can be expressed as

$$I_2 \approx \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_1. \qquad (6)$$

Hence, you can easily design I_2 by controlling the size of the transistors. In this experiment you need to make $I_2 \approx 2I_1$.

Pre-lab:

(a) Design the resistor R (between V_{DD} and drain of Q_1) to provide drain current I_{ref} = 1mA through NFET Q_1. Assume that V_{DD} = 5V, K_n = 0.08 A/V^2, V_T = 1.7 V, and λ = 0 (i.e., we neglect the effect of λ since it is much less than 1).

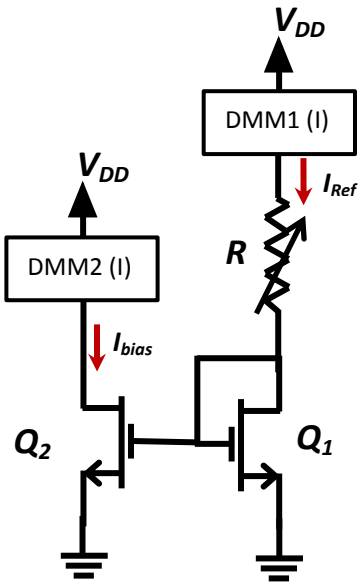

Figure 2 Current mirror source.

Lab Procedures:

1. Using CMOS Dual Complementary CD4007 IC chip, Figure A-1 in Appendix A, construct the current mirror circuit of Figure 2 with a reference current I_{Ref} =1 mA, V_{DD}= 5 V and I_{Bias} ≈ 1 mA. The CD4007 has three NMOS transistors, use one of them for Q1. To build Q2 connect the other two NMOS transistors in parallel to make I_{Bias} ≈2 $I_{Ref.}$

2. *<u>Very important:</u> 1) Make sure to ground Pin 7 of the CD4007 IC which will ground the bodies of all three NFETs, thereby preventing body feedback effects which can cause noise in the circuit's output. 2) Recheck all connections before applying power to the CD4007. 3) When power is first applied, check the current draw on the power supply; if you see any current reading over 10 mA, immediately switch off the supply and recheck your circuit, in order to prevent burning out the CD4007.*

3. For the resistor R, use a potentiometer (pot) or resistor box to provide variable resistance, and vary the resistance (starting from the value of R you designed in the pre-lab) until I_{Ref} = 1 mA.

4. Measure your currents using the DMM and record them in your lab notebook.

5. *Demonstrate your circuit to the TA and have him or her initial your lab checklist.*

III. <u>CMOS Inverter</u>

CMOS technology uses NMOS and PMOS transistors that act as complementary switching transistors on the same wafer (substrate) or chip. The complementary transistors work in a push-pull mechanism such that when one transistor is ON then it becomes a short circuit, but when it is OFF it acts as open circuit. The push-pull switching mechanism is useful in building digital circuits. The simplest digital CMOS circuit is the inverter which is made of a PMOS transistor and an NMOS transistor as shown in Figure 3.

When the CMOS inverter's input V_i is zero (logical low) then the NMOS transistor is OFF ($V_{GSn} < V_{tn}$) but the PMOS transistor is ON ($V_{SGp} > |V_{tp}|$) and $I_D=0$ because NMOS is off. Since $I_D= 0$ and PMOS is ON, then the PMOS is operating in the triode region and $V_{SDp}=0$ which implies $V_o= V_{Dp} = V_{Sp} = V_{DD}$ or Logical High. Similarly, when $V_i = V_{DD}$ (logical High) then the NMOS is ON, PMOS is OFF and $I_D=0$ because PMOS is OFF. Hence, the NMOS is in the Triode region and $V_{DSn} = 0$ which implies that $V_D=V_S =V_o = 0$ (logical Low).

During the transition from 0 V (low) to V_{DD} (high), the CMOS inverter transitions through five operating regions as shown in Figure 3; these regions are summarized in Table1. Note that the current is non-zero when the output of the inverter is transitioned; hence, the power dissipation is non-zero. This explains why the power dissipation is proportional to switching frequency. Note that in Region 3 $\left|\frac{dV_o}{dV_i}\right|$ is maximum, so it acts as an amplifier. In this experiment, you will build a CMOS inverter and you will investigate the different regions of the inverter. Then you will bias the inverter in Region 3 and test it as an amplifier.

Table 1 Summary of the five CMOS inverter transition regions

	NMOS	PMOS	V_i	I_D	V_o
Region 1	OFF	Triode	LOW	0	High V_{DD}
Region 2	Saturation	Triode	LOW	Small	High ≈ V_{DD}
Region 3	Saturation	Saturation	Medium	High	Mixed > 0 & < V_{DD}
Region 4	Triode	Saturation	High	Small	Low ≈ V_{DD}
Region 5	Triode	OFF	High	0	Low (0 V)

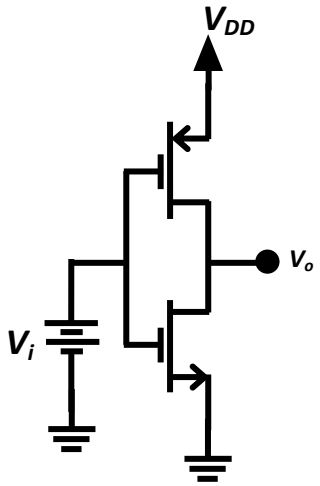

Figure 3 CMOS inverter

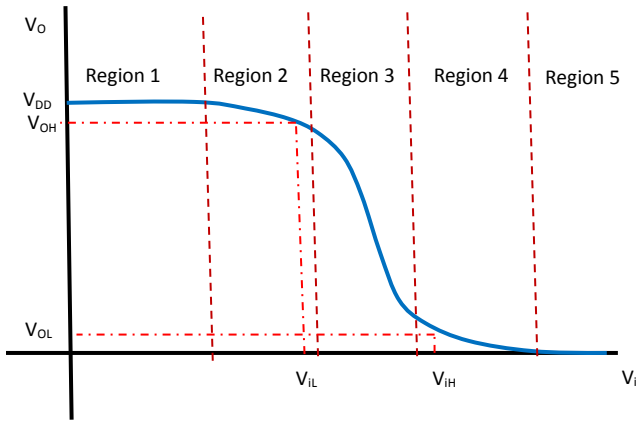

Figure 4 The voltage transfer curve of CMOS inverter

Lab Procedures:

1. Set up the CMOS inverter circuit shown in Figure 3. Use CMOS Dual Complementary Pair Plus Inverter CD4007. The complementary pair must be Q2 (P and N) on the CD4007; Q1

cannot be used because Pin 14 (Q1(P) drain) must be hooked to V_{DD} (see step 2 below), and Q3 cannot be used because it has the PFET source tied to the NFET drain (Pin 12). Use one supply voltage to be V_{DD} and set V_{DD}=5 V, and the other DC supply voltage to be the DC input voltage.

2. *Very important: 1) Make sure to ground Pin 7 of the CD4007 so that the NFET body is grounded. Also, make sure to hook Pin 14 of the CD4007 to V_{DD}, so that the PFET body is at V_{DD}. These steps prevent body feedback effects which can cause noise in your circuit's output. 2) Recheck your circuit before applying power to the CD4007, and immediately shut off the power if the current draw is more than 10 mA.*

3. Using computer software such as MS Excel or Matlab, plot the voltage transfer curve (V_o vs. V_i) by varying the input voltage from 0 to 5 Volts. You may use the DMMs to measure your data points. You should get a curve that is similar to that shown in Figure 4.

4. Determine the five transition regions of CMOS inverter, similar to those in Figure 4.

5. *Demonstrate your circuit and your transition curve to the TA and have him or her initial your lab checklist.*

6. In region 3, both transistors are saturated, $\frac{dV_o}{dV_i}$ is maximum, and the inverter acts as an amplifier. At the input, use the function generator to apply a 10 mV peak-to-peak sine wave at 1 kHz. Slowly adjust the offset voltage of the function generator until V_o is centered at ½ V_{DD}= 2.5V. At this point, the peak-to-peak output voltage swing is maximum. Determine the gain of the amplifier at this point.

7. *Demonstrate your circuit and gain to the TA and have him or her initial your lab checklist.*

Lab Report:

In your lab report, provide a summary of the results of this lab assignment. You should include, at a minimum, all items indicated on the lab checklist. Append the lab checklist sheet with Laboratory Instructor's initials indicating completed lab demos to your report.

Appendix A: Components Packages and Pins Assignments

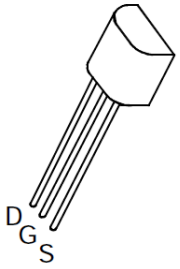

Figure A1. TO-92 Package for ZVN2210A and ZVP2110A and their pin assignments

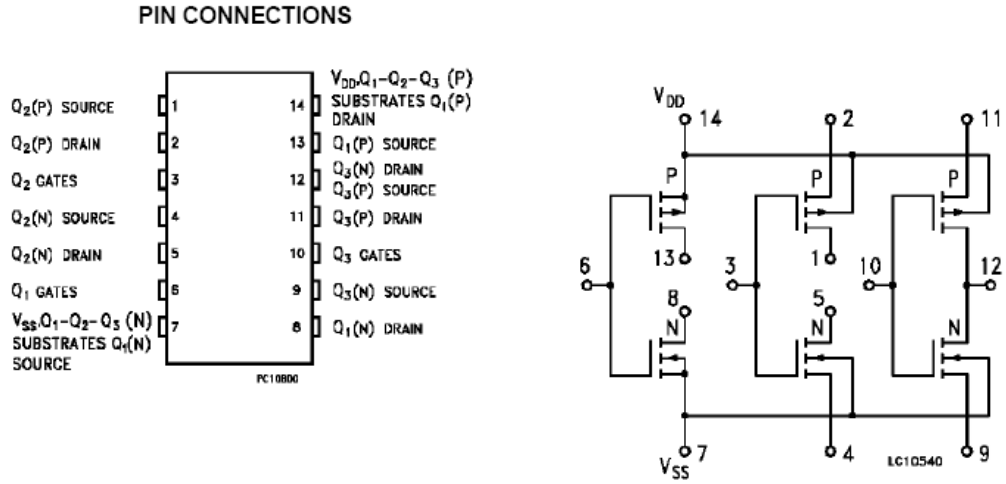

Figure A2 Package and pin assignment for CD4007 complementary dual CMOS transistors

Lab 8 Checklist

Name:_____

Lab title and introduction

- Lab title, your name, date, and lab partner.
- Brief introduction (two or three sentences) explaining the purpose of this lab.

I. Single Stage MOSFET Amplifier (45 pts total)

1. Diagram of amplifier.
2. Measured component values: R_1, R_2, R_S, R_D, R_L, C_G, C_D, C_S
3. Measured DC voltages: V_G, V_S, V_D, I_D
4. Measured mid-band gain.

_____ **5. DEMO**: Have a TA initial this sheet, indicating that he/she has observed your circuit's mid-band gain operation.

6. Measured values of upper and lower corner frequencies.
7. Table of measured values of gain vs. frequency.
8. Plot of measured gain vs. frequency.
9. Maximum peak-to-peak output swing.

_____ **10. DEMO**: Have a TA initial this sheet, indicating that he/she has observed your circuit's frequency response operation.

II. Current Mirror Source (25 pts total)

1. Diagram of current mirror circuit.
2. Table of measured values of I_{Ref} and I_{Bias} compared with expected values

_____ 4. **DEMO**: Have a TA initial this sheet, indicating that he/she has observed your circuit's operation.

III. CMOS Inverter (30 pts total)

1. Diagram of CMOS inverter.
2. Table of measured V_i vs. V_o for the voltage transfer curve.
3. Plot the voltage transfer curve.

_____ 4. **DEMO**: Have a TA initial this sheet, indicating that he/she has observed your circuit's operation and your voltage transfer curve.

5. Measured amplifier gain at the midpoint of V_o.

_____ 6. **DEMO**: Have a teaching assistant initial this sheet, indicating that they have observed your circuit's operation as an amplifier.

