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# Power Electronic Interface for Energy Management in Battery Ultracapacitor Hybrid Energy Storage System

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**Abstract** *The desirable features of batteries used in electric vehicles are high energy density and high power density, but this combination may result in an undesirable large size of battery bank. Ultracapacitors having high power density can be used to complement the high energy density batteries to form an excellent hybrid energy storage system. This article deals with design, simulation, and experimental validation of a power electronic interface between a lead acid battery bank, an ultracapacitor module, and a permanent magnet direct current traction motor. The objective is to achieve desired acceleration and deceleration with minimum stress on the battery bank.*

**Keywords** DC-DC converter, energy management, permanent magnet direct current motor, regenerative braking, ultracapacitors

## 1. Introduction

In the last few years, there has been a strong inclination toward electric vehicles (EVs) because of depleting oil reserves, deteriorating urban air quality, increasing environmental concerns, and geo-political concerns of all nations toward oil dependence. EVs have numerous advantages over internal combustion engine vehicles in terms of operational convenience, cleanliness, and energy efficiency. Also, developments in the field of power electronics and electrical machines have paved the way for efficient, reliable, and cheap motor drives [1]. The main bottlenecks for their successful market penetration are their limited driving range and longer recharging (refuelling) time as compared to conventional gasoline powered vehicles, with the weak link being electrochemical batteries [2, 3]. Battery banks in an EV must have high energy density to attain the vehicle's desired drive range and high power density needed to satisfy acceleration requirements. Unfortunately for a given cell chemistry, there is a trade-off between power output and stored energy: the higher the power available, the lower the stored energy [4]. Thus, to achieve the desired acceleration performance and driving range without degrading the life of batteries, the size and weight of the battery pack need to be increased, which will in turn have negative effects on vehicle performance. This problem can be solved by providing a

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complementary energy source to level the load of the existing high energy density batteries.

Among the available alternatives [5–9], the ultracapacitor can provide a good solution as a complementary energy source because of its high power density, which is useful in assisting the batteries during the periods of peak power demand. Thus, the battery design can be optimized for higher energy density, which will result in a smaller and lighter battery bank. Ultracapacitors can also improve the regenerative braking capability of vehicles, as they can take large currents during deceleration that the batteries cannot because of their lower charging currents. The life of ultracapacitors is longer than batteries, and the operating temperature range is also wider. Thus, integration of ultracapacitors with batteries will result in a hybrid energy storage system (HESS) of high energy density and high power density, providing benefits like a longer driving range, better acceleration performance, controlled regenerative braking, smaller battery pack, and longer battery life.

Over the last decade, there has been substantial research in the area of integrating ultracapacitors with batteries to form a suitable HESS for EVs. One well-emphasized point is the importance of a proper power electronics interface and its control to realize the desired benefits of the complementary characteristics of the two sources. The authors of [10] analyzed the topologies of an ultracapacitor-based regenerative braking system and stated the advantages and flexibility of using a DC-DC converter for interfacing ultracapacitors in an energy storage system. In [11, 12], several bidirectional non-isolated DC-DC converter topologies for interfacing ultracapacitors with batteries were compared. The half-bridge converter topology was utilized in [13–15], but the control strategy used was either rule based or look-up table based and is therefore system specific. In [16], the half-bridge converter topology was used with a classical control technique to control battery and ultracapacitor current. The control dynamics are not satisfactory when there is a shift in load current and very high current flows for a short time that might burn the insulated-gate bipolar transistors (IGBT) switches. In the above-mentioned works, the implementation of a classical control technique is difficult, because three output parameters—battery current, ultracapacitor current, and DC-link voltage—need to be controlled with only one control variable, the duty cycle of pulse-width modulation (PWM) signal given to switches of converter. Thus there is a need to introduce more control flexibility in the overall circuit [17].

Different HESS topologies for battery–ultracapacitor hybridization were reviewed in [18], and a two-input bidirectional DC-DC converter topology was selected as the best option because of higher efficiency, reliability, and control flexibility. This topology was used in [19] along with classical controllers to obtain satisfactory results for a resistive load. All of the above-mentioned topologies have a basic aim to achieve the desired stable voltage at the DC-link of a motor drive inverter; thereby, the inverter of the motor drive must have PWM-based switching to flow the required phase current, which adds to the switching losses of the DC-DC converter. Reliability of the overall system is also reduced because of the presence of large DC-link electrolytic capacitor [20].

The work presented in this article uses the two-input converter topology to control directly the current flowing to (from) a permanent magnet direct current (PMDC) motor. This will eliminate the need of an additional PWM-based drive circuit for the motor, and thus, switching losses are reduced. The battery–ultracapacitor HESS is used to minimize stresses on the battery, present during periods of acceleration and braking of the PMDC traction motor by judicious division of armature current between the two complementary sources. The remainder of the article is organized as follows. Section 2 covers the proposed circuit topology, its control scheme, and the design of required controllers.

Section 3 discusses the simulation and hardware results, and Section 4 contains conclusions.

## 2. Proposed Circuit Topology and Control Scheme

### 2.1. Circuit Topology and Its Operation

The two-input converter topology is used to interface the ultracapacitor with battery to form a suitable HESS. The battery and ultracapacitor banks are connected to the motor terminals using a unidirectional buck converter and a bidirectional buck-boost converter, respectively, as shown in Figure 1. The motor used here is a PMDC motor and is modeled as a series connection of resistance  $R_a$ , inductance  $L_a$ , and speed-dependent voltage source  $e_b$ . The battery bank is represented as an ideal voltage source  $v_{batt}$  with a series resistance  $R_{batt}$  and the ultracapacitor module as an ideal capacitor  $C_{uc}$  with a series resistance  $R_{uc}$ .

For the proper flow of power, both the battery bank and ultracapacitor module are designed in such a way that their voltages  $v_{batt}$  and  $v_{uc}$  are higher than the rated voltage  $v_a$  of the motor. Also in this topology, the battery pack has to supply only the average current required by the motor, and it is not allowed to take in any impulsive regenerative current, as its rated charging current is much lesser than ultracapacitors. The ultracapacitor module assists the battery bank during acceleration of the motor when the current requirement

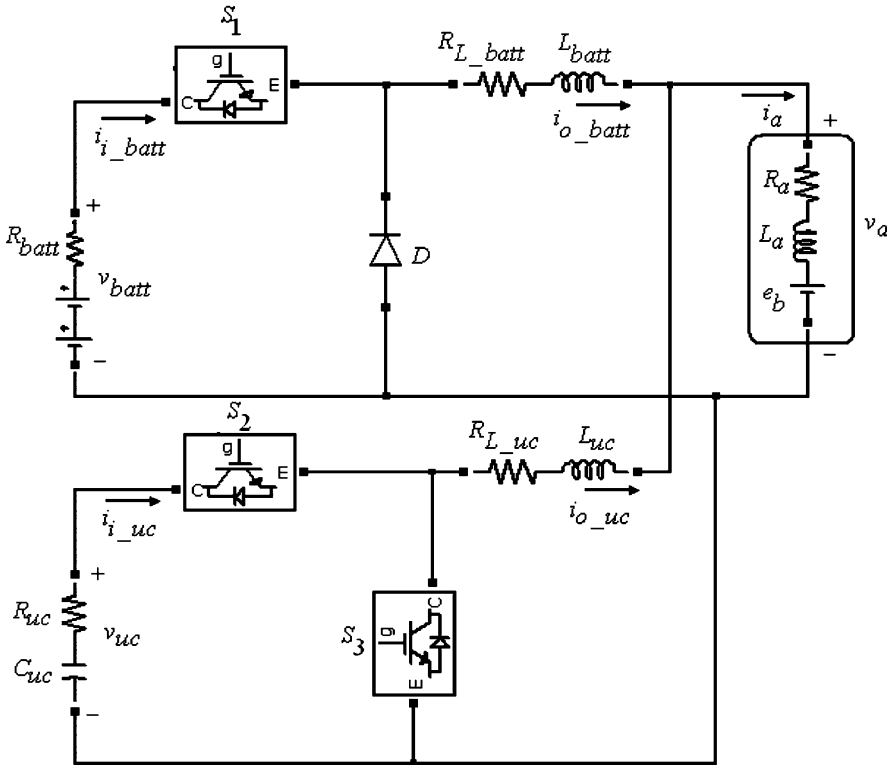


Figure 1. Circuit topology.

is high, as well as taking the impulsive regenerative current during braking of the motor. For these reasons, the unidirectional buck converter topology and bidirectional buck-boost converter topology are selected for the battery bank and ultracapacitor module, respectively. The inductors at the output of the converters try to keep the current constant; thus, the two converters together with inductors act like a current source to the motor. The circuit operation and power flow during different driving conditions is explained as follows.

- **During acceleration:** As the current requirement of a motor is high during this period, both the battery as well as the ultracapacitor converters operate in buck mode to meet the current requirement  $i_a$  of the motor. Switch  $S_1$ , diode  $D$  of the battery converter, switch  $S_2$ , and the anti-parallel diode of switch  $S_3$  of the ultracapacitor converter are active during this period. When switch  $S_1$  is on, the battery bank directly supplies current  $i_{o\_batt}$  to the motor through inductor  $L_{batt}$ , and when the switch is off, the current maintains its direction by flowing through diode  $D$ . Similarly when switch  $S_2$  is on, the ultracapacitor module supplies current  $i_{o\_uc}$  to the motor through inductor  $L_{uc}$ , and when the switch is off, the current maintains its direction by flowing through the anti-parallel diode of switch  $S_3$ .
- **During steady speed:** When the motor is running at a constant speed, the current requirement is less; thus only the battery bank supplies the required current and the ultracapacitor module remains idle. Switch  $S_1$  and diode  $D$  of the battery converter are active while operating in buck mode. Current flow directions for the battery bank remain the same as explained above for the acceleration case.
- **During braking:** During braking, the motor acts as a generator and pumps current back into the circuit. Since the battery bank is not allowed to take this large regenerative current, the battery converter switch  $S_1$  is off during this period. The ultracapacitor converter operates in boost mode and uses the regenerative current to charge the ultracapacitor module. Switch  $S_3$  and the anti-parallel diode of switch  $S_2$  are active during this period. When switch  $S_3$  is on, the current supplied by the motor's back electromotive force (emf) builds up in inductor  $L_{uc}$ , and when the switch is off, the current flows through the anti-parallel diode of switch  $S_2$  into the ultracapacitor module, thus charging it.

## 2.2. Control Scheme and Controller Design

In order to operate the complete system in the desired manner, as explained above, the control scheme shown in Figure 2 is implemented. The variables in the control diagram with an asterisk (\*) represent the reference values of the corresponding variables. The control scheme consists of two feedback loops, an outer speed loop, and an inner current loop. The outer speed loop generates appropriate electric torque reference  $\tau_e^*$  so that the motor speed tracks the given reference speed  $\omega^*$ . The inner current loop is shown within the dotted line, and it ensures that the required amount of current flows into the motor so that the desired torque can be produced. The two loops and design of appropriate controllers are discussed in following subsections.

**2.2.1. Outer Speed Loop.** The outer speed loop is based on a basic mechanical equation, given in Eq. (1). Angular speed  $\omega$  is the state to be controlled, with electric torque  $\tau_e$  as the control input and load torque  $\tau_l$  as a disturbance input. The motor's moment of

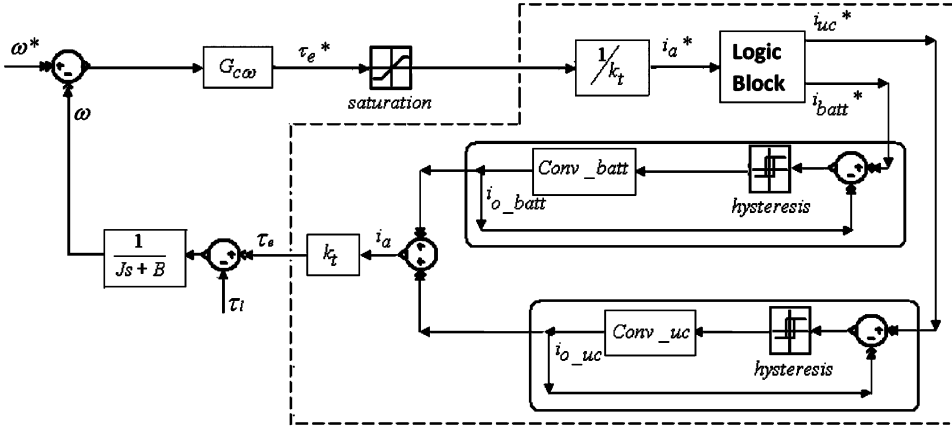


Figure 2. Proposed control scheme.

inertia and coefficient of friction are represented as  $J$  and  $B$ , respectively:

$$\tau_e - \tau_l = J \frac{d\omega}{dt} + B\omega. \quad (1)$$

The outer speed loop shown in Figure 3 is obtained by the transfer function between  $\omega(s)$  and  $\tau_e(s)$ . The transfer function is given as Eq. (2):

$$\left. \frac{\omega(s)}{\tau_e(s)} \right|_{\tau_l(s)=0} = \frac{1}{Js + B}. \quad (2)$$

In the speed loop,  $G_{c\omega}$  is the speed controller, which takes in speed error signal and generates electric torque reference. The design of the speed controller is covered in Section 2.2.3. A saturation block is also used to limit the torque reference within the rated values of the motor [21]. The current required to produce the desired torque is maintained by the inner current loop, and since current dynamics are much faster than speed dynamics, the inner current loop can be represented as unity gain in the speed loop.

**2.2.2. Inner Current Loop.** The current loop is shown within the dotted lines in Figure 2. Initially, with the help of torque constant  $k_t$ , armature current reference  $i_a^*$  is extracted

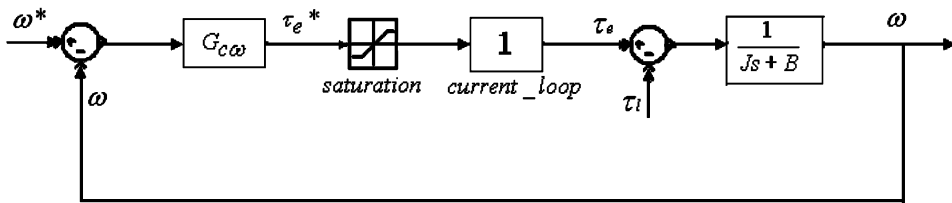


Figure 3. Outer speed loop.

from the torque reference  $\tau_e^*$ . The motor armature current reference is then divided into battery current reference  $i_{batt}^*$  and ultracapacitor current reference  $i_{uc}^*$  by a logic block depending upon different driving conditions. The implemented logic for current division is explained next.

- Current division logic block:** The flowchart of the current division logic is shown in Figure 4. High current demand of the motor during the periods of acceleration are met without extra stress on the battery bank by the intelligent division of current between the battery bank and ultracapacitor module. While the reference to the battery current  $i_{batt}^*$  is maintained at its rated value  $i_{batt\_rated}$ , the remaining current is given as reference to the ultracapacitor circuit  $i_{uc}^*$ . During braking, the ultracapacitor module is made to take in all of the regenerative current by making  $i_{uc}^*$  equal to  $i_a^*$ , thus preventing the battery bank from taking any potentially damaging impulsive regenerative current. When the motor is running at a constant speed, the current requirement is low and the battery bank alone is sufficient; thus  $i_{batt}^*$  is made equal to  $i_a^*$  and the ultracapacitor module is kept idle. The current

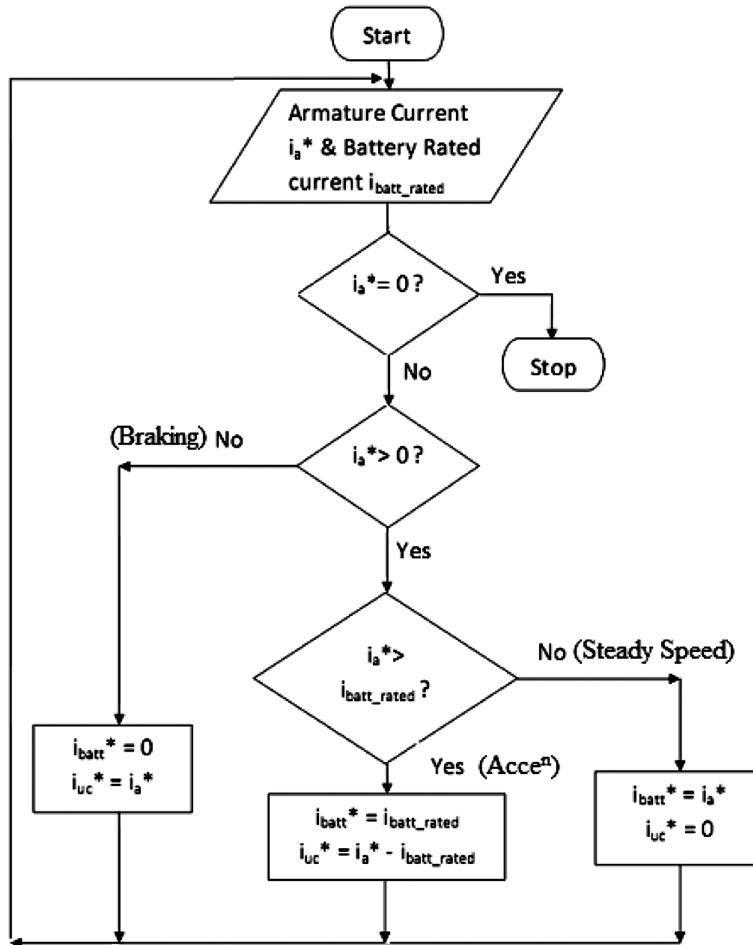


Figure 4. Flowchart of current division logic block.

references are given as input to the current control loops, one each for the battery current and ultracapacitor current. The operation of these loops is explained in what follows.

- **Current control loop:** The reference current values as given by the logic block are compared with corresponding actual output currents  $i_{o\_batt}$  and  $i_{o\_uc}$  of the converters to generate error signals that are fed into current controller blocks. The design of the current controller can be based on any linear or non-linear techniques available [22]. Each method has its own merits and demerits in terms of dynamic response, switching frequency, harmonic content, and tracking errors. The design of a linear fixed frequency proportional-integral (PI) current controller for the proposed system was given in [17]. Presently, for validation of control scheme, the hysteresis controller is selected because of its simplicity, outstanding robustness, lack of tracking errors, independence from load parameter changes, and extremely good dynamics. The hysteresis controller [23] performs two tasks: the first is error compensation, decreasing the error between the reference current and actual current; the second is modulation, determination of switching states of switches. The switching signals are then given to appropriate IGBT switches of the converters (shown as *Conv\_batt* and *Conv\_uc* in Figure 2) to operate them in such a way that the output currents keep tracking their reference values. The sum total of two output currents contributes to the total armature current.

**2.2.3. Design of Speed Controller Using Frequency Response Based Approach.** The outer speed loop is shown in Figure 3. The purpose of designing the speed controller is to properly simulate different driving conditions of the motor and then analyze circuit operations. The design philosophy is based on a simple step-wise introduction of proportional and integral control parameters as per the requirement of the system. The MATLAB environment (The MathWorks, Natick, Massachusetts, USA) is used to simulate bode plots and time responses of the system, and the plots of the system with and without controller are shown in Figure 5.

The open-loop transfer function is given by Eq. (2). The value of  $J$  of the motor used is  $0.00596 \text{ kgm}^2$ , and value of  $B$  is taken as  $0.0001 \text{ Nmsrad}^{-1}$ . Complete specifications of the motor are given in Table 1. Putting these values in Eq. (2) gives Eq. (3):

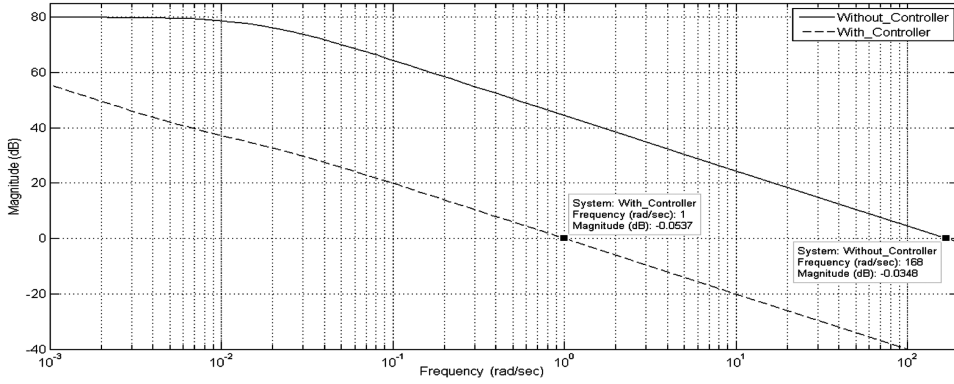
$$ori = \frac{\omega(s)}{\tau_e(s)} = \frac{10,000}{59.6s + 1}. \quad (3)$$

After analyzing the bode plot of Eq. (3) and the unit step time response of the closed-loop transfer function with unity feedback (Figure 5), it is observed that the uncompensated

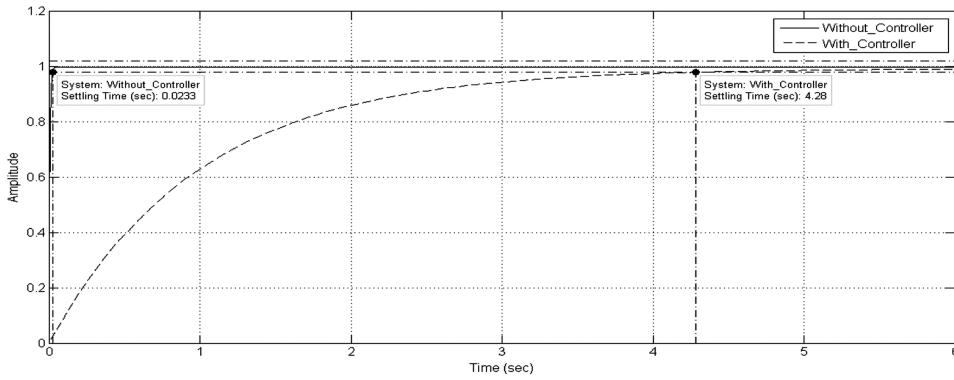
**Table 1**  
Motor specifications

Rated voltage (V)	24	Armature resistance (mΩ)	50
Rated current (A)	62	Armature inductance (mH)	0.106
Rated torque (Nm)	2.4	Armature inertia (kgm <sup>2</sup> )	0.00596
Rated power (kW)	1.5	Speed constant (Vsrads <sup>-1</sup> )	0.038
Rated speed (rads <sup>-1</sup> )	628	Torque constant (NmA <sup>-1</sup> )	0.033





(a)



(b)

**Figure 5.** (a) Magnitude plot and (b) unit step time response of system with and without controller.

system is very fast and that there is a need to increase the settling time of the system. In order to achieve this, the gain crossover frequency  $\omega_{gc}$  is reduced to  $1 \text{ rad/s}^{-1}$  from the original value of  $168 \text{ rad/s}^{-1}$  by multiplying Eq. (3) with a proportional constant  $k_p = 1/168$ . The modified transfer function is given as Eq. (4):

$$ori\_kp = ori * k_p = \frac{59.52}{59.6s + 1}. \quad (4)$$

Upon observing the bode plot of Eq. (4), it is found that  $\omega_{gc}$  has reduced to  $1 \text{ rad/s}^{-1}$ , but there is also a decrement in gain below  $10^{-2} \text{ rad/s}^{-1}$  from 80 dB to 35 dB. When the effect of this drop in low-frequency gain is observed in the unit step time response of a modified closed-loop transfer function, it is found that the settling time has increased to a more realistic value of 3.85 sec from the original value of 0.023 sec, but there is a steady-state error of 1.7%. This steady-state error is removed by introducing an integral controller,  $k_i/s$ . Thus, the modified controller structure is given as Eq. (5), and the open

loop transfer function with the controller is given as Eq. (6):

$$G_{c\omega} = k_p + \frac{k_i}{s} = k_p \left( \frac{1 + Ts}{Ts} \right), \quad \text{where } T = \frac{k_p}{k_i}, \quad (5)$$

$$ori\_G_{c\omega} = ori * G_{c\omega} = \left( \frac{1 + Ts}{Ts} \right) * ori\_kp. \quad (6)$$

The term  $(1 + Ts)/Ts$  increases the gain only below  $1/T$   $\text{rads}^{-1}$ , which, in this case, is taken as  $10^{-2}$   $\text{rads}^{-1}$ , thus giving the value of  $T$  as 100. The value of  $k_i$  is given by  $k_p/T$ , and it comes out to be 0.01/168. The designed controller is represented by Eq. (7), and the final transfer function with a controller is given as Eq. (8):

$$G_{c\omega} = k_p \left( \frac{1 + Ts}{Ts} \right) = \frac{1}{168} \left( \frac{1 + 100s}{100s} \right), \quad (7)$$

$$ori\_G_{c\omega} = \frac{5952s + 59.52}{5960s^2 + 100s}. \quad (8)$$

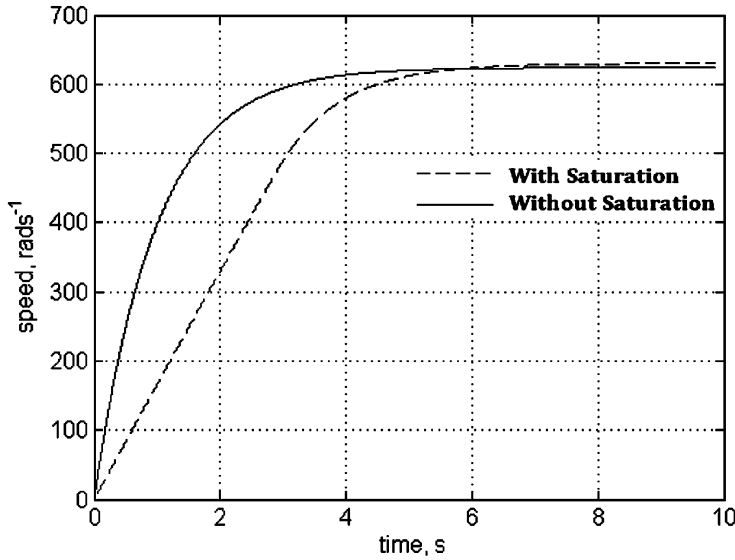
To observe the effectiveness of the controller, the bode plot of Eq. (8) and the unit step response of the final closed-loop transfer function is analyzed (Figure 5). It is found that the steady-state error has reduced to zero and that the system settles to steady-state value in 4.28 sec. The low-frequency gain at  $10^{-3}$   $\text{rads}^{-1}$  has also increased to 55 dB from 35.5 dB. The gain margin and phase margin of the system is infinity and  $90.4^\circ$ , respectively, with a gain cross-over frequency of 1  $\text{rads}^{-1}$ . Thus, the speed controller has been properly designed.

- **Effect of introduction of saturation block:** The introduction of a saturation block to limit the control input  $\tau_e$  within rated values will only have an effect of increased settling time to reach the reference speed. To study this effect a MATLAB/SIMULINK model is used. A step input of the rated speed of the motor, *i.e.*, 628  $\text{rads}^{-1}$ , is given to the system with and without a saturation block. The saturation block limits the control input to a maximum value of 1 Nm. The time responses of the system with and without a saturation block are shown in Figure 6, which clearly shows an increase in the setting time for the system with a saturation block by approximately 2 sec. This sluggishness is tolerable to the system, and the saturation block does not cause any other changes; thus the designed controller can be used with the system having a saturation block.

### 3. Results and Discussion

#### 3.1. Simulation Results

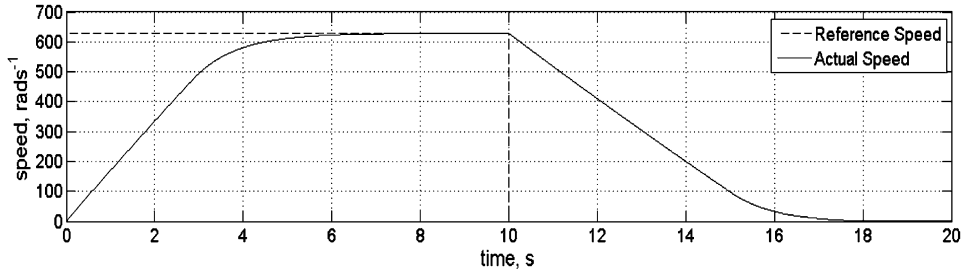
The circuit together with the control algorithm is simulated in MATLAB/SIMULINK. The SimPowerSystems toolbox is used to simulate different electrical components, such as resistance, inductance, capacitance, voltage source, IGBT switches, and diodes. The PMDC motor is simulated as a series connection of armature resistance, armature inductance, and speed-dependent voltage source (for representing back emf). Specifications of the motor used in the experiment, for proper simulation, are given in Table 1. The data sheet of the model RT12200 valve regulated lead acid batteries manufactured by RITAR (Shenzhen, China) [24] is utilized to simulate the battery bank as a lead acid battery



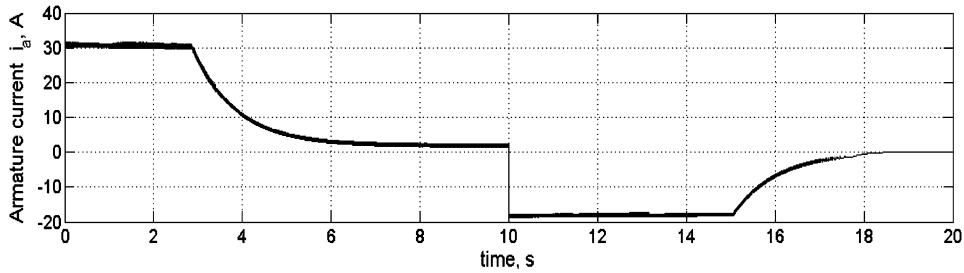
**Figure 6.** Time response of system with and without saturation.

block. Each battery is 12 V/20 Ah@20-hour rate, and the battery bank consists of three such batteries in series; consequently, the battery bank is 36 V/20 Ah@20-hour rate with a total internal series resistance  $R_{batt}$  of 42 m $\Omega$ . The design steps for proper cell sizing of an ultracapacitor are given in [25]. For simulation and hardware experiment, a readily available ultracapacitor module from NESSCAP (Gyeonggi-do, South Korea) of an appropriate size (36 F) and voltage rating (48 V) is selected. Its data sheet [26] is used to simulate the ultracapacitor module as an ideal capacitor with a series resistance. The ultracapacitor series resistance  $R_{uc}$  is 12 m $\Omega$ , and the ultracapacitor module is assumed to be initially charged with a terminal voltage of 40 V. The inductor selection at fixed switching frequency is based on the maximum allowable output current ripple. Since the hysteresis current control technique is being used, the switching frequency is variable; thus, a slightly higher value of 5 mH is selected for filter inductors  $L_{batt}$  and  $L_{uc}$  so that the current ripple limit and continuous current conduction operation requirements are fulfilled. The series resistance of inductors  $R_{L\_batt}$  and  $R_{L\_uc}$  is taken as 20 m $\Omega$ . The parameters of speed controller  $G_{c\omega}$  are the designed values with  $k_p = 1/168$  and  $k_i = 0.01/168$ . The saturation block is used to limit the forward motoring torque to 1 Nm and, thus, the armature current to approximately 30 A. It also limits the forward braking torque to -0.6 Nm and, thus, the regenerative current to approximately 18 A. The saturation limits can be varied within the rated value, thereby resulting in different rates of acceleration and deceleration.

The speed response and armature current of the motor under a no-load condition are shown in Figure 7. Initially, the reference speed is set to be the rated speed of the motor, and at  $t = 10$  sec, the reference speed is made zero, which demonstrates forward motoring and forward braking of the motor. The armature current of the motor shows that during the initial acceleration period, high torque, thus high current, is demanded; during braking, the motor torque is negative, so it acts as a generator and supplies current back to the circuit.



(a)



(b)

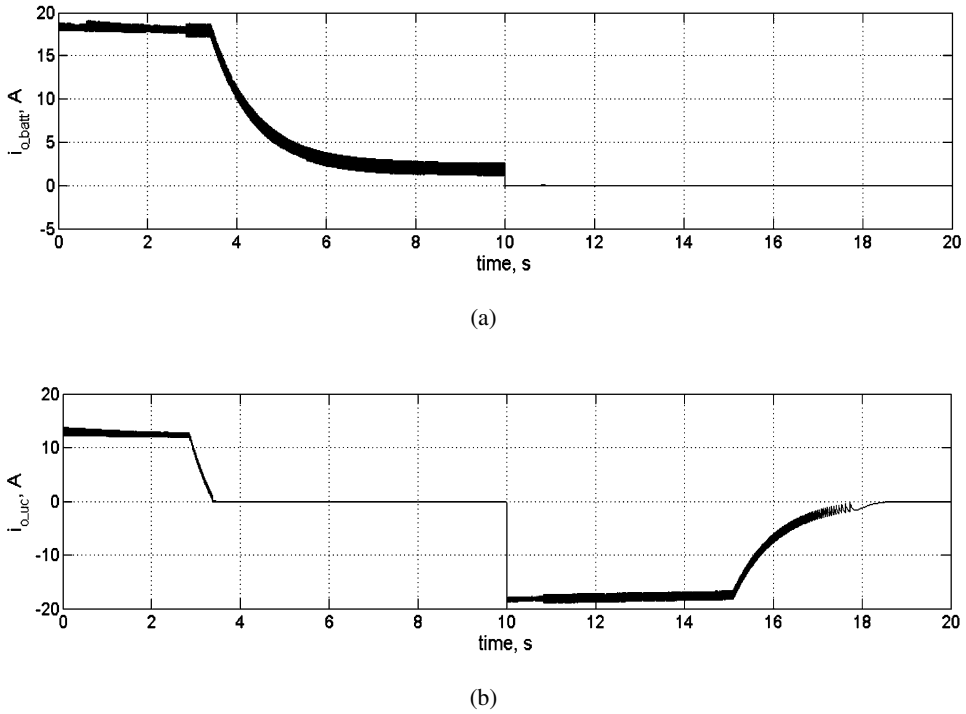
**Figure 7.** (a) Speed response and (b) armature current of motor.

The output current profiles of battery and ultracapacitor converters are shown in Figure 8. Maximum rated discharge current of the battery bank is fixed at 18 A, so the extra current demanded by the motor during acceleration needs to be supplied by the ultracapacitor module. As the motor reaches a steady speed, the current requirement decreases, and when it falls below the maximum rated discharge current of the battery bank, the ultracapacitor module stops supplying current and only the battery bank handles the current requirement. Also during braking, since the battery bank is not supposed to intake impulsive regenerative current, the ultracapacitor module thus takes all of the current to charge itself.

Also, if the amount of regenerative current taken by the ultracapacitor pack is increased to a higher value, it results in fast deceleration, thus achieving controlled regenerative braking. Figure 9 shows the speed response and ultracapacitor converter output current with the charging current limit raised to 30 A. Different rates of deceleration can be observed easily by comparing the speed responses after 10 sec between Figures 7 and 9.

### 3.2. Hardware Results

A personal computer based hardware setup is prepared to test the effectiveness of both circuit topology and control scheme in creating a smart battery ultracapacitor HESS. The PMDC motor, battery bank, ultracapacitor module, and filter inductors used in the experiment are the same as those used for numerical simulation (see Section 3.1). The DC-DC converter circuit is fabricated using a Semikron IGBT module (SKM75GB063D; Semikron Elektronik GmbH & Co., KG, Nuremberg, Germany) and Semikron power

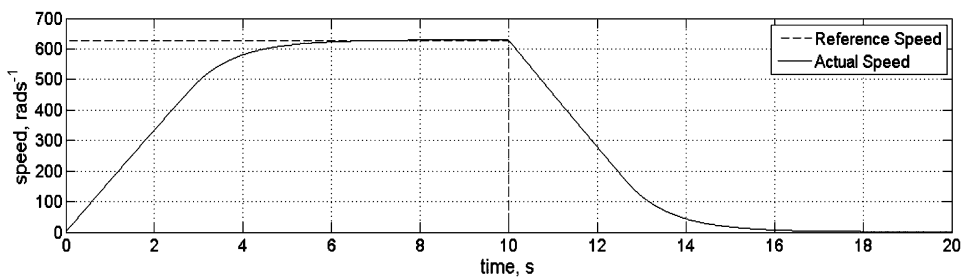


**Figure 8.** (a) Battery converter output current and (b) ultracapacitor converter output current.

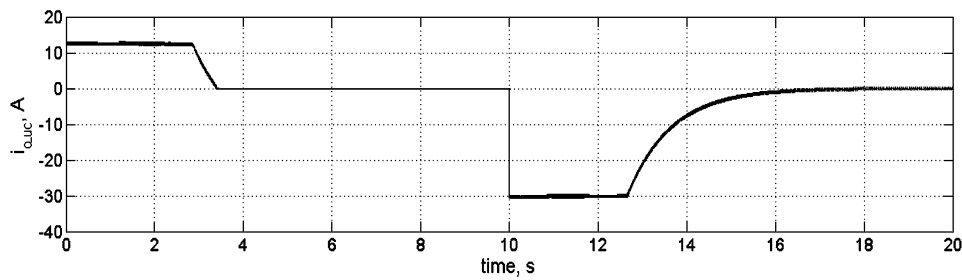
diode (MD7EF4008). To drive the IGBT switches, FUJI's hybrid IGBT driver (IC VLA517-01R; Fuji Electric Co. Ltd., Tokyo, Japan) is used to provide driving signals across the gate emitter terminals. The operation of control logic needs sensing of motor speed and output currents of converters. For sensing speed, an incremental optical encoder is used [27, 28].

To sense output currents, two LEM-manufactured current transducers (LA 55-P; LEM Holding SA, Plan-les-Ouates, Switzerland) are used. The complete control scheme is implemented on MATLAB/SIMULINK platform. The Real-time Windows Target toolbox of MATLAB is used to receive and send signals between the experimental setup and the computer through a National Instruments (PCI-6229; National Instruments Corporation, Austin, Texas, USA) data acquisition card. Because of the computational limitations of the Real-time Windows Target toolbox, the switching frequency up to only 1 kHz is used, which leads to increased ripples in current waveforms. The prepared hardware setup is shown in Figure 10.

In the experiment, the motor is accelerated to  $50 \text{ rad s}^{-1}$  from rest, and after 5 sec, it is again brought back to rest. Figures 11(a), 11(b), and 11(c) show the armature current, battery converter output current, and ultracapacitor converter output current, respectively, with the corresponding motor speed. The battery rated current is limited to 10 A; thus, during acceleration, the extra current demand is fulfilled by the ultracapacitor module. During a steady-speed running condition, only the battery bank is providing current and the ultracapacitor current is zero. During braking, the motor current is negative, which shows that the motor is acting like a generator. The negative regenerative current is taken by the ultracapacitor to charge itself. The magnitude of negative current is small, because

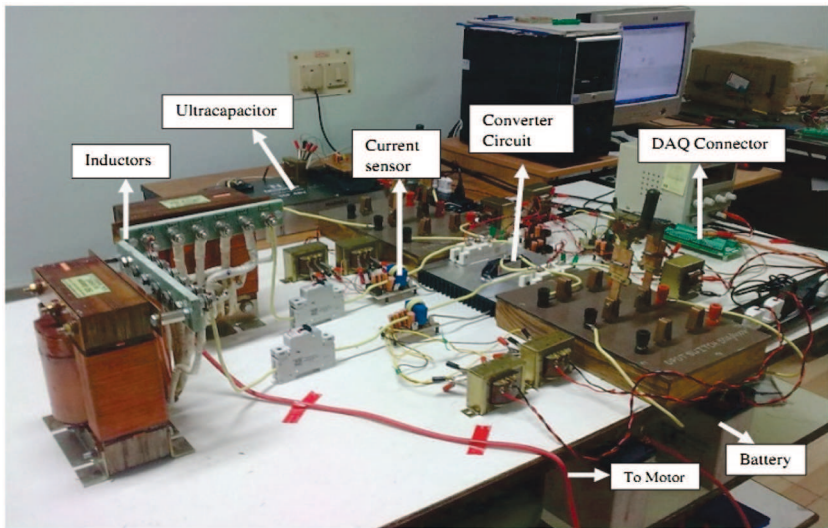


(a)

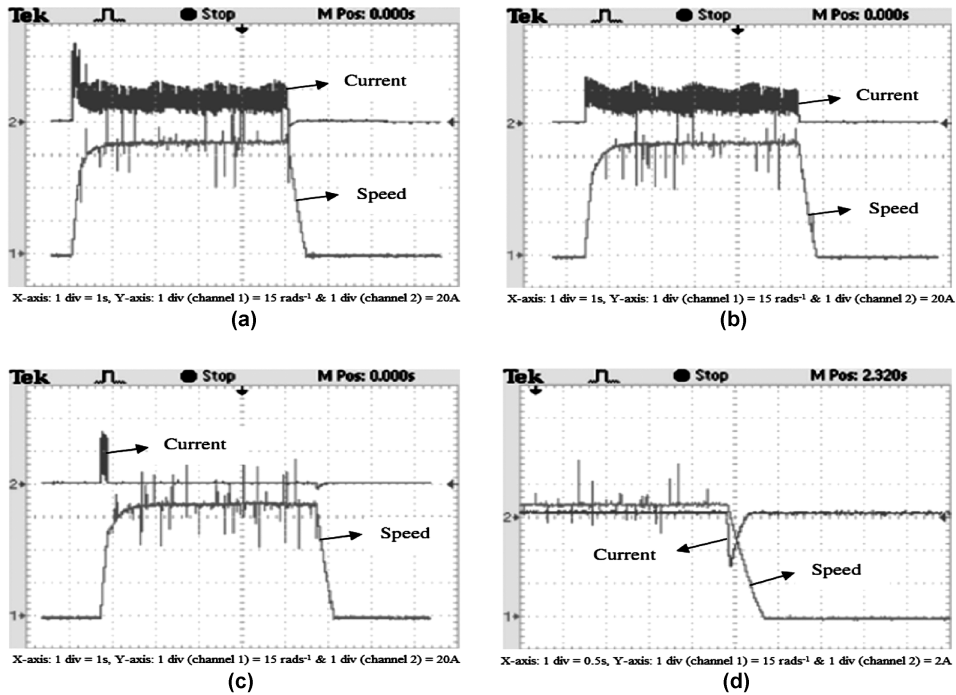


(b)

**Figure 9.** (a) Speed response and (b) ultracapacitor current at higher regenerative current.



**Figure 10.** Hardware setup. (color figure available online)



**Figure 11.** (a) Motor speed and armature current, (b) motor speed and battery converter output current, (c) motor speed and ultracapacitor converter output current, and (d) magnified view of regenerative current.

the friction of the motor is higher than the expected value and it is rotating at a lower speed. The magnified view of the regenerative current going into the ultracapacitor is shown in Figure 11(d).

#### 4. Conclusion

The issue of properly integrating an ultracapacitor with a battery for potential application in EVs is taken in the presented work. A power electronics interface and its control scheme are proposed, and their effectiveness for driving a PMDC traction motor is illustrated in both simulation and experimental results. The hardware experiment results are found to be in close agreement with the simulation results. The motor is accelerating and decelerating as per the instructions given, and there are no large spikes in current waveforms. This topology uses the least number of IGBT switches and also eliminates additional PWM-based drive circuits for the motor, thus minimizing switching losses. The reliability of the system is also improved because of the absence of a large electrolytic capacitor at the DC link. The control strategy implemented to coordinate the power flow to (from) the motor ensures smooth distribution of the armature current between the two complementary sources. Controlled regenerative braking can also be achieved by controlling the regenerative charging current of the ultracapacitor. From the results, it can be concluded that the circuit topology and its control scheme work fine, and they can be refined further for possible applications in an HESS for EVs.

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