ELT-3050 Final Project

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**Preliminary Design Proposal**

**Overview:**

The purpose of this this project is to produce an arbitrary waveform generator (AWG). AWG’s can synthesize a general selection of waveforms usually ranging from sine, square, or triangle patterns.

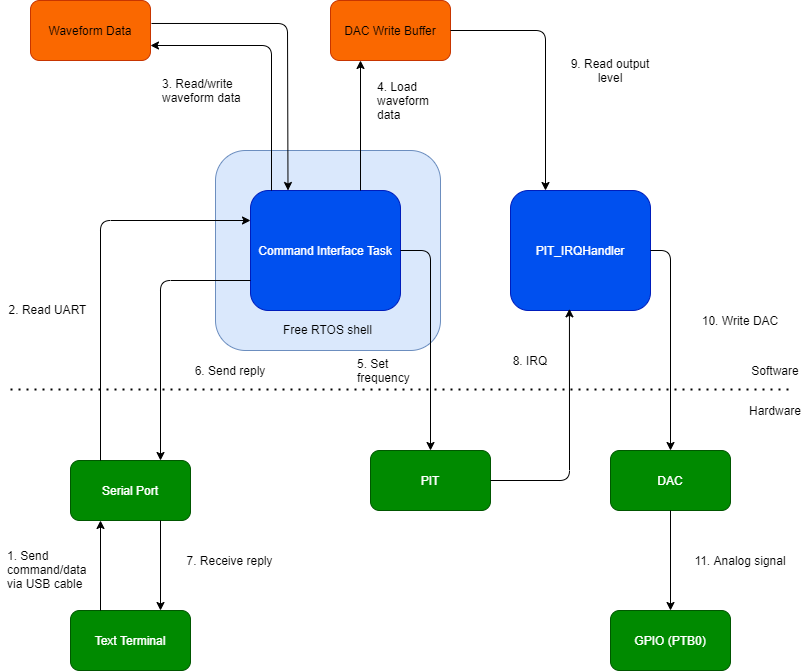
They can also produce waveforms which are custom tailored to meet certain criteria an end user may require.

**Scope of project:**

An AWG will be created using the FRDM-KL25Z development board, along with the accompanying VTC shield board. The AWG will have the ability to generate three pre-defined waveforms, as well as two user specified arbitrary waveforms. The AWG will have four selectable output frequencies, each having a maximum voltage output of 3.3 volts. AWG functionality will be controlled via serial communication using predetermined commands.

**Project Design:**

The initial design for the AWG consists of both hardware peripherals, and source code incorporated into a Free RTOS environment.



**Figure I: Block Diagram of AWG**

The AWG shall be controlled by a serial terminal such as TeraTerm which can send commands and arbitrary waveform data to the microcontroller. The commands/data travel via a USB cable to the Open SDA port on the KL25Z.

The Command Interface Task is a task created in the main function using FreeRTOS, so that other possible tasks can run concurrently. It processes commands, reads/writes waveform data, and sets the PIT value. The Command Interface Task also has the important function of loading the DAC write buffer with the correct waveform data to be sent to the DAC.

The PIT\_IRQHandler is the KL25Z’s standard ISR for the PIT. In this case, it is used to set the DAC output at a particular frequency. Once triggered by the PIT, this interrupt reads one integer in the DAC write buffer at the current index. The interrupt will then write the level to the DAC, and update the index. The index starts at 0 and wraps back to 0 once the end of the write buffer is reached.

When the DAC value has been set, it will output an analog value to PTB0 on the shield board.

**Project Timeline:**

This proposal will be presented for review on 05/01/2021. Upon approval, a functional prototype will be developed for a final review with an anticipated date of 05/12/2021. Any necessary revisions will be made at that time. The finished AWG, including documentation will be submitted 05/21/2021.