Uart Implementation Reference

v1.0.0

Written by
Kevin LASTRA

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1 Introduction

1.1 Purpose of the manual

The purpose of this manual is twofold. First, it serves as a comprehensive resource to document the Implementation of a Universal Asynchronous Receiver-Transmitter (UART). This process has been undertaken not only as a journey of self-learning but also as a way to share knowledge and contribute to the broader community of developers, engineers, and enthusiasts.

1.2 Audience

This manual is primarly intended for design engineers who are involved in the development and implementation of communication systems, particularly those working with embedded systems, microcontrollers, and hardware interfaces.

2 UART overview

The Universal Asynchronous Receiver-Transmitter (UART) is a fundamental hardware communication protocol used for asynchronous serial communication.
This protocol is widely used in embedded systems, microcontrollers, and communication devices due to its simplicity and effectiveness in handling relatively low-speed data transfer.

2.1 UART fundamentals

2.1.1 Reception and transmission

UART allows two devices to exchange data using only two wires, RX for receive data and TX for transmit data.

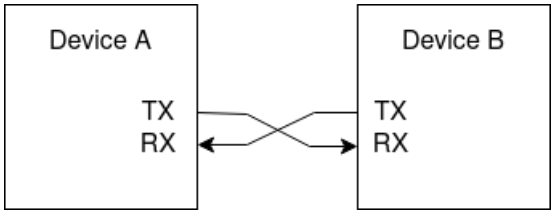

Figure 1: Two UART's interfaces connected

2.1.2 Asynchronous communication

An asynchronous communication refers to a type of data transmission where the sender and receiver do not rely on a shared clock signal for synchronization. Instead, each device operates using its own internal clock and relies on specific timing conventions to ensure data is transmitted and received correctly.

In asynchronous UART communication, the data is sent in discrete chunks (called data frames) over the communication channel, with the timing governed by agreed-upon parameters like baud rate and frame size.

2.1.3 Baud rate

The baud rate defines the speed at which data is transmitted over the communication channel. It is usually expressed in bits per second (bps).
In the context of UART the baud rate specifies how many bits of data can be transmitted each second. Both transmitter and receiver must be set to the same baud rate.

The general formula for calculating the baud rate is:

$$BaudRate = \frac{ClockFrequency}{Divisor}$$

2.1.4 Data frame structure

A UART data frame typically consists of:

Range name	**Description**	**Implementation bit length**
Start bit	Signals the beginning of data transmission	1
Data bits	The actual data being sent	5 - 9
Parity	Used for error checking	0 - 1
Stop bit	Signals the end of the data transmission	1 - 2

2.2 Advantages and limitations

Advantages:

1. Minimal pins required, essay to implement on a system.
2. Low cost, because of its minimal hardware requirements the UART is a cost-effective solution.
3. Widely supported.
4. Simplicity in software implementation.

limitations:

1. Distance limitations, the maximum range depends on the baud rate, the quality of the wires and the environment (e.g. electromagnetic interferences).
2. Relatively slow data transfer.
3. Limited to two devices.
4. Susceptibility to baud rate mismatch.
5. Limited error detection, UART error detection is limited to parity checks and stop bits.

3 Implementation

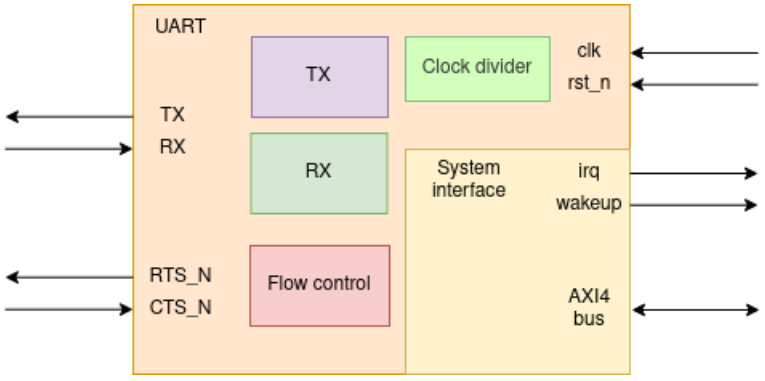

Figure 2: Implementation diagram

3.1 Design

3.2 Interface

3.2.1 UART

The UART interface includes the basic two wires for data transmission and reception **rx** and **tx**.

In addition to the basic lines, the UART interface includes two control flow lines:

1. RTS_N **(Ready to Send)**: Signals that the device is ready to send data.

2. CTS_N **(Clear to Send)**: Indicate that the receiving device is ready to accept data.

Why use cts_n and rts_n?

The flow control solve two principal issues:

1. Overflow, a fast transmitter could overwhelm a slower receiver, leading to data loss or corruption

2. Collision, when two devices attempt to transmit data simultaneously, it can result in garbled communication or corrupted data.

Without proper flow control, these issues can severely impact communication reliability. The control flow wires solve this by coordinating the readiness of both devices:

1. The transmitter checks **cts_n** to ensure the receiver is ready before sending data.

2. The receiver asserts **rts_n** when it is ready to receive more data, allowing the transmitter to proceed.

This approach is especially useful in systems with devices of varying processing speeds or in applications where reliability is critical, such as industrial communication systems or high-throughput embedded designs.

3.2.2 System

On the system side, the UART interface is connected to the system using the following components:

AXI4 bus

The UART control and configuration are managed through an AXI4 bus

interface, a widely used protocol in system-on-chip (SoC) designs. The AXI4 bus allows the system to:

1. Configure UART parameters.
2. Monitor UART status registers for errors, activity, or flow control states.
3. Enable or disable interrupts for data transmission and reception.

IRQ lines for RX and TX

To optimize system efficiency, the UART module includes two dedicated interrupt wires.

Wakeup line

The wake-up line is used to bring the system out of a low-power or sleep mode when activity is detected on the UART interface.

3.3 Registers

3.4 Interrupt request (IRQ)

3.5 Low power

4 Versioning

This manual follows a structured versioning system to ensure clarity and traceability of updates. The version number is formatted as vX.Y.Z, where:

1. **X** - major revisions, such as significant updates to content or structure.
2. **Y** - minor revisions, such as additions or updates to specific sections.
3. **Z** - minor edits, such as corrections to typos, formatting, or small clarifications.

4.1 History

Version	Date	Author	Description
v1.0.0	0	Kevin Lastra	Initial release of the UART Implemenation Reference

5 Glosary

6 References