



## 8K X 8 BIT LOW POWER CMOS SRAM

### FEATURES

- Access time :55ns
- Low power consumption:  
Operation current :  
15mA (TYP.),  $V_{CC} = 3.0V$   
Standby current :  
1 $\mu A$  (TYP.),  $V_{CC} = 3.0V$
- Wide range power supply : 2.7 ~ 5.5V
- Fully Compatible with all Competitors 5V product
- Fully Compatible with all Competitors 3.3V product
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **All products ROHS Compliant**
- Package : 28-pin 600 mil PDIP  
28-pin 330 mil SOP  
28-pin 8mm x 13.4mm sTSOP

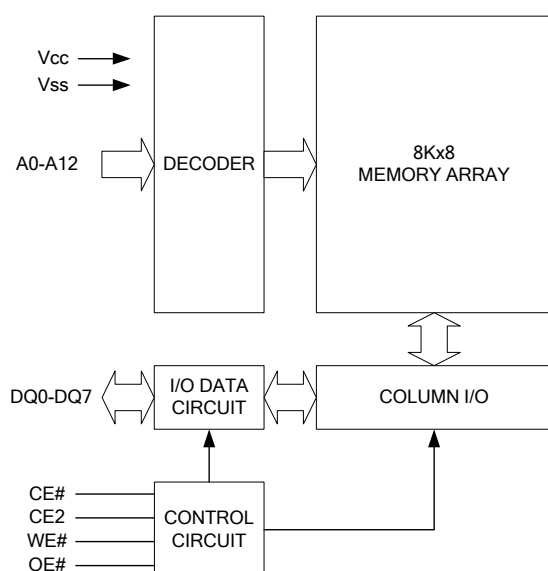
### GENERAL DESCRIPTION

The AS6C6264 is a 65,536-bit low power CMOS static random access memory organized as 8,192 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C6264 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C6264 operates with wide range power supply.

### FUNCTIONAL BLOCK DIAGRAM



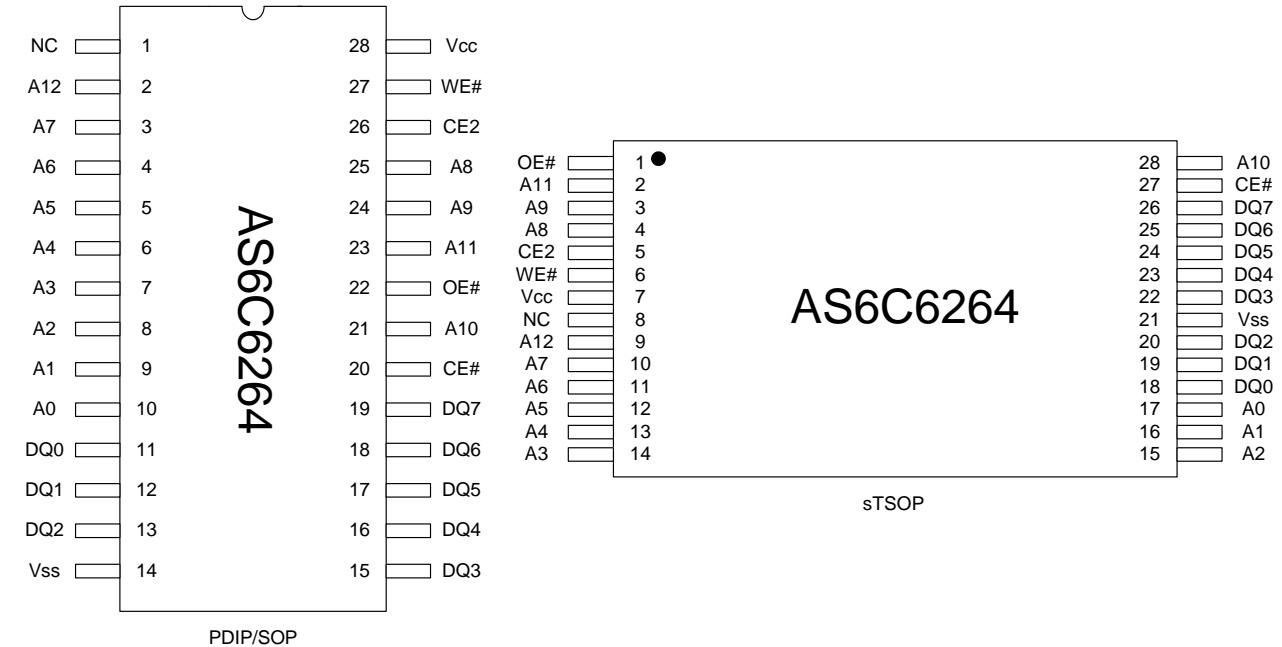
### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection



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### PIN CONFIGURATION



### ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	V <sub>TERM</sub>	-0.5 to 7.0	V
Operating Temperature	T <sub>A</sub>	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA
Soldering Temperature (under 10 sec)	T <sub>SOLDER</sub>	260	°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

### TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
	X	L	X	X	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	H	High-Z	I <sub>CC</sub> , I <sub>CC1</sub>
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>CC</sub> , I <sub>CC1</sub>
Write	L	H	X	L	D <sub>IN</sub>	I <sub>CC</sub> , I <sub>CC1</sub>

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.



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### DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>5</sup>	MAX.	UNIT
Supply Voltage	V <sub>CC</sub>		2.7	3.0	5.5	V
Input High Voltage	V <sub>IH</sub> <sup>1</sup>		0.7*V <sub>CC</sub>	-	V <sub>CC</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub> <sup>2</sup>		- 0.5	-	0.6	V
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	- 1	-	1	μA
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	- 1	-	1	μA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA	2.4	3.0	-	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA	-	-	0.4	V
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min. CE# = V <sub>IL</sub> and CE2 = V <sub>IH</sub> , I <sub>I/O</sub> = 0mA	- 55	15	45	mA
	I <sub>CC1</sub>	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V <sub>CC</sub> -0.2V, I <sub>I/O</sub> = 0mA other pins at 0.2V or V <sub>CC</sub> -0.2V	-	3	10	mA
Standby Power Supply Current	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> -0.2V or CE2 ≤ 0.2V	-C	1	50 <sup>4</sup>	μA
			-I	1	80 <sup>4</sup>	μA

Notes: C = Commercial Temperature I = Industrial temperature

1. V<sub>IH</sub>(max) = V<sub>CC</sub> + 30V for pulse width less than 10ns

2. V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.

3. Over/Undershoot specifications are characterized, not 10% tested.

4. 10μA for special request

5. Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C

### CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

### AC TEST CONDITIONS

Input Pulse Levels	0.2V to V <sub>CC</sub> - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 50pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -1mA/2mA



## 8K X 8 BIT LOW POWER CMOS SRAM

### AC ELECTRICAL CHARACTERISTICS

#### (1) READ CYCLE

PARAMETER	SYM.			AS6C6264-55				UNIT
				MIN.	MAX.			
Read Cycle Time	t <sub>RC</sub>			55	-			ns
Address Access Time	t <sub>AA</sub>			-	55			ns
Chip Enable Access Time	t <sub>ACE</sub>			-	55			ns
Output Enable Access Time	t <sub>OE</sub>				30			ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *			10	-			ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *			5	-			ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *			-	20			ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *				20			ns
Output Hold from Address Change	t <sub>OH</sub>			10	-			ns

#### (2) WRITE CYCLE

PARAMETER	SYM.			AS6C6264-55				UNIT
				MIN.	MAX.			
Write Cycle Time	t <sub>WC</sub>			55	-			ns
Address Valid to End of Write	t <sub>AW</sub>			50	-			ns
Chip Enable to End of Write	t <sub>CW</sub>			50	-			ns
Address Set-up Time	t <sub>AS</sub>			0	-			ns
Write Pulse Width	t <sub>WP</sub>			45	-			ns
Write Recovery Time	t <sub>WR</sub>			0	-			ns
Data to Write Time Overlap	t <sub>DW</sub>			25	-			ns
Data Hold from End of Write Time	t <sub>DH</sub>			0	-			ns
Output Active from End of Write	t <sub>OW</sub> *			5	-			ns
Write to Output in High-Z	t <sub>WHZ</sub> *			-	20			ns

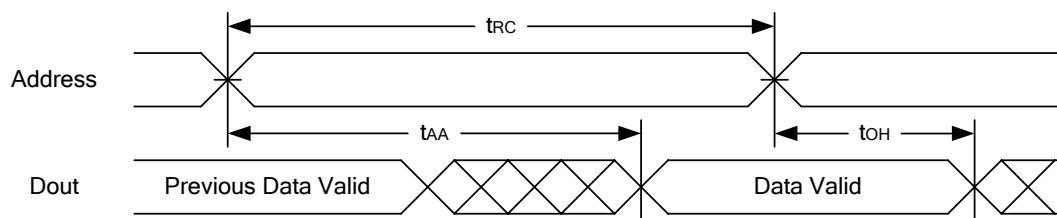
\*These parameters are guaranteed by device characterization, but not production tested.



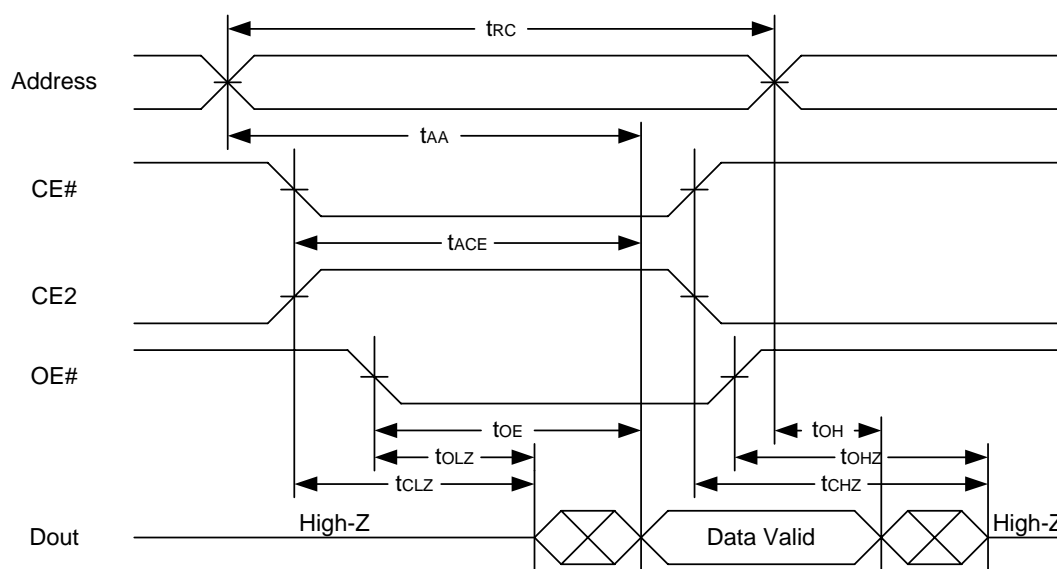
## 8K X 8 BIT LOW POWER CMOS SRAM

### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2)



#### READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



#### Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

[illegible]

The timing diagram illustrates the relationship between the Address, CE#, CE2, WE#, Dout, and Din signals. Key timing parameters are labeled:

- twc**: Address setup time before WE# assertion.
- taw**: Address hold time after WE# deassertion.
- tAS**: CE# setup time before WE# assertion.
- tWR**: CE# hold time after WE# deassertion.
- tcw**: CE2 setup time before WE# assertion.
- tWP**: WE# pulse width.
- twHZ**: WE# hold time after WE# deassertion.
- High-Z**: State of the WE# signal after deassertion.
- tdw**: Data Valid setup time before WE# assertion.
- tdH**: Data Valid hold time after WE# deassertion.

The diagram also shows the data bus (Dout) being driven during the WE# pulse and then returning to High-Z. The data input (Din) is shown as a constant signal during the data valid period.

6.  $t_{\text{LOW}}$  and  $t_{\text{WHZ}}$  are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.



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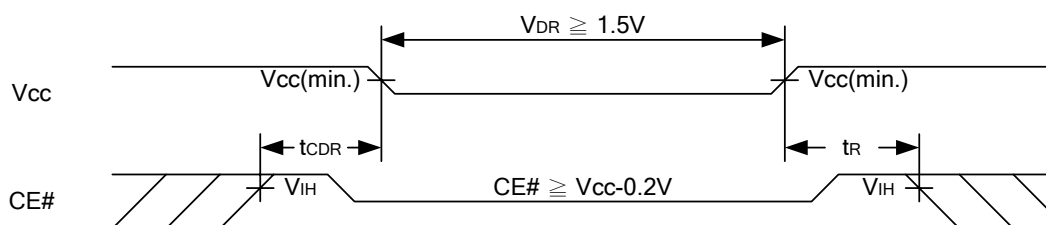
### DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# $\geq$ V <sub>CC</sub> - 0.2V or CE2 $\leq$ 0.2V	1.5	-	5.5	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V CE# $\geq$ V <sub>CC</sub> - 0.2V or CE2 $\leq$ 0.2V	-	0.5	10	$\mu$ A
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *	-	-	ns

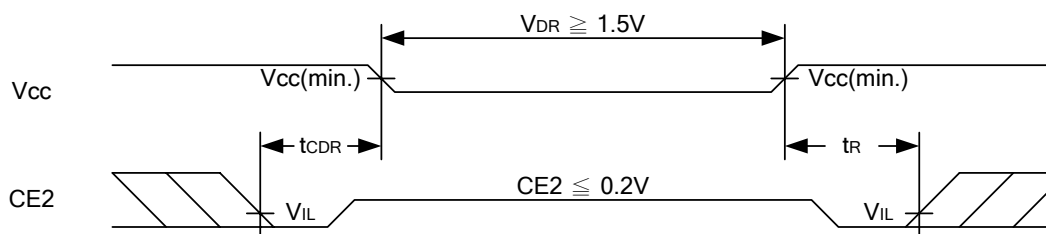
t<sub>RC</sub>\* = Read Cycle Time

### DATA RETENTION WAVEFORM

#### Low V<sub>CC</sub> Data Retention Waveform (1) (CE# controlled)



#### Low V<sub>CC</sub> Data Retention Waveform (2) (CE2 controlled)

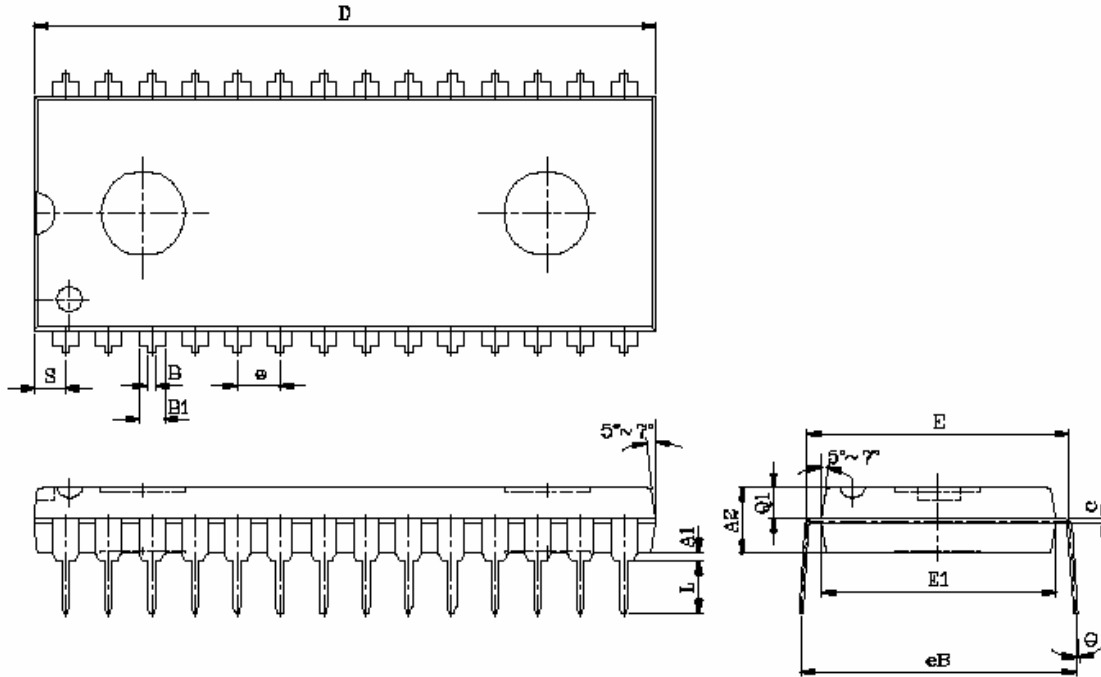




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### PACKAGE OUTLINE DIMENSION

28 pin 600 mil PDIP Package Outline Dimension



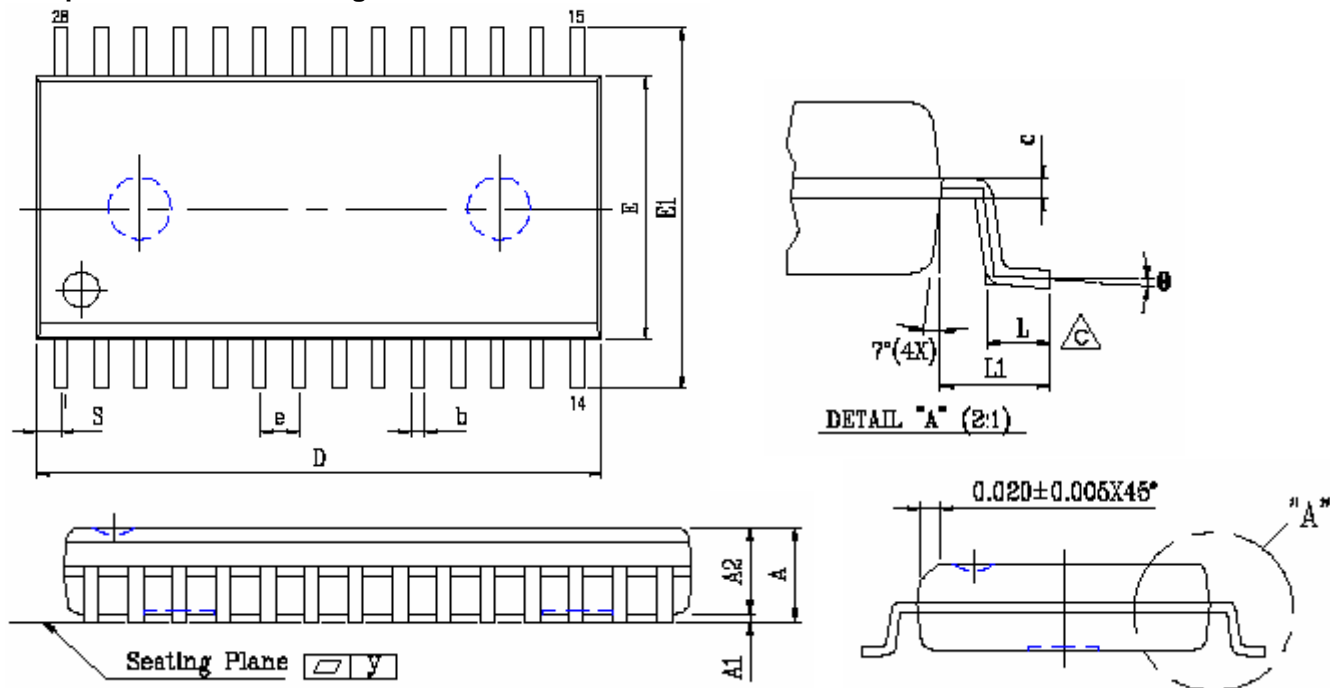
SYM.	UNIT	INCH.(BASE)	MM(REF)
A1		0.010 (MIN)	0.254 (MIN)
A2		0.150±0.005	3.810±0.127
B		0.020 (MAX)	0.508(MAX)
B1		0.055 (MAX)	1.397(MAX)
c		0.012 (MAX)	0.304 (MAX)
D		1.430 (MAX)	36.322 (MAX)
E		0.6 (TYP)	15.24 (TYP)
E1		0.52 (MAX)	13.208 (MAX)
e		0.100 (TYP)	2.540(TYP)
eB		0.625 (MAX)	15.87 (MAX)
L		0.180(MAX)	4.572(MAX)
S		0.06 (MAX)	1.524 (MAX)
Q1		0.08(MAX)	2.032(MAX)
Θ		15°(MAX)	15°(MAX)





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### 28 pin 330 mil SOP Package Outline Dimension

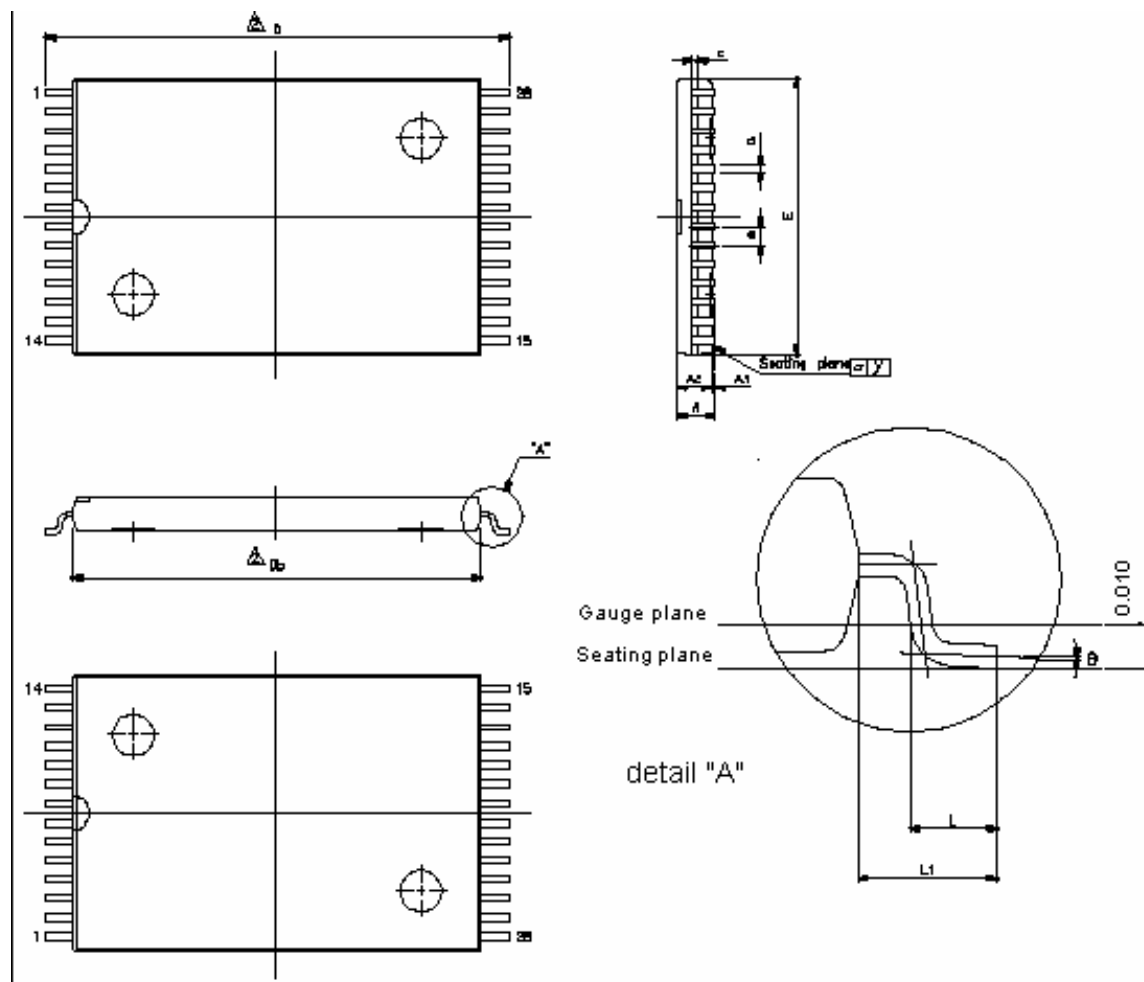


SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.120 (MAX)	3.048 (MAX)
A1		0.002(MIN)	0.05(MIN)
A2		0.098±0.005	2.489±0.127
b		0.016 (TYP)	0.406(TYP)
c		0.010 (TYP)	0.254(TYP)
D		0.728 (MAX)	18.491 (MAX)
E		0.340 (MAX)	8.636 (MAX)
E1		0.465±0.012	11.811±0.305
e		0.050 (TYP)	1.270(TYP)
L		0.05 (MAX)	1.270 (MAX)
L1		0.067±0.008	1.702 ±0.203
S		0.047 (MAX)	1.194 (MAX)
y		0.003(MAX)	0.076(MAX)
Θ		0°~10°	0°~10°



# 8K X 8 BIT LOW POWER CMOS SRAM

## 28 pin 8mm x 13.4mm sTSP Package Outline Dimension



UNIT SYM.	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.006 (TYP)	0.15(TYP)
c	0.010 (TYP)	0.254(TYP)
Db	0.465±0.004	11.80±0.10
E	0.315±0.004	8.00±0.10
e	0.022 (TYP)	0.55(TYP)
D	0.528±0.008	13.40±0.20
L	0.020±0.004	0.50±0.10
L1	0.0315±0.004	0.80±0.10
y	0.08(MAX)	0.003(MAX)
Θ	0°~5°	0°~5°

Note : E dimension is not including end flash. The total of both sides' end flash is not above 0.3mm.



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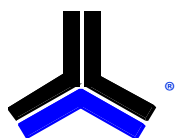
**ORDERING INFORMATION**

## Ordering Codes

Alliance	Organization	VCC range	Package	Operating Temp	Speed ns
<b>AS6C6264-55PCN</b>	8k x 8	2.7-5.5V	28pin 600mil PDIP	Commercial ~ 0° C to 70° C	55
<b>AS6C6264-55SCN</b>	8k x 8	2.7-5.5V	28pin 330mil SOP	Commercial ~ 0° C to 70° C	55
<b>AS6C6264-55SIN</b>	8k x 8	2.7-5.5V	28pin 330mil SOP	Industrial ~ -40° C to 85° C	55
<b>AS6C6264-55STCN</b>	8k x 8	2.7-5.5V	28pin sTSOP (8 x 13.4 mm)	Commercial ~ 0° C to 70° C	55
<b>AS6C6264-55STIN</b>	8k x 8	2.7-5.5V	28pin sTSOP (8 x 13.4 mm)	Industrial ~ -40° C to 85° C	55

## Part numbering system

<b>AS6C</b>	<b>6264</b>	<b>- 55</b>	<b>X</b>	<b>X</b>	<b>N</b>
low power SRAM prefix	Device Number <b>6264</b>	Access Time	Package Options: P = 28 pin 600 mil P-DIP S = 28 pin 330 mil SOP ST = 28 pin sTSOP (8mm x 13.4 mm)	Temperature Range: C = Commercial (0° C to +70° C) I = Industrial (-40° to +85° C)	N = Lead Free ROHS Compliant Part



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