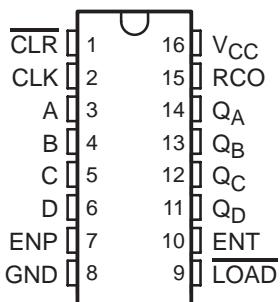


# SN54HC161, SN74HC161 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS297D – JANUARY 1996 – REVISED SEPTEMBER 2003

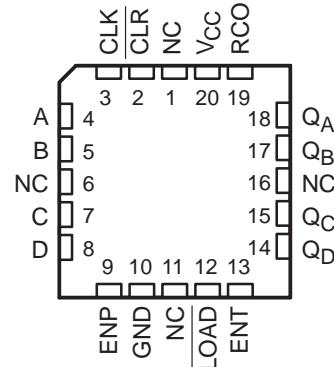
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max I<sub>CC</sub>
- Typical t<sub>pd</sub> = 14 ns
- $\pm 4$ -mA Output Drive at 5 V

SN54HC161 . . . J OR W PACKAGE  
SN74HC161 . . . D, N, NS, OR PW PACKAGE  
(TOP VIEW)



- Low Input Current of 1  $\mu$ A Max
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable

SN54HC161 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'HC161 devices are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC161N	SN74HC161N
	SOIC – D	Tube of 40	SN74HC161D	HC161
		Reel of 2500	SN74HC161DR	
		Reel of 250	SN74HC161DT	
	SOP – NS	Reel of 2000	SN74HC161NSR	HC161
	TSSOP – PW	Tube of 90	SN74HC161PW	HC161
		Reel of 2000	SN74HC161PWR	
		Reel of 250	SN74HC161PWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC161J	SNJ54HC161J
	CFP – W	Tube of 150	SNJ54HC161W	SNJ54HC161W
	LCCC – FK	Tube of 55	SNJ54HC161FK	SNJ54HC161FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# **SN54HC161, SN74HC161 4-BIT SYNCHRONOUS BINARY COUNTERS**

SCLS297D – JANUARY 1996 – REVISED SEPTEMBER 2003

---

## **description/ordering information (continued)**

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'HC161 devices is asynchronous. A low level at the clear ( $\overline{\text{CLR}}$ ) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ( $\overline{\text{LOAD}}$ ), or enable inputs.

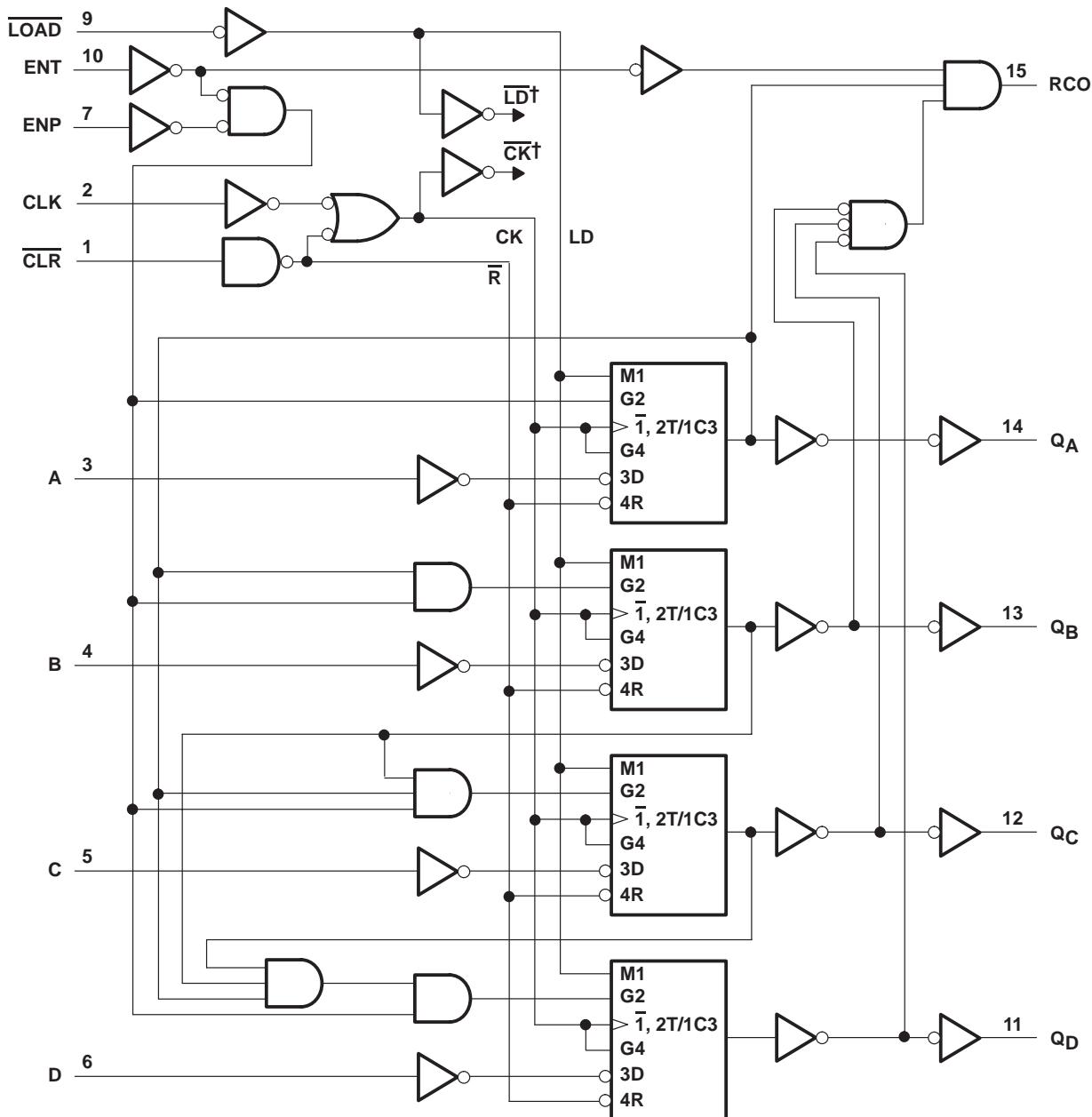
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry output (RCO). Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with  $Q_A$  high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or  $\overline{\text{LOAD}}$ ) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**logic diagram (positive logic)**



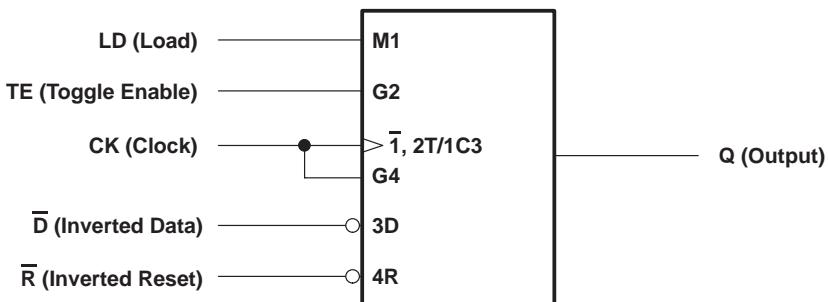
† For simplicity, routing of complementary signals  $\overline{LD}$  and  $\overline{CK}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

Pin numbers shown are for the D, J, N, NS, PW, and W packages.

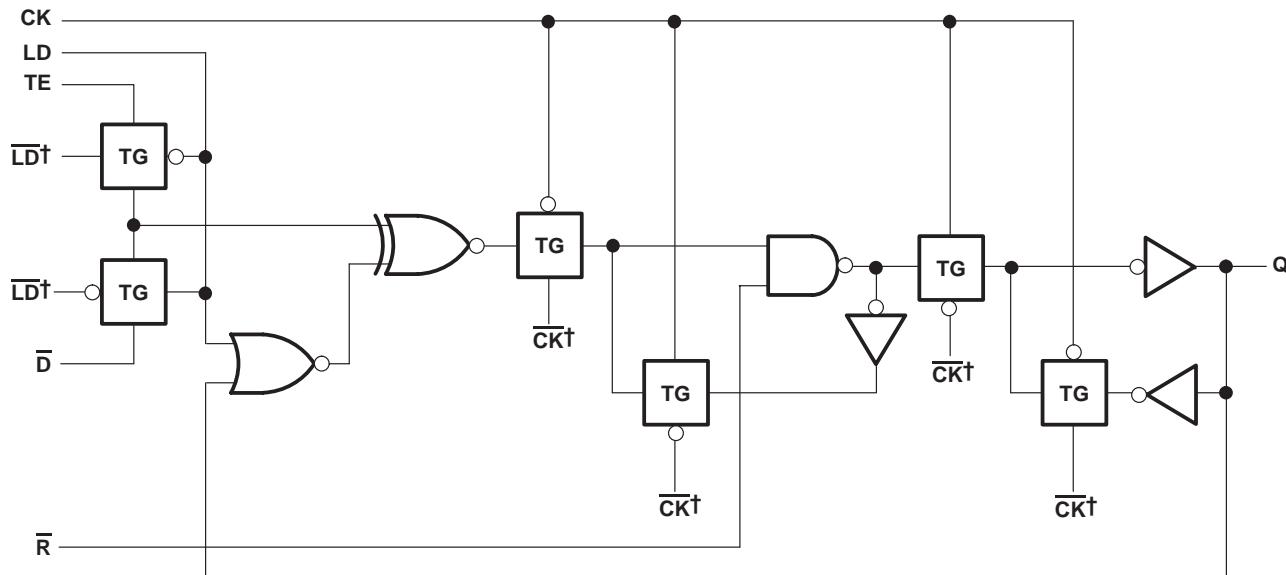
# SN54HC161, SN74HC161 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS297D – JANUARY 1996 – REVISED SEPTEMBER 2003

logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)

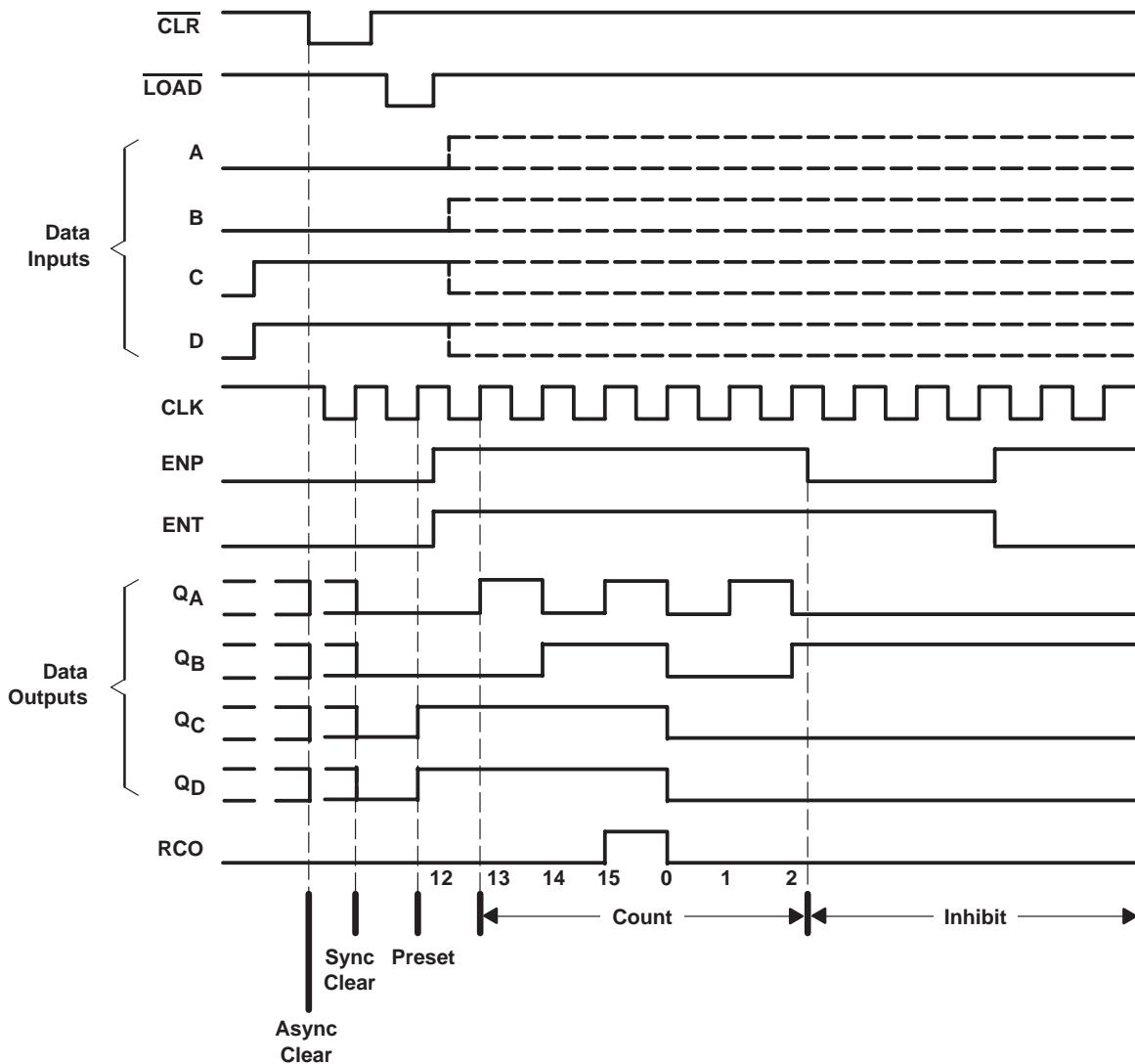


† The origins of  $\overline{LD}$  and  $\overline{CK}$  are shown in the logic diagram of the overall device.

### typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



# **SN54HC161, SN74HC161 4-BIT SYNCHRONOUS BINARY COUNTERS**

SCLS297D – JANUARY 1996 – REVISED SEPTEMBER 2003

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:** 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

		SN54HC161			SN74HC161			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5			V
		V <sub>CC</sub> = 4.5 V	3.15		3.15			
		V <sub>CC</sub> = 6 V	4.2		4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5		0.5		V
		V <sub>CC</sub> = 4.5 V		1.35		1.35		
		V <sub>CC</sub> = 6 V		1.8		1.8		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
$\Delta t/\Delta v^\ddagger$	Input transition rise/fall time	V <sub>CC</sub> = 2 V		1000		1000		ns
		V <sub>CC</sub> = 4.5 V		500		500		
		V <sub>CC</sub> = 6 V		400		400		
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

**NOTE 3:** All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

<sup>‡</sup>If this device is used in the threshold region (from  $V_{IL\max} = 0.5\text{ V}$  to  $V_{IH\min} = 1.5\text{ V}$ ), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_f = 1000\text{ ns}$  and  $V_{CC} = 2\text{ V}$  does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

**SN54HC161, SN74HC161**  
**4-BIT SYNCHRONOUS BINARY COUNTERS**

SCLS297D – JANUARY 1996 – REVISED SEPTEMBER 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC161	SN74HC161	UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 µA	2 V	1.9	1.998	1.9	1.9	V
			4.5 V	4.4	4.499	4.4	4.4	
			6 V	5.9	5.999	5.9	5.9	
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3	3.7	3.84	V
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8	5.2	5.34	
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA	2 V	0.002	0.1	0.1	0.1	V
			4.5 V	0.001	0.1	0.1	0.1	
			6 V	0.001	0.1	0.1	0.1	
		I <sub>OL</sub> = 4 mA	4.5 V	0.17	0.26	0.4	0.33	V
		I <sub>OL</sub> = 5.2 mA	6 V	0.15	0.26	0.4	0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V	±0.1	±100	±1000	±1000	nA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V		8	160	160	80	µA
C <sub>i</sub>		2 V to 6 V	3	10	10	10	10	pF

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC161	SN74HC161	UNIT
			MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	6	4.2	5		MHz
		4.5 V	31	21	25		
		6 V	36	25	29		
t <sub>w</sub>	Pulse duration	CLK high or low	2 V	80	120	100	ns
			4.5 V	16	24	20	
			6 V	14	20	17	
		CLR low	2 V	80	120	100	
			4.5 V	16	24	20	
			6 V	14	20	17	
t <sub>su</sub>	Setup time before CLK↑	A, B, C, or D	2 V	150	225	190	ns
			4.5 V	30	45	38	
			6 V	26	38	32	
		LOAD low	2 V	135	205	170	
			4.5 V	27	41	34	
			6 V	23	35	29	
		ENP, ENT	2 V	170	255	215	
			4.5 V	34	51	43	
			6 V	29	43	37	
		CLR inactive	2 V	125	190	155	
			4.5 V	25	38	31	
			6 V	21	32	26	
t <sub>h</sub>	Hold time, all synchronous inputs after CLK↑	2 V	0	0	0		ns
		4.5 V	0	0	0		
		6 V	0	0	0		

# SN54HC161, SN74HC161 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS297D – JANUARY 1996 – REVISED SEPTEMBER 2003

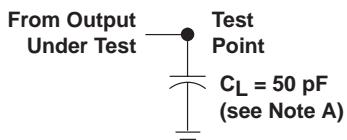
**switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC161	SN74HC161	UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{max}$			2 V	6	14		4.2	5	MHz
			4.5 V	31	40		21	25	
			6 V	36	44		25	29	
$t_{pd}$	CLK	RCO	2 V	83	215		325	270	ns
			4.5 V	24	43		65	54	
			6 V	20	37		55	46	
		Any Q	2 V	80	205		310	255	
			4.5 V	25	41		62	51	
			6 V	21	35		53	43	
	ENT	RCO	2 V	62	195		295	245	
			4.5 V	17	39		59	49	
			6 V	14	33		50	42	
		Any Q	2 V	105	210		315	265	ns
			4.5 V	21	42		63	53	
			6 V	18	36		54	45	
		RCO	2 V	110	220		330	275	
			4.5 V	22	44		66	55	
			6 V	19	37		56	47	
$t_t$		Any	2 V	38	75		110	95	ns
			4.5 V	8	15		22	19	
			6 V	6	13		19	16	

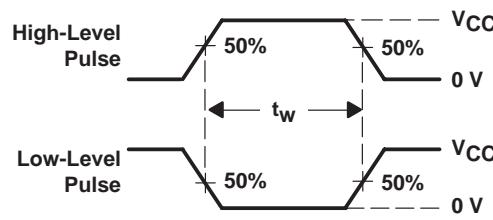
## operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load	60	pF

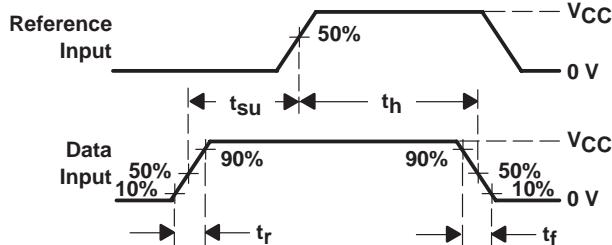
### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

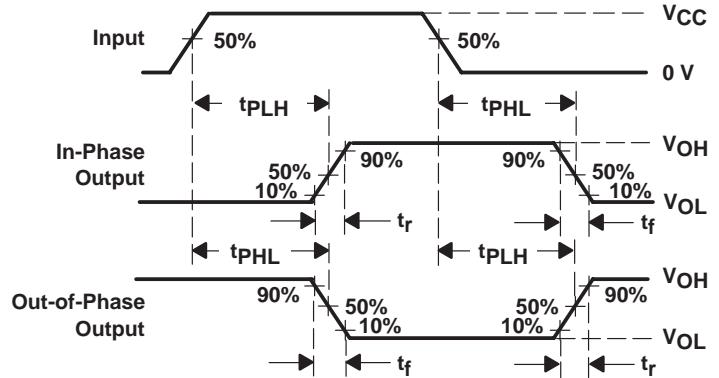


VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS

SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - The outputs are measured one at a time with one input transition per measurement.
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

# **SN54HC161, SN74HC161 4-BIT SYNCHRONOUS BINARY COUNTERS**

SCLS297D – JANUARY 1996 – REVISED SEPTEMBER 2003

---

## **APPLICATION INFORMATION**

### **n-bit synchronous counters**

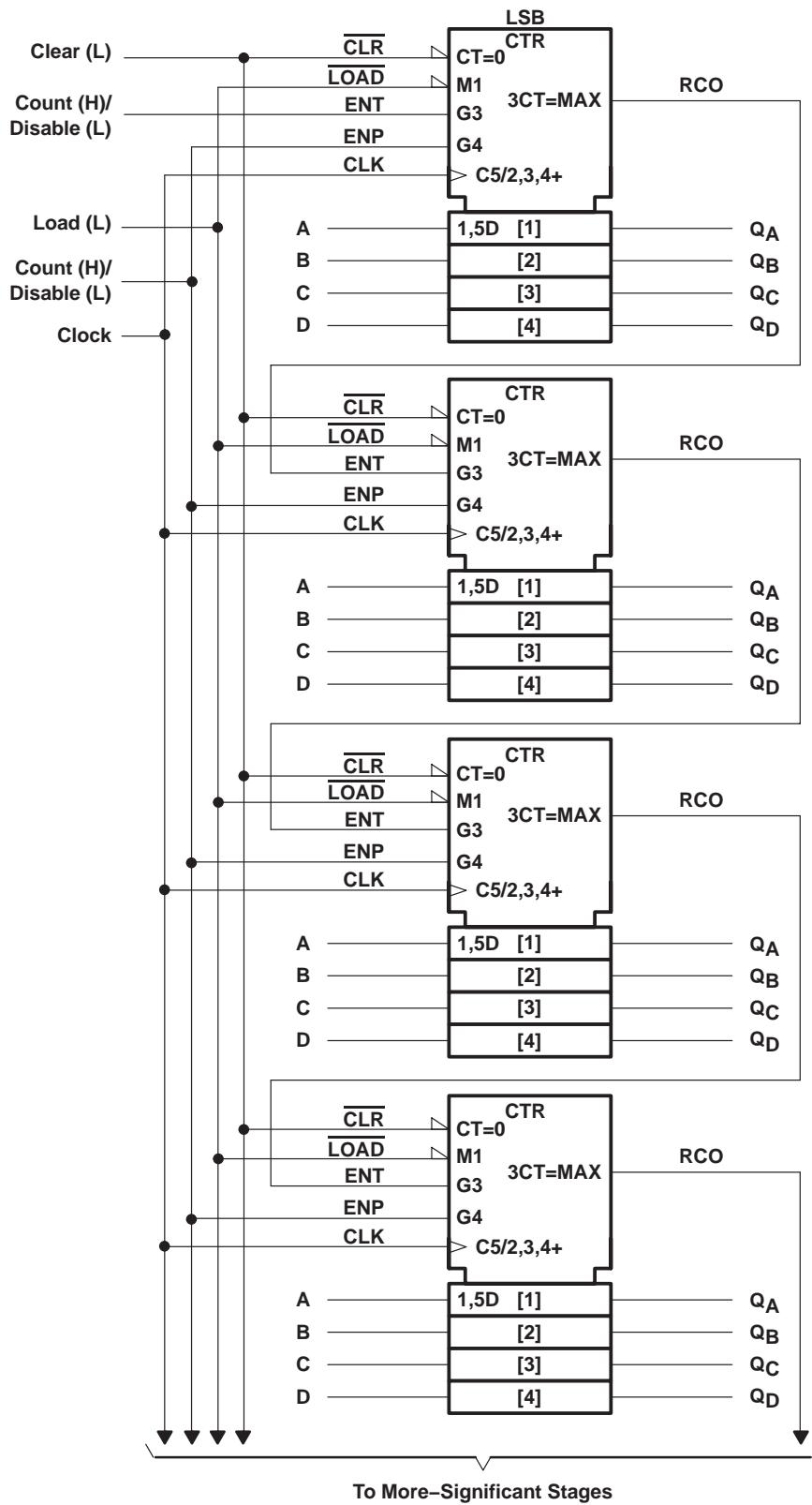
This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'HC161 devices count in binary. Virtually any count mode (modulo-N, N<sub>1</sub>-to-N<sub>2</sub>, N<sub>1</sub>-to-maximum) can be used with this fast look-ahead circuit.

The application circuit shown in Figure 2 is not valid for clock frequencies above 18 MHz (at 25°C and 4.5-V V<sub>CC</sub>). The reason for this is that there is a glitch that is produced on the second stage's RCO and every succeeding stage's RCO. This glitch is common to all HC vendors that Texas Instruments has evaluated, in addition to the bipolar equivalents (LS, ALS, AS).



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**APPLICATION INFORMATION**



To More-Significant Stages

**Figure 2**

# SN54HC161, SN74HC161 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS297D – JANUARY 1996 – REVISED SEPTEMBER 2003

## APPLICATION INFORMATION

The glitch on RCO is caused because the propagation delay of the rising edge of  $Q_A$  of the second stage is shorter than the propagation delay of the falling edge of ENT. RCO is the product of ENT,  $Q_A$ ,  $Q_B$ ,  $Q_C$ , and  $Q_D$  ( $ENT \times Q_A \times Q_B \times Q_C \times Q_D$ ). The resulting glitch is about 7–12 ns in duration. Figure 3 shows the condition in which the glitch occurs. For simplicity, only two stages are being considered, but the results can be applied to other stages.  $Q_B$ ,  $Q_C$ , and  $Q_D$  of the first and second stage are at logic one, and  $Q_A$  of both stages are at logic zero (1110 1110) after the first clock pulse. On the rising edge of the second clock pulse,  $Q_A$  and RCO of the first stage go high. On the rising edge of the third clock pulse,  $Q_A$  and RCO of the first stage return to a low level, and  $Q_A$  of the second stage goes to a high level. At this time, the glitch on RCO of the second stage appears because of the race condition inside the chip.

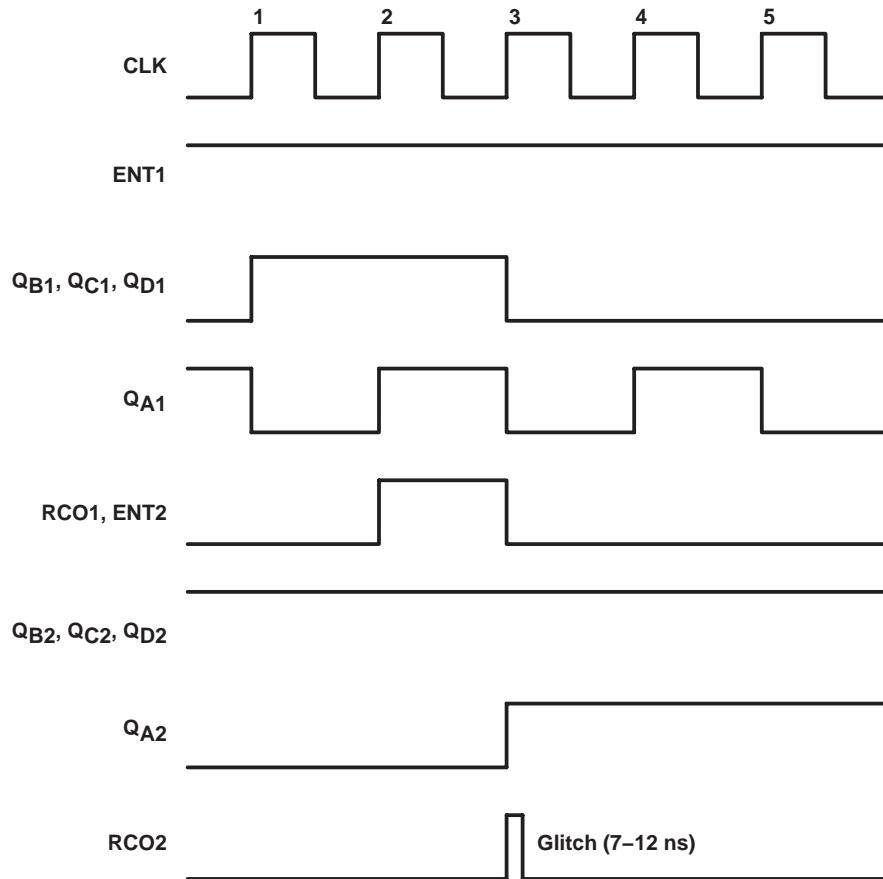


Figure 3

The glitch causes a problem in the next stage (stage three) if the glitch is still present when the next rising clock edge appears (clock pulse 4). To ensure that this does not happen, the clock frequency must be less than the inverse of the sum of the clock-to-RCO propagation delay and the glitch duration ( $t_g$ ). In other words,  $f_{max} = 1/(t_{pd} CLK-to-RCO + t_g)$ . For example, at 25°C at 4.5-V  $V_{CC}$ , the clock-to-RCO propagation delay is 43 ns and the maximum duration of the glitch is 12 ns. Therefore, the maximum clock frequency that the cascaded counters can use is 18 MHz. The following tables contain the  $f_{clock}$ ,  $t_w$ , and  $f_{max}$  specifications for applications that use more than two 'HC161 devices cascaded together.

## APPLICATION INFORMATION

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC161		SN74HC161		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
<i>f<sub>clock</sub></i>	Clock frequency	2 V	3.6		2.5		2.9		MHz
		4.5 V		18		12		14	
		6 V		21		14		17	
<i>t<sub>w</sub></i>	Pulse duration, CLK high or low	2 V	140		200		170		ns
		4.5 V	28		40		36		
		6 V	24		36		30		

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Note 4)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC161		SN74HC161		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
<i>f<sub>max</sub></i>			2 V	3.6		2.5		2.9		MHz
			4.5 V	18		12		14		
			6 V	21		14		17		

NOTE 4: These limits apply only to applications that use more than two 'HC161 devices cascaded together.

If the 'HC161 devices are used as a single unit, or only two cascaded together, then the maximum clock frequency that the device can use is not limited because of the glitch. In these situations, the device can be operated at the maximum specifications.

A glitch can appear on RCO of a single 'HC161 device, depending on the relationship of ENT to CLK. Any application that uses RCO to drive any input except an ENT of another cascaded 'HC161 device must take this into consideration.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8407501VEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8407501VEA SNV54HC161J
5962-8407501VEA.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8407501VEA SNV54HC161J
84075012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84075012A SNJ54HC161FK
8407501EA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407501EA SNJ54HC161J
8407501FA	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407501FA SNJ54HC161W
JM38510/66302BEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 66302BEA
JM38510/66302BEA.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 66302BEA
M38510/66302BEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 66302BEA
SN54HC161J	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC161J
SN54HC161J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC161J
SN74HC161D	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-40 to 85	HC161
SN74HC161DR	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161
SN74HC161DR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161
SN74HC161DRE4	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161
SN74HC161DT	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-40 to 85	HC161
SN74HC161N	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC161N
SN74HC161N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC161N
SN74HC161NSR	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161
SN74HC161NSR.A	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161
SN74HC161PW	Obsolete	Production	TSSOP (PW)   16	-	-	Call TI	Call TI	-40 to 85	HC161
SN74HC161PWR	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC161PWR.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC161
<a href="#">SN74HC161PWT</a>	Obsolete	Production	TSSOP (PW)   16	-	-	Call TI	Call TI	-40 to 85	HC161
<a href="#">SNJ54HC161FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84075012A SNJ54HC 161FK
SNJ54HC161FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84075012A SNJ54HC 161FK
<a href="#">SNJ54HC161J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407501EA SNJ54HC161J
SNJ54HC161J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407501EA SNJ54HC161J
<a href="#">SNJ54HC161W</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407501FA SNJ54HC161W
SNJ54HC161W.A	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407501FA SNJ54HC161W

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

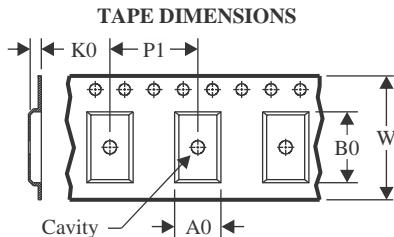
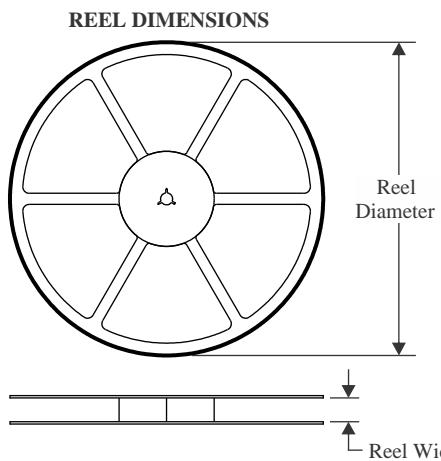
**OTHER QUALIFIED VERSIONS OF SN54HC161, SN54HC161-SP, SN74HC161 :**

- Catalog : [SN74HC161](#), [SN54HC161](#)
- Military : [SN54HC161](#)
- Space : [SN54HC161-SP](#)

**NOTE: Qualified Version Definitions:**

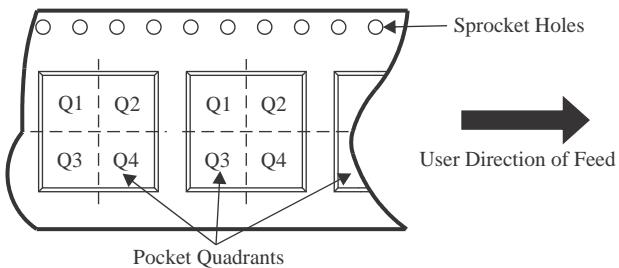
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



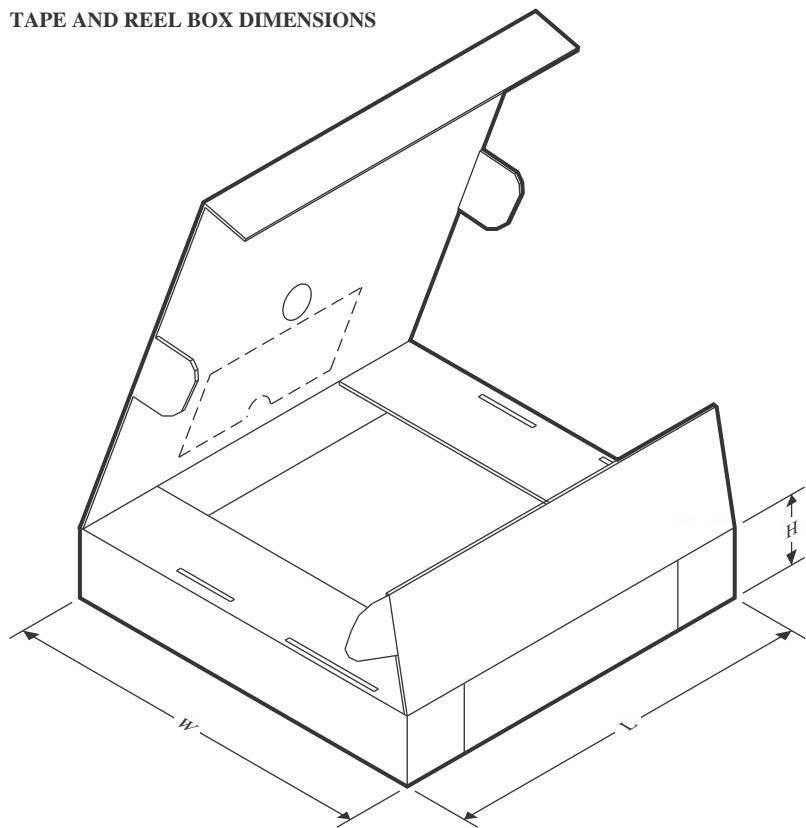
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



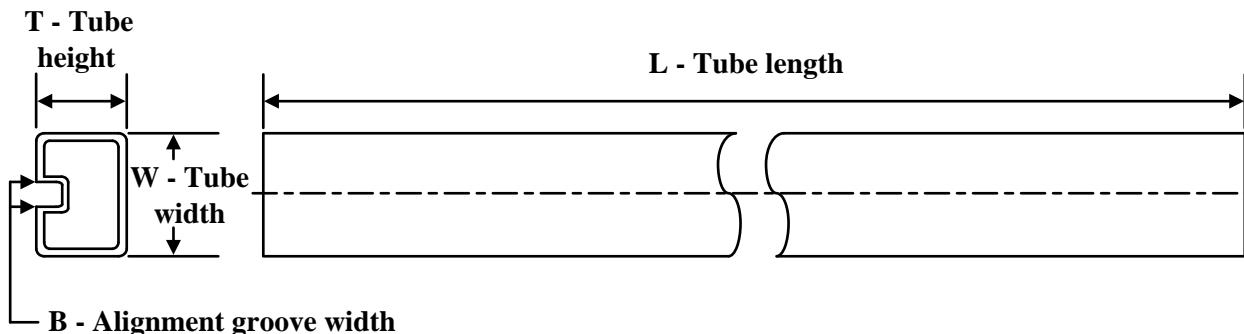
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC161DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC161NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HC161PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC161DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC161NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74HC161PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
84075012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8407501FA	W	CFP	16	25	506.98	26.16	6220	NA
SN74HC161N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC161N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC161N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC161N.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC161FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC161FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC161W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54HC161W.A	W	CFP	16	25	506.98	26.16	6220	NA

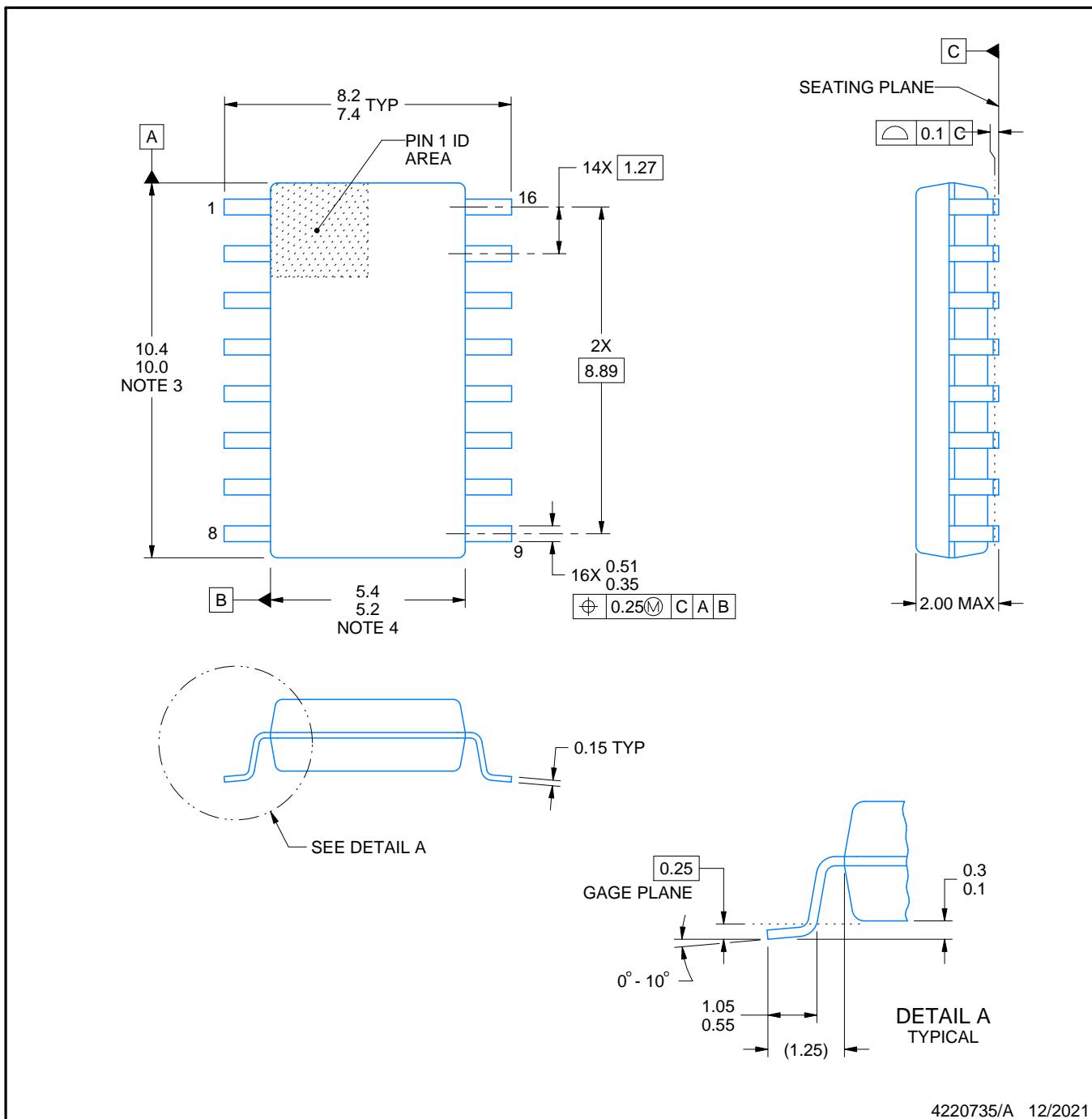
**NS0016A**



# PACKAGE OUTLINE

**SOP - 2.00 mm max height**

SOP



4220735/A 12/2021

## NOTES:

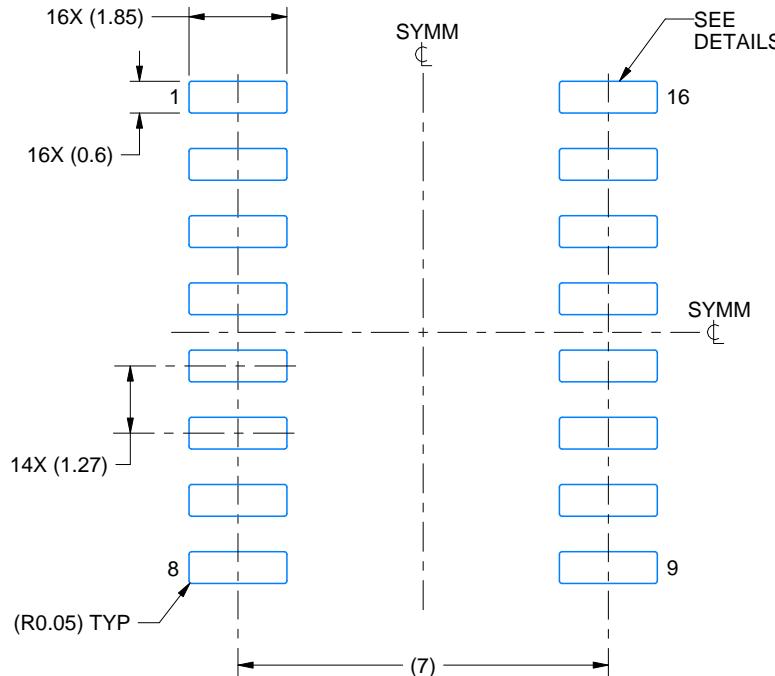
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

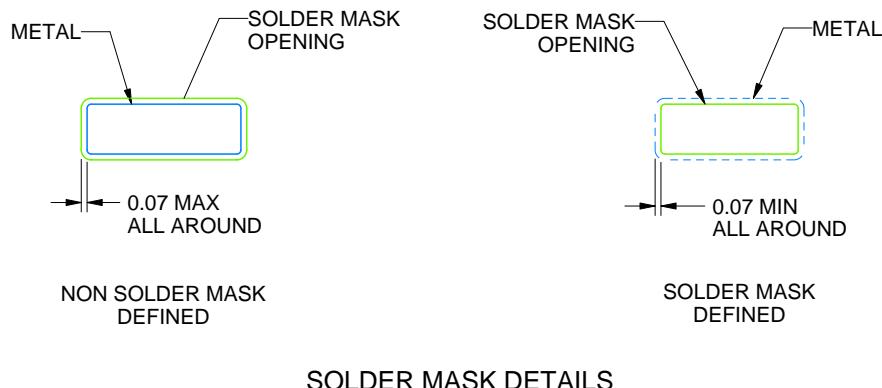
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE  
SCALE:7X



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

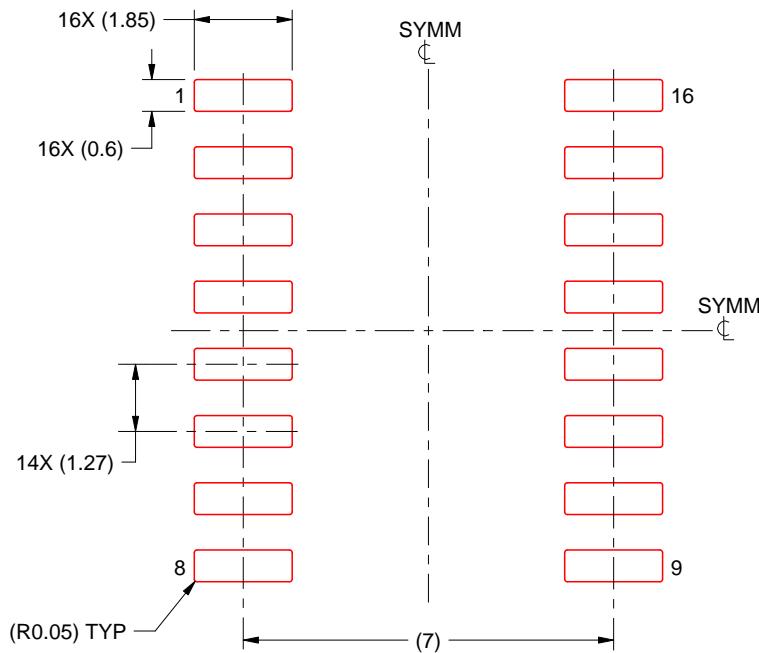
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

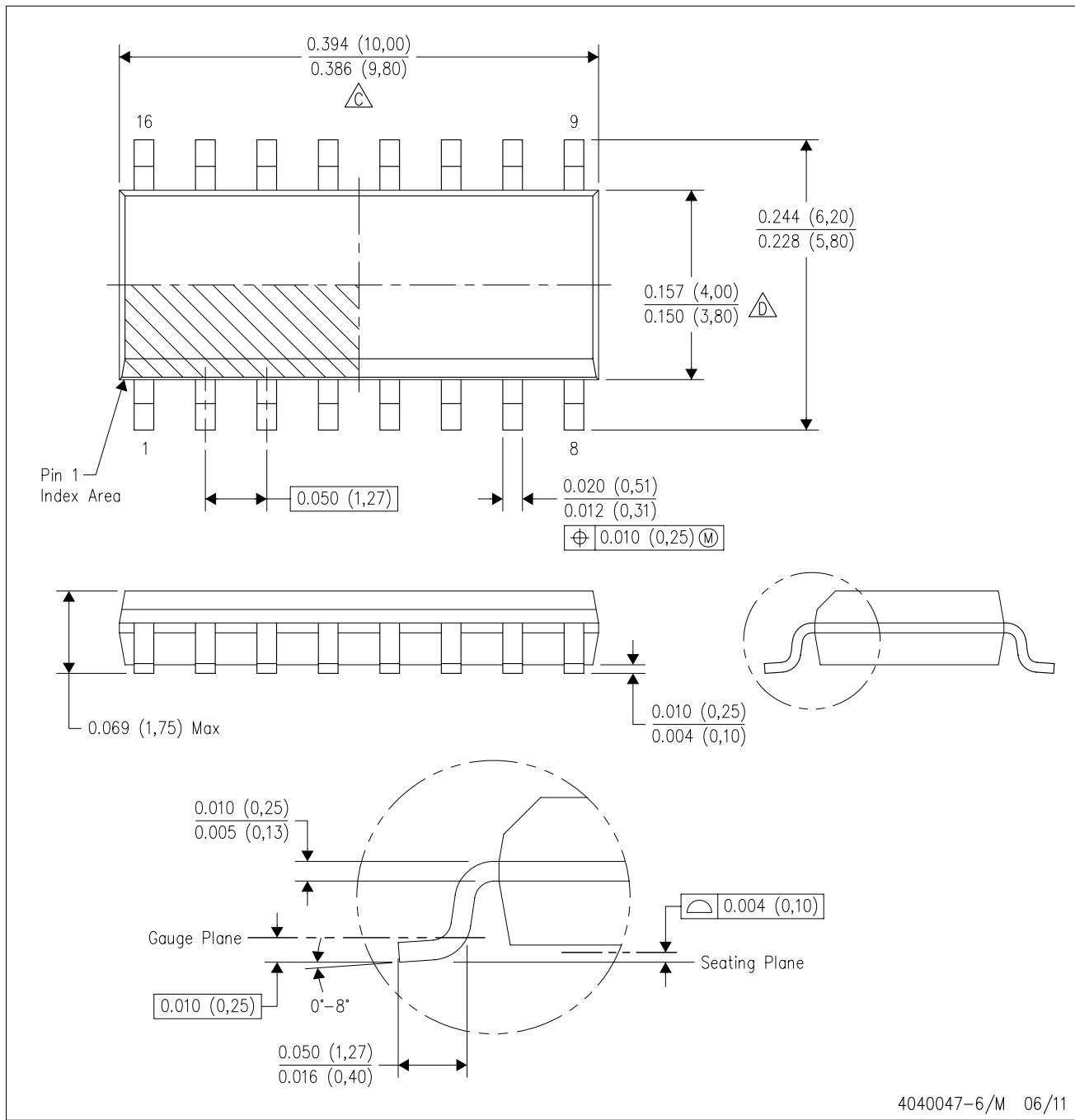
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

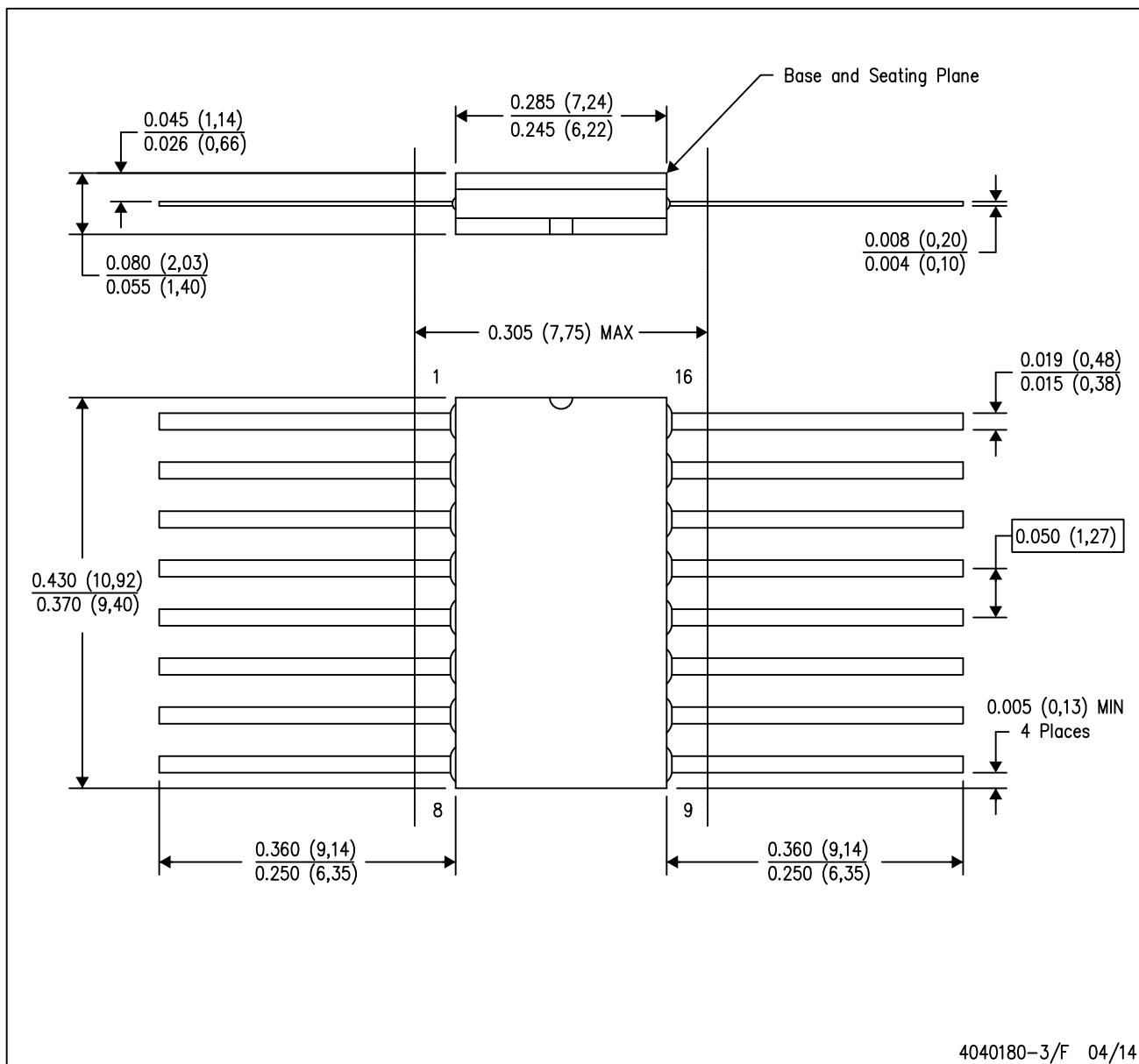
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

## MECHANICAL DATA

W (R-GDFP-F16)

## CERAMIC DUAL FLATPACK



4040180-3/F 04/14

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2-F16

# GENERIC PACKAGE VIEW

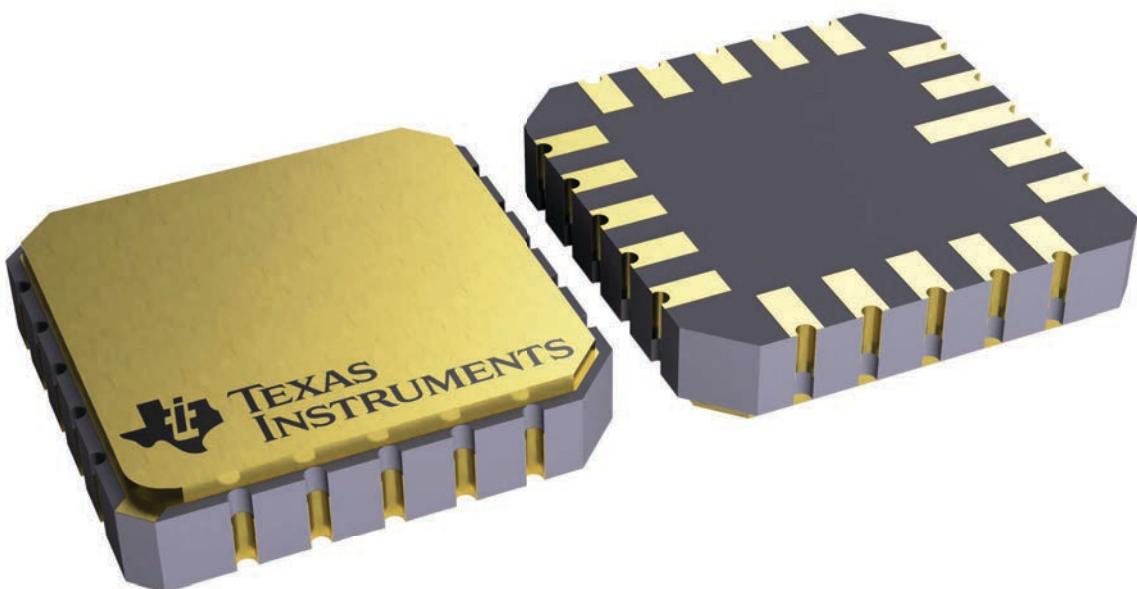
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

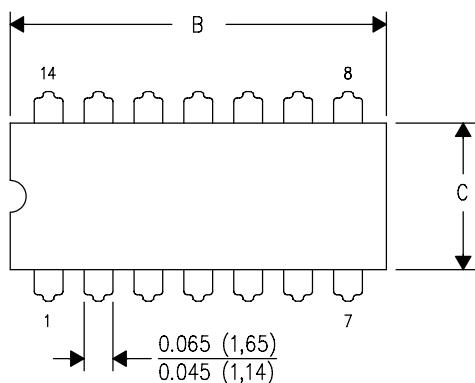


4229370VA\

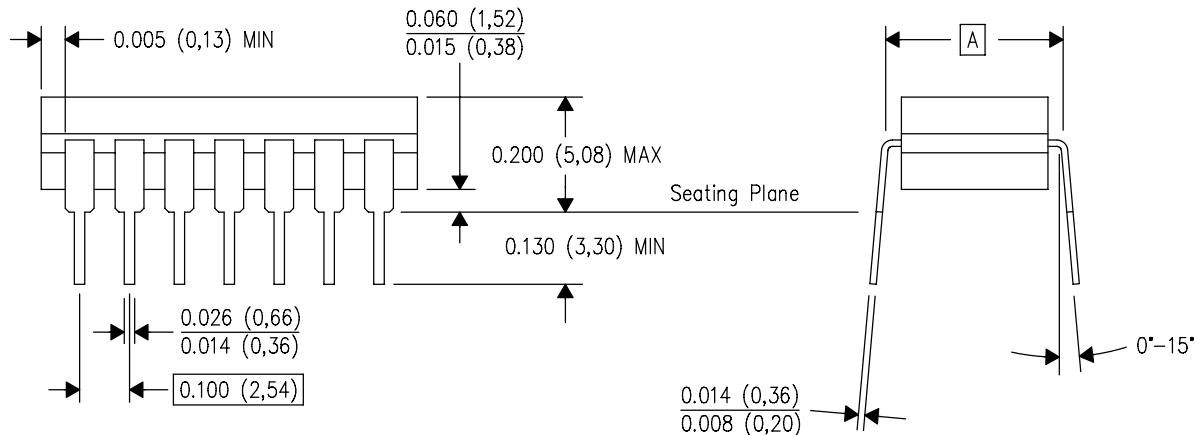
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **\nDIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

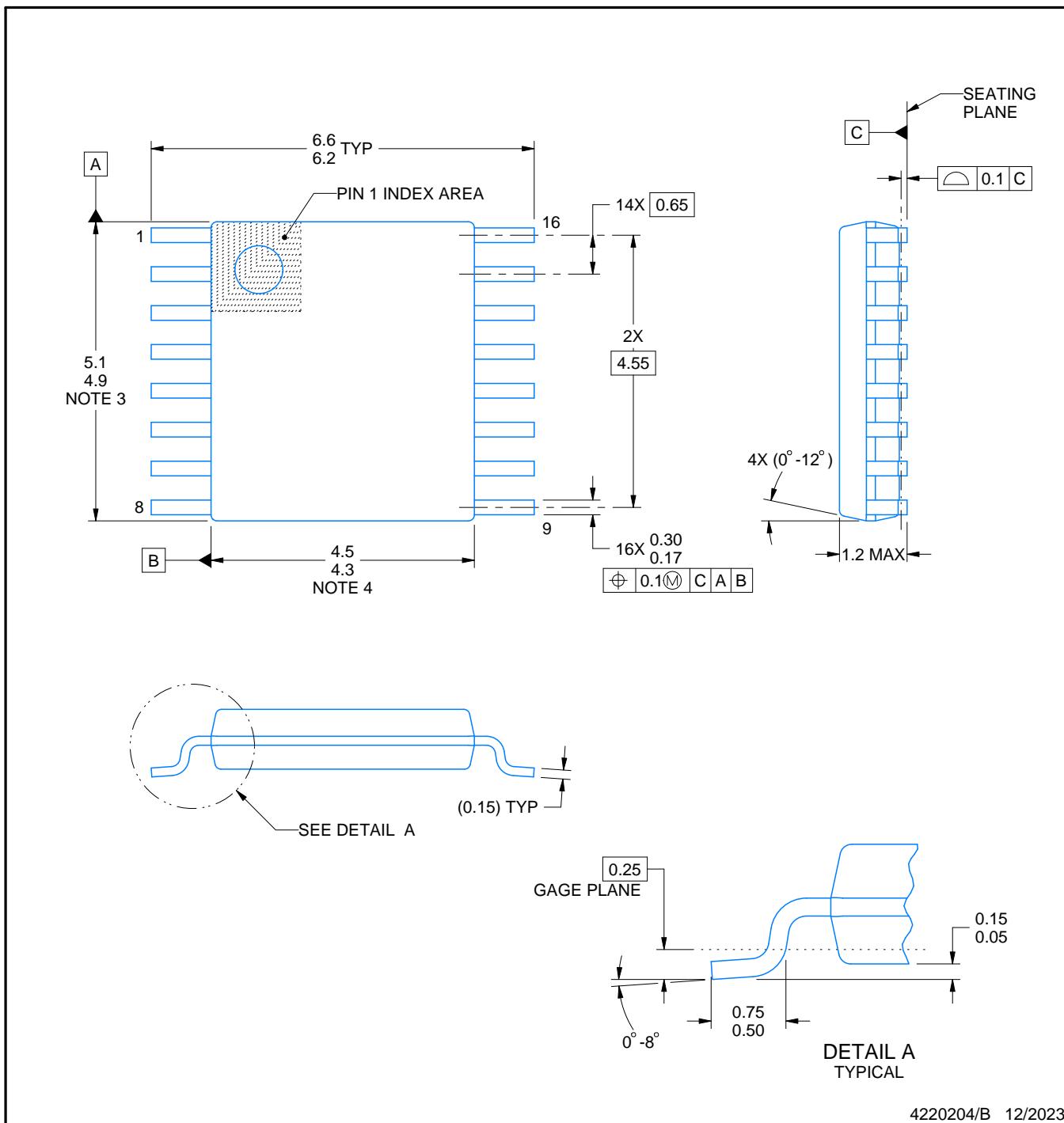
# PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

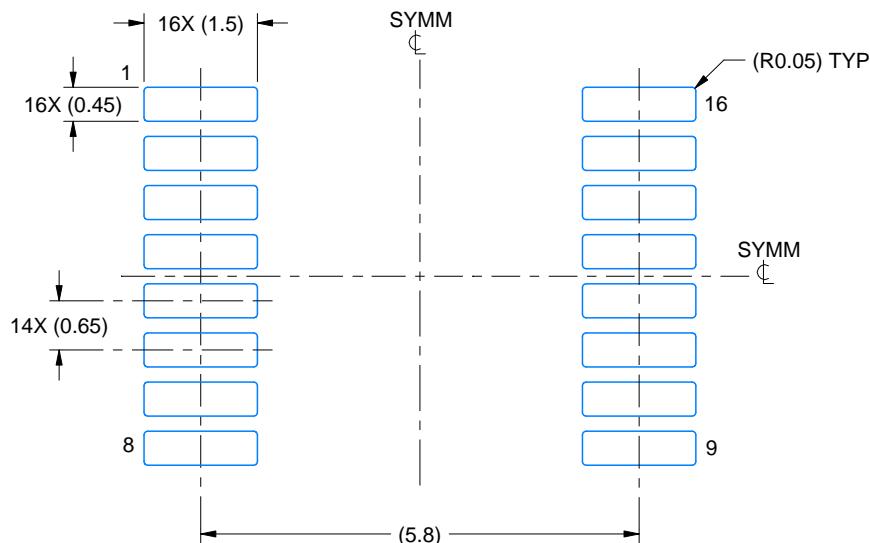
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

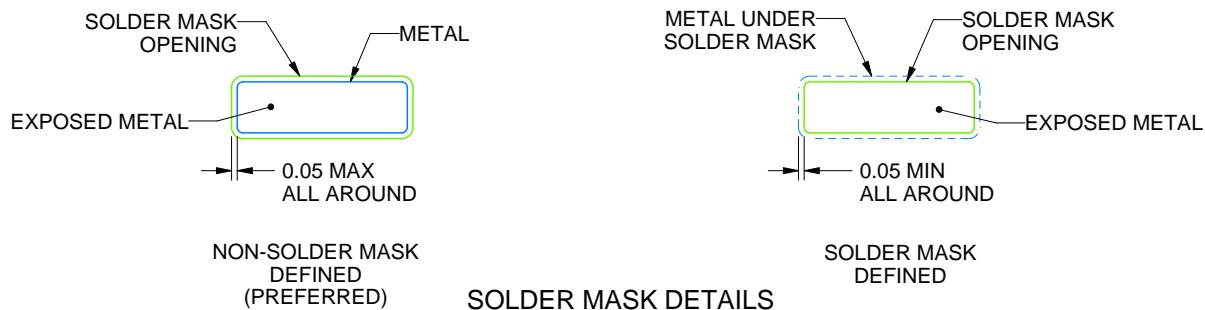
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

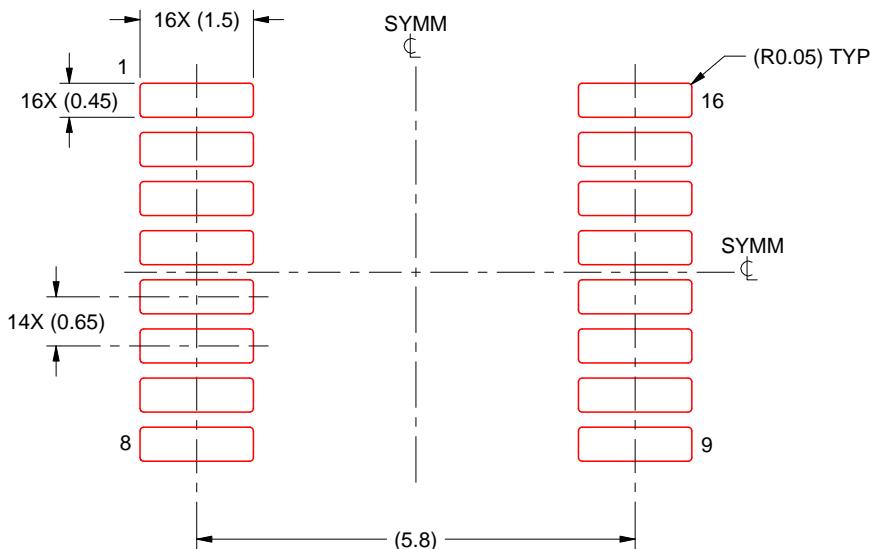
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

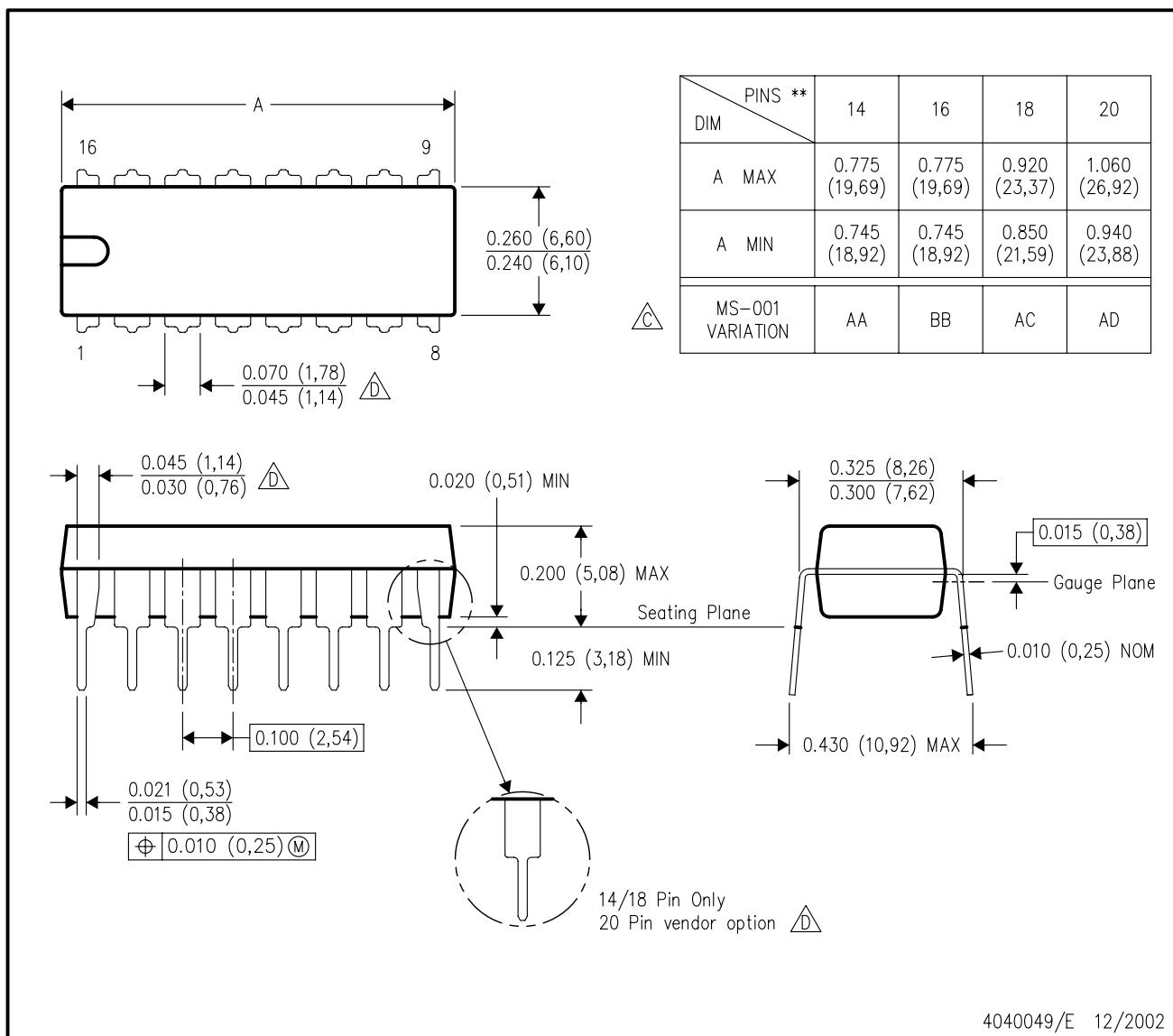
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



## **IMPORTANT NOTICE AND DISCLAIMER**

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025