Page 2
Power,Flash,SDcard
User switch,Reset switch.

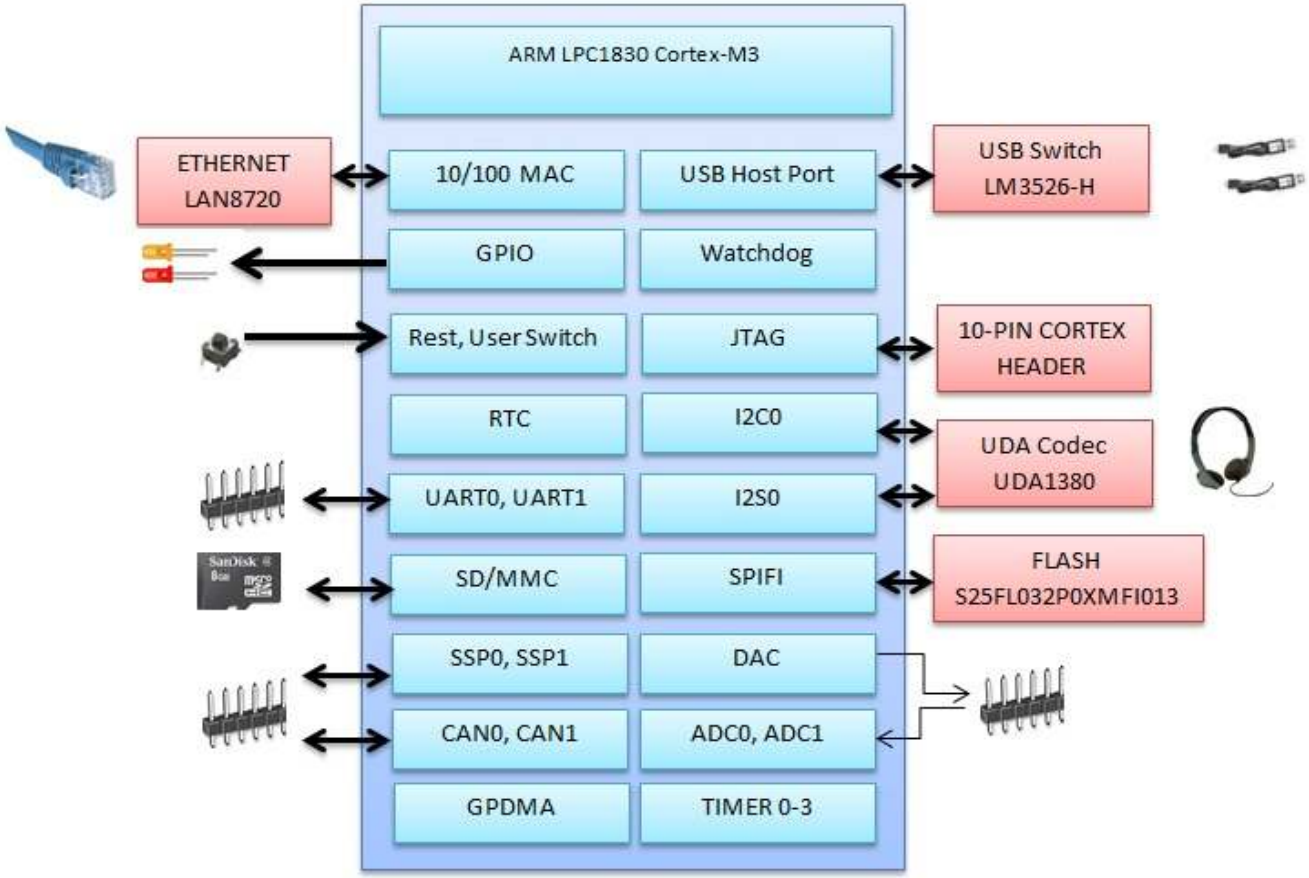
Page 3
Ethernet

Page 4
Audio

Page 5
USB

Page 6
JTAG,BOOTSW,LED,Header

Design Overview



Disclaimer:

Schematic's are for reference only.
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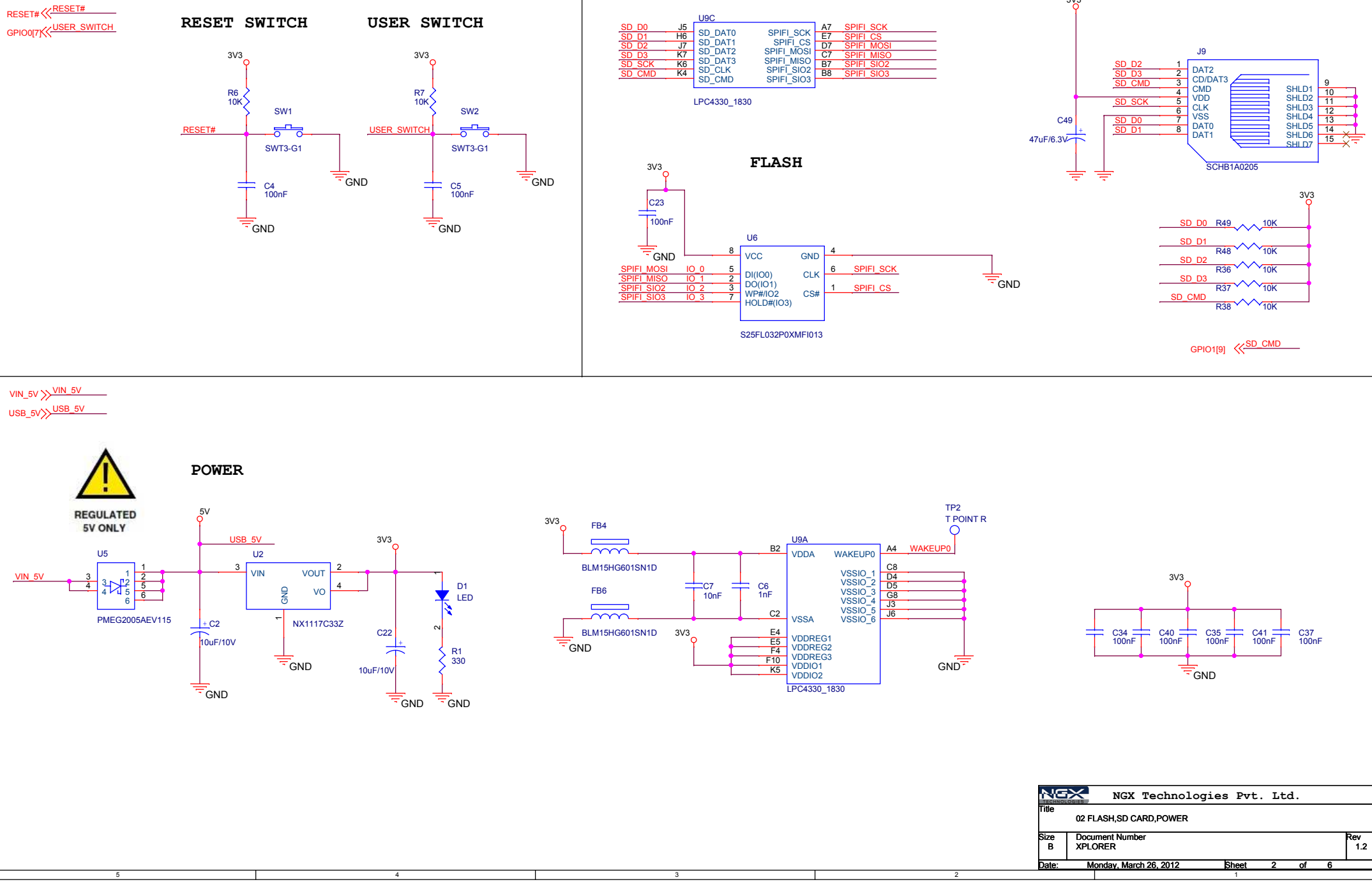
Title: 01 COVER		
Size: B	Document Number: XPLORER	Rev: 1.2
Date: Monday, March 26, 2012	Sheet 1 of 6	


RESET#
GPIO0[7]
USER_SWITCH
RESET SWITCH
USER SWITCH
3V3
R6
10K
SW1
RESET#
SWT3-G1
C4
100nF
GND
R7
10K
SW2
USER_SWITCH
SWT3-G1
C5
100nF
U9C
SD_D0
SD_D1
SD_D2
SD_D3
SD_SCK
SD_CMD
SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3
SD_CLK
SD_CMD
SPIFI_SCK
SPIFI_CS
SPIFI_MOSI
SPIFI_MISO
SPIFI_SIO2
SPIFI_SIO3
LPC4330_1830
SD CARD
J9
DAT2
CD/DAT3
CMD
VDD
CLK
VSS
DAT0
DAT1
SHLD1
SHLD2
SHLD3
SHLD4
SHLD5
SHLD6
SHLD7
SCHB1A0205
C49
47uF/6.3V
FLASH
C23
100nF
U6
VCC
GND
DI(IO0)
DO(IO1)
WP#/IO2
HOLD#(IO3)
CLK
CS#
IO_0
IO_1
IO_2
IO_3
S25FL032P0XMFI013
R49
R48
R36
R37
R38
10K
GPIO1[9]
VIN_5V
USB_5V
POWER
REGULATED
5V ONLY
5V
U5
PMEG2005AEV115
U2
VIN
VOUT
GND
VO
NX1117C33Z
C2
10uF/10V
C22
10uF/10V
D1
LED
R1
330
FB4
FB6
BLM15HG601SN1D
C7
10nF
C6
1nF
U9A
VDDA
WAKEUP0
VSSIO_1
VSSIO_2
VSSIO_3
VSSIO_4
VSSIO_5
VSSIO_6
VSSA
VDDREG1
VDDREG2
VDDREG3
VDDIO1
VDDIO2
LPC4330_1830
TP2
T POINT R
C34
C40
C35
C41
C37
100nF
NGX Technologies Pvt. Ltd.
Title
02 FLASH,SD CARD,POWER
Size
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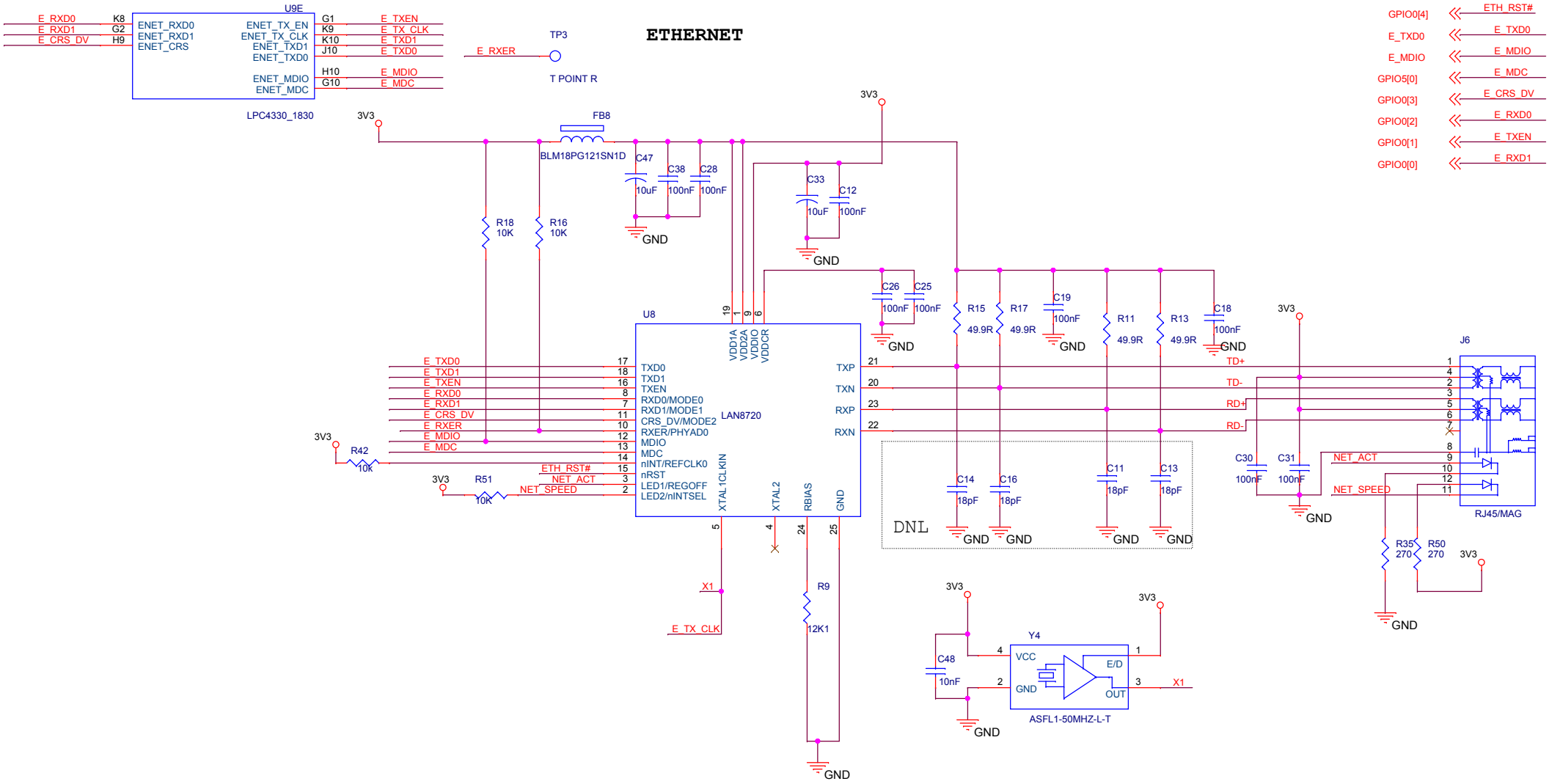
Document Number
XPLORER
Rev
1.2
Date:
Monday, March 26, 2012
Sheet
2
of
6

ETHERNET



ETHERNET ROUTING GUIDELINES

=>Keep the trace length difference between TX+ and TX- (or RX+ and RX-) in 700 mils.
=> Keep RX+/- signal on the top layer, the RX+/- signal should avoid any vias, if possible. Avoid right angle signal trace.
=>The crystal/oscillator clock and the switching noise from digital signals should be far away from TX+/-, RX+/- pairs.
=>Keep TX, RX differential signals running symmetric, equal length, and closely. The trace spacing between TX+ and TX- or between RX+ and RX- pair should be in 8 ~ 10 mils.
The better spacing between TX+/- and RX+/- pairs should be larger than 200 mils
=>The trace length from LAN8720 to the transformer should not be longer than 5 inches, keep the trace as straight as possible, and keep it parallel for differential pairs.
=>The termination resistors 49.9Ω and capacitors of TX± and RX± pairs should be placed near the transformer side and should be shorter than 400 mils.

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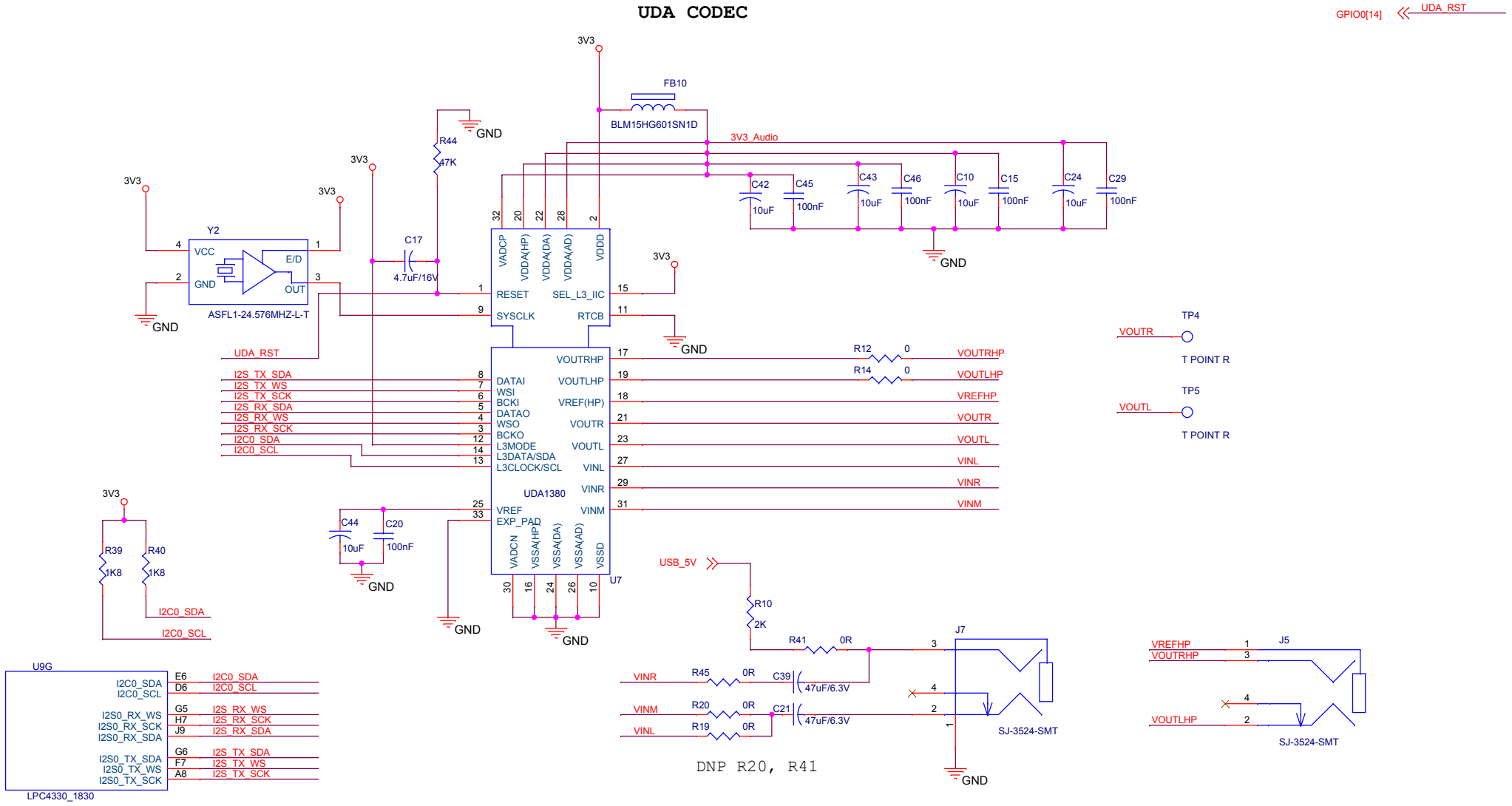
Title: 03 ETHERNET		
Size: B	Document Number: XPLORER	Rev: 1.2
Date: Monday, March 26, 2012	Sheet 3 of 6	

UDA CODEC



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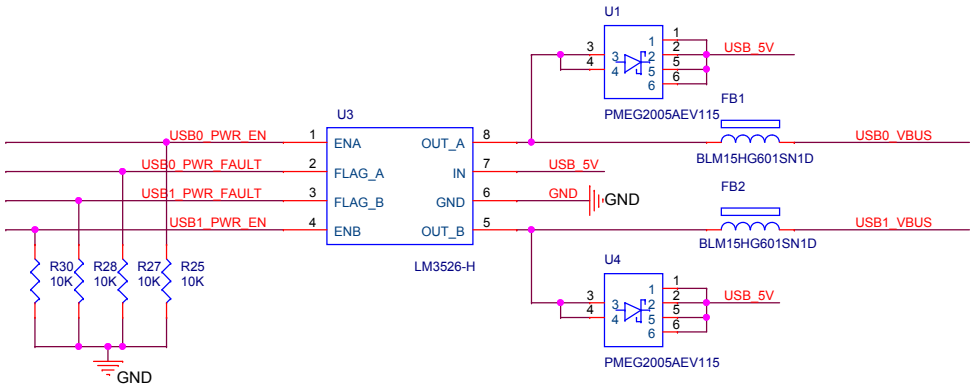
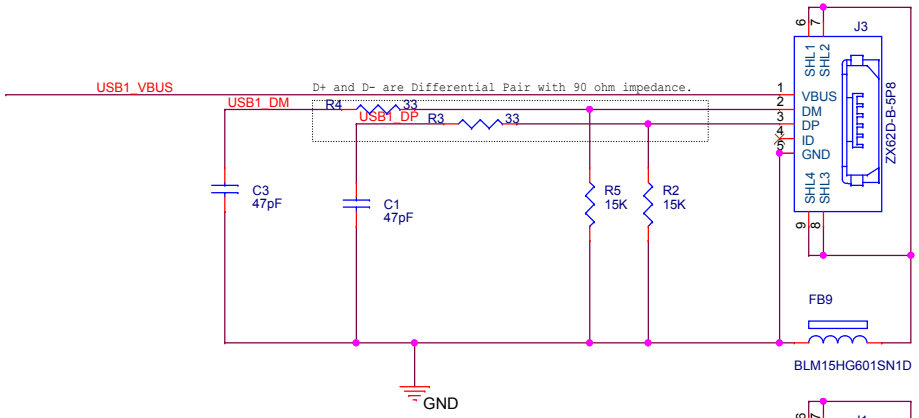
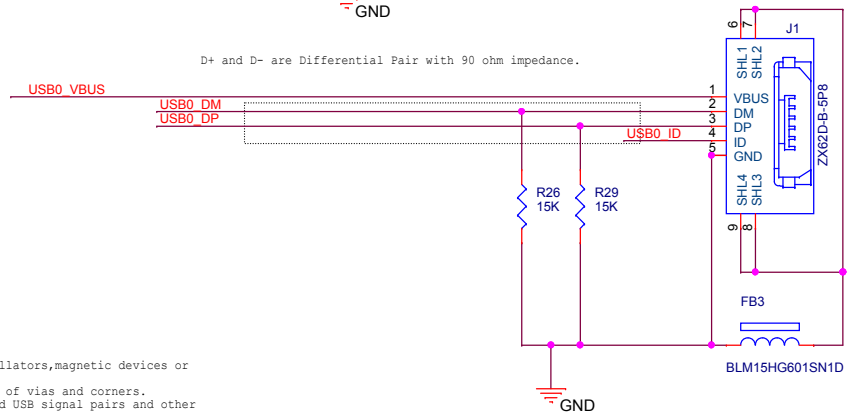
Title	04 AUDIO
Size	B
Document Number	XPLORER
Rev	1.2
Date:	Monday, March 26, 2012
Sheet	4 of 6

USB SECTION



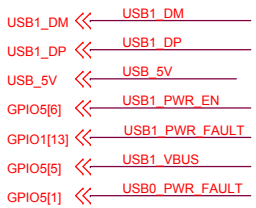
USB1 Power enable and fault pins are monitored/controlled using GPIO.

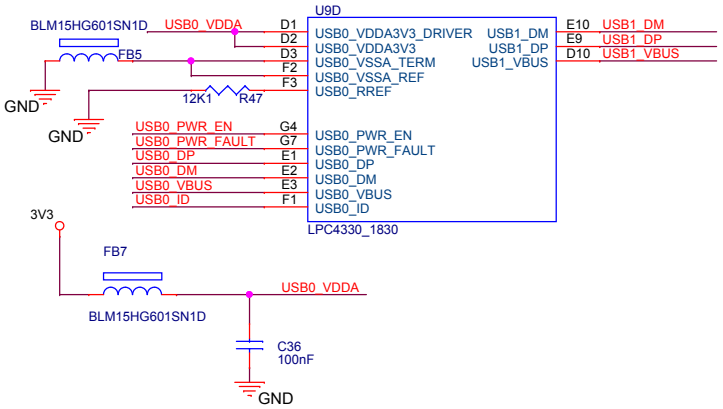




USB ROUTING GUIDELINES

=>Route USB trace pairs together [DM & DP].
=>Do not route USB traces under crystals, oscillators,magnetic devices or ICs that use and/or duplicate clocks.
=>Route high-speed USB signals using a minimum of vias and corners.
=>Use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality.





	1/0
USB0_PWR_EN	HOST/DEVICE
USB1_PWR_EN	HOST/DEVICE

NOTE:- When both USB0 and USB1 are in Host mode external 5V DC to be given to J8 pin 2.

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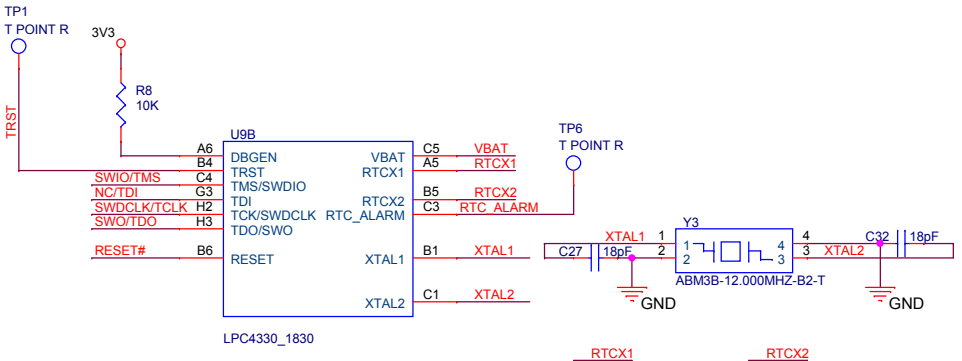
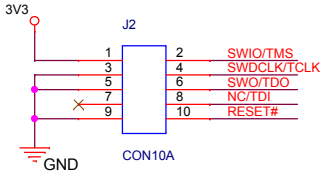
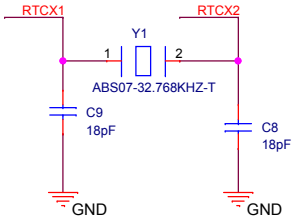
Title: 05 USB		
Size: B	Document Number: XPLORER	Rev: 1.2
Date: Monday, March 26, 2012	Sheet 5 of 6	

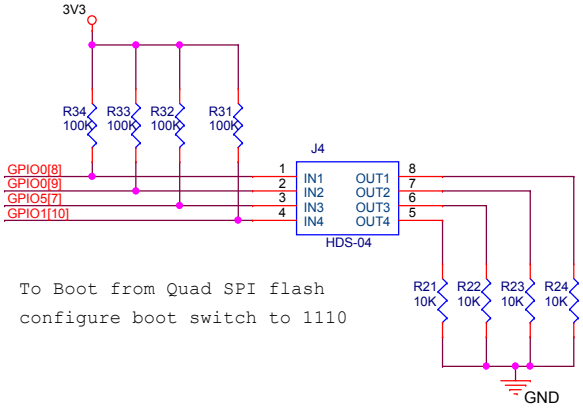


JTAG

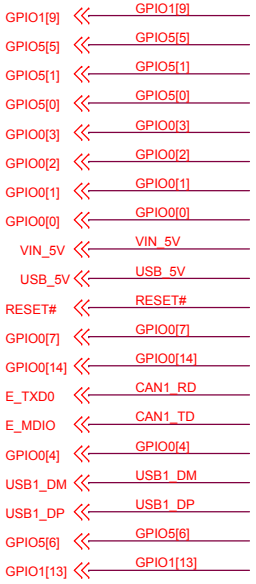




BOOT SELECT SWITCH

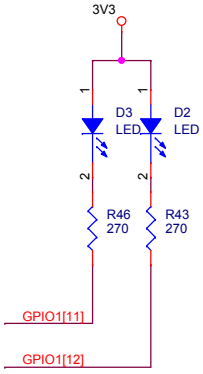


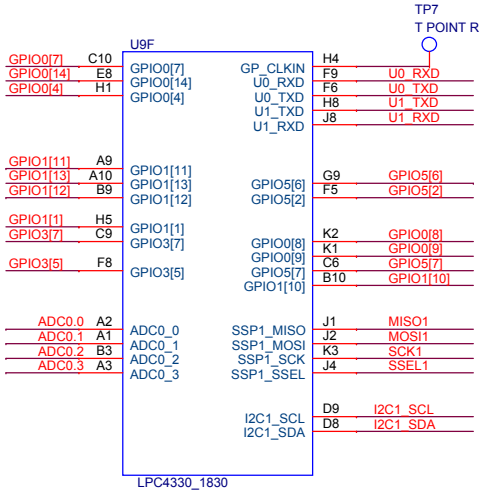
To Boot from Quad SPI flash
configure boot switch to 1110

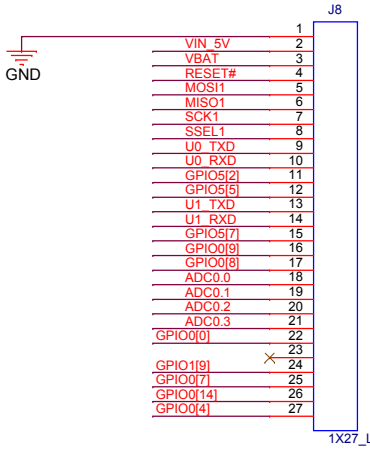


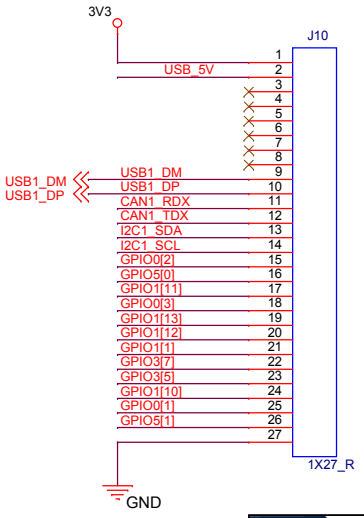
CAN1 IS MULTIPLEXED WITH ETHERNET

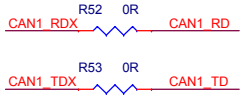
BLINKY LED











NOTE:

* CAN1 cannot be used when Ethernet is enabled.
* Load R52 and R53 to use CAN1
* ADC lines 5V tolerant

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Title: 06 JTAG,BOOT SW,BLINKY LED,HEADER		
Size: B	Document Number: XPLORER	Rev: 1.2
Date: Monday, March 26, 2012	Sheet 6 of 6	