ECE – 448 Lab Section – 201

Lab Assignment 1

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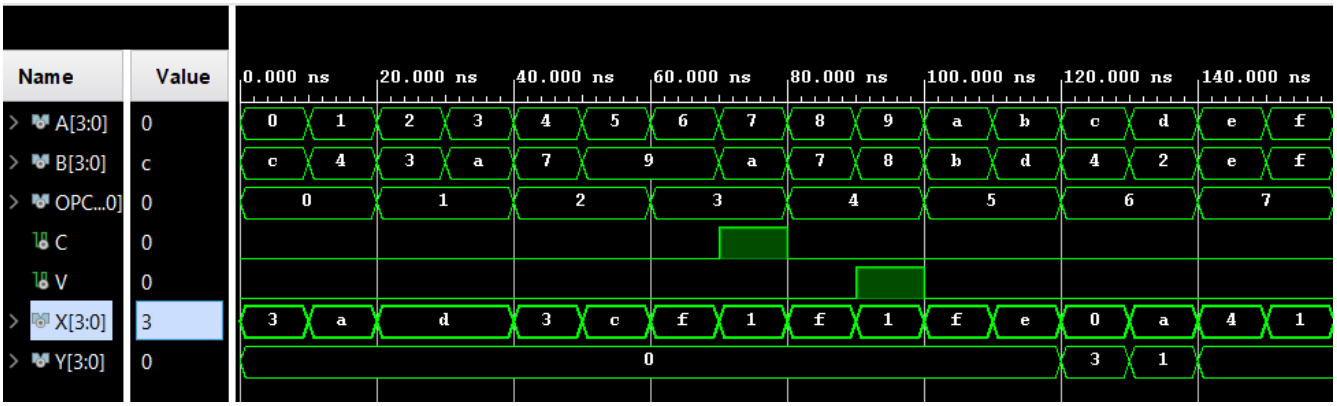
Part 1:

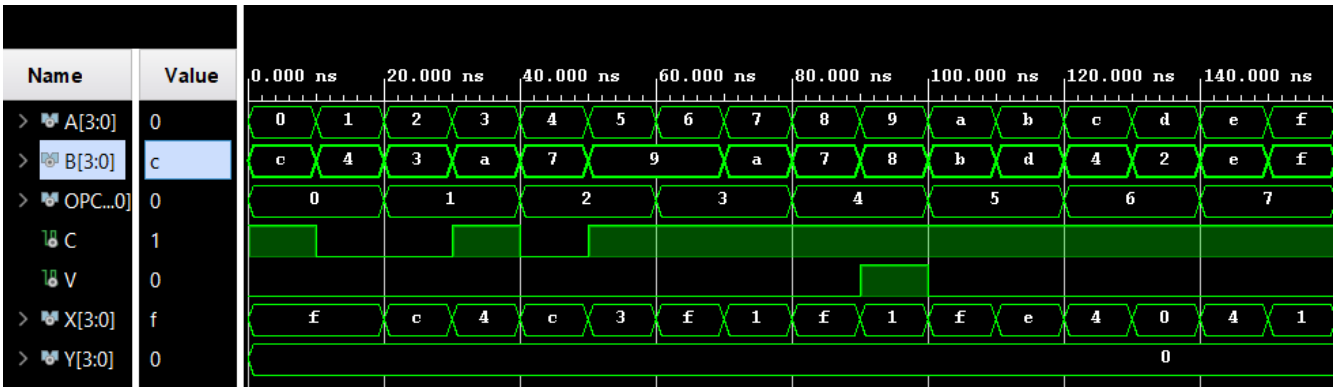
Table of Expected Values

Opcode	Operation	Formula	A	B	X	Y	C	V
000	NOR	X = A NOR B	0	C	3	0	0	0
000	NOR	X = A NOR B	1	4	A	0	0	0
001	NAND	X = A NAND B	2	3	D	0	0	0
001	NAND	X = A NAND B	3	A	D	0	0	0
010	XOR	X = A XOR B	4	7	3	0	0	0
010	XOR	X = A XOR B	5	9	C	0	0	0
011	Uaddition	(C:X) = A + B	6	9	F	0	0	0
011	Uaddition	(C:X) = A + B	7	A	1	0	1	0
100	Saddition	X = A + B	8	7	F	0	0	0
100	Saddition	X = A + B	9	8	1	0	0	1
101	Ssubtraction	X = A – B	A	B	F	0	0	0
101	Ssubtraction	X = A – B	B	D	E	0	0	0
110	Umultiply	(Y:X) = A * B	C	4	0	3	0	0
110	Umultiply	(Y:X) = A * B	D	2	A	1	0	0
111	Smultiply	(Y:X) = A * B	E	E	4	C	0	0
111	Smultiply	(Y:X) = A * B	F	F	1	0	0	0

ALU_psm_1: correct



ALU_psm_2: incorrect



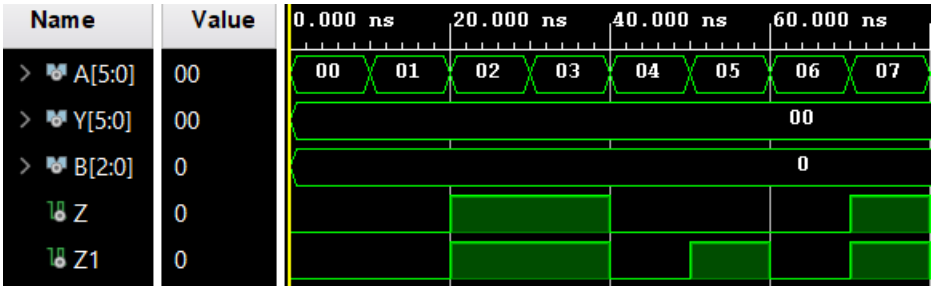
For entries A = 0 and B = C, the carryout is incorrect it should be 0 and the output X is incorrect it should be 3. For entries A = 1 and B = 4, the output X is incorrect it should be A. For entries A = 2 and B = 3, the output X is incorrect it should be D. For entries A = 3 and B = A, the carryout is incorrect it should be 0 and the output X is incorrect it should be D.

```
testing1: PROCESS
Begin
    wait for 10ns;
    A <= std_logic_vector(unsigned(A) + 1);
end PROCESS;

opcode1: PROCESS
Begin
    wait for 20ns;
    OPCODE <= std_logic_vector(unsigned(OPCODE) + 1);
end PROCESS;

testing2: PROCESS
Begin
    B <= x"C";
    wait for 10ns;
    B <= x"4";
    wait for 10ns;
    B <= x"3";
    wait for 10ns;
    B <= x"A";
    wait for 10ns;
    B <= x"7";
    wait for 10ns;
    B <= x"9";
    wait for 10ns;
    B <= x"9";
    wait for 10ns;
```

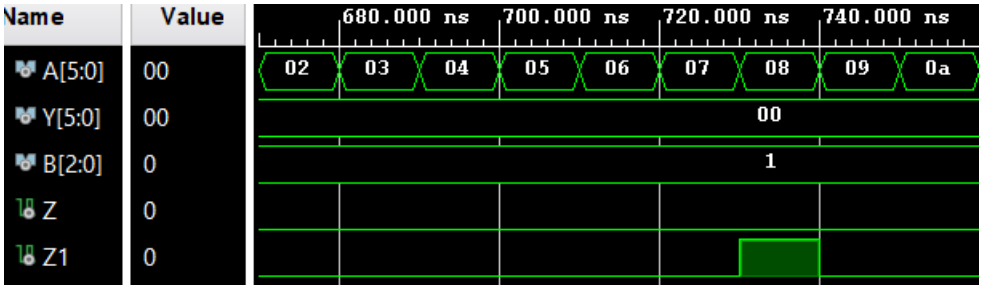
Part 2:

Lab1_psm_1:

Error Z is not equal to Z1, 5 is a prime number



Error Z is not equal to Z1, 8 is divisible by 8



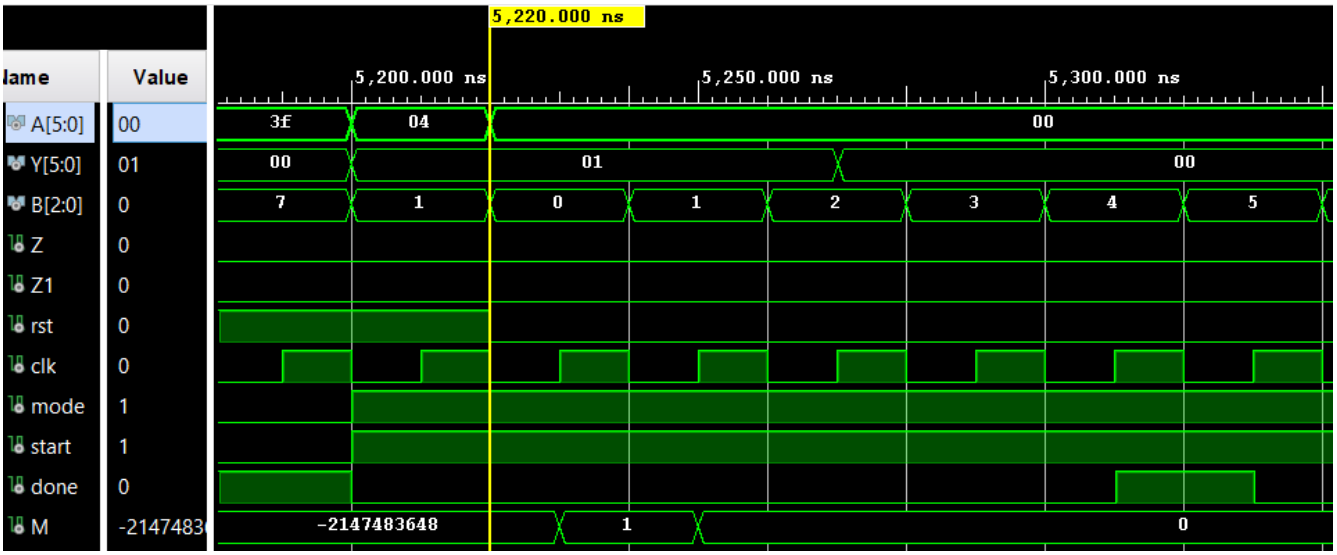
TCL Console output

```
# }
add_wave: Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak = 1322.809 ; gain = 0.000
# run 15500ns
Error: Assertion Failed - Error count: 1
Time: 60 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 2
Time: 740 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 3
Time: 900 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 4
Time: 1060 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 5
Time: 1220 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 6
Time: 1440 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 7
Time: 1700 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 8
Time: 2020 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 9
Time: 2770 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 10
Time: 3480 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 11
Time: 4160 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 12
Time: 4820 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 13
Time: 5230 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 14
```

There were 487 errors found in the first model of lab 1. Most of the errors were in mode 1 but there were errors in mode 0 also however it seems that the bits are being shifted incorrectly in mode 1.

Lab1_psm_2:

Reset does not work Y should be 0, and Y is also incorrect for A = 0 & B = 1 it should be 0




```
# }
# run 15500ns
Error: Assertion Failed - Error count: 1
Time: 5230 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 2
Time: 5270 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 3
Time: 5390 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 4
Time: 5410 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 5
Time: 5430 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 6
Time: 5450 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 7
Time: 5470 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 8
Time: 5490 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 9
Time: 5590 ns  Iteration: 0  Process: /Lab1_tb/testing  File: C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_2_tb.vhd
Error: Assertion Failed - Error count: 10
```

There were 475 errors found in this model, they were all found in mode 1 only. It seems like the bits are being shifted while the core is in mode 1. It seems like both of the models were faulty according to their outputs but the least faulty model was the second core since it performed correctly for mode 0 but not for mode 1, the first core failed both mode 0 and 1.

Lab1_tb.vhd | Untitled 9

C:/Users/Cunker/Documents/Fall 2021/ECE-448/Lab 1/Lab1_tb.vhd

```
    wait for 10ns;
    clk <='1';
    wait for 10ns;
end process;

testing: PROCESS
Begin
    Z1 <= '0';
    Count <= 0;
    A <= "000000";
    B <= "000";
    for j in 0 to 7 loop
        for i in 0 to 64 loop
            if (j = 0 and (i = 2 or i = 3 or i = 5 or i = 7 or i = 11 or i = 13 or i = 17 or i = 19 or i = 23 or i = 29 or i = 31 or i = 37 or i = 41 or i = 43 or i
            elsif (j = 1 and (i = 0 or i = 8 or i = 16 or i = 24 or i = 32 or i = 40 or i = 48 or i = 56)) then Z1 <= '1';
            elsif (j = 2 and (i = 0 or i = 13 or i = 26 or i = 39 or i = 52)) then Z1 <= '1';
            elsif (j = 3 and (i = 0 or i = 1 or i = 3 or i = 6 or i = 10 or i = 15 or i = 21 or i = 28 or i = 36 or i = 45 or i = 55)) then Z1 <= '1';
            elsif (j = 4 and (i = 0 or i = 1 or i = 4 or i = 9 or i = 16 or i = 25 or i = 36 or i = 49)) then Z1 <= '1';
            elsif (j = 5 and (i = 1 or i = 5 or i = 12 or i = 22 or i = 35 or i = 51)) then Z1 <= '1';
            elsif (j = 6 and (i = 1 or i = 6 or i = 15 or i = 28 or i = 45)) then Z1 <= '1';
            elsif (j = 7 and (i = 1 or i = 7 or i = 18 or i = 34 or i = 55)) then Z1 <= '1';
            else Z1 <= '0';
            end if;
            if (TO_INTEGER(unsigned(Z)) /= TO_INTEGER(unsigned(Z1))) then Count <= Count + 1; end if;
            assert TO_INTEGER(unsigned(Z)) = TO_INTEGER(unsigned(Z1))
            report "Assertion Failed - Error count: " & integer'image(Count + 1);
            wait for 10ns;
            if (i /= 63) then A <= std_logic_vector(unsigned(A) + 1); end if;
```