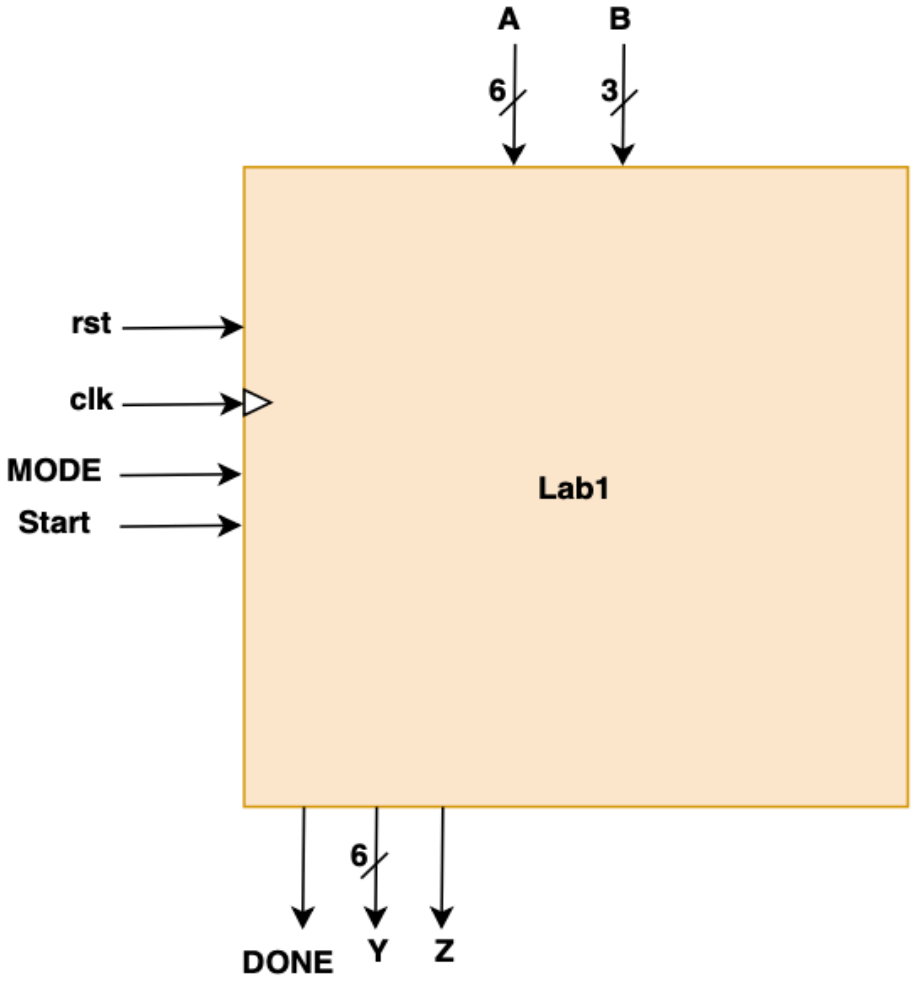
Specification for Lab Assignment Part 2:

Interface



For MODE=0 : Combinational Mode

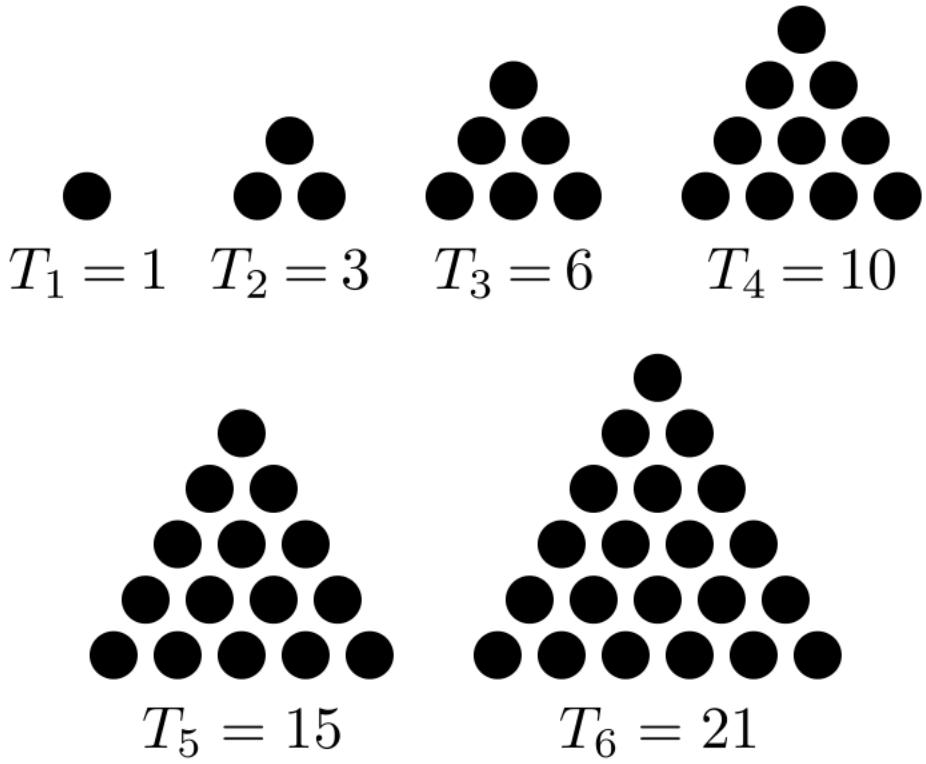
A	B (OP)	Operation described using words
Prime	000	Z = 1 if A is Prime
Divisible by 8	001	Z = 1 if A is divisible by 8
Divisible by 13	010	Z = 1 if A is divisible by 13
Triangular Number	011	Z = 1 if A is a Triangular Number
Square Number	100	Z = 1 if A is a Square Number
Pentagonal Number	101	Z = 1 if A is a Pentagonal Number
Hexagonal Number	110	Z = 1 if A is a Hexagonal Number
Heptagonal Number	111	Z = 1 if A is a Heptagonal Number

Additionally, Y=0 and DONE = 1

Triangular Numbers

List: 0, 1, 3, 6, 10, 15, 21, 28, 36, 45, 55, 66, 78, 91, …

0 is included!



Link: Triangular Numbers

Square Numbers

Note: 0 is included!

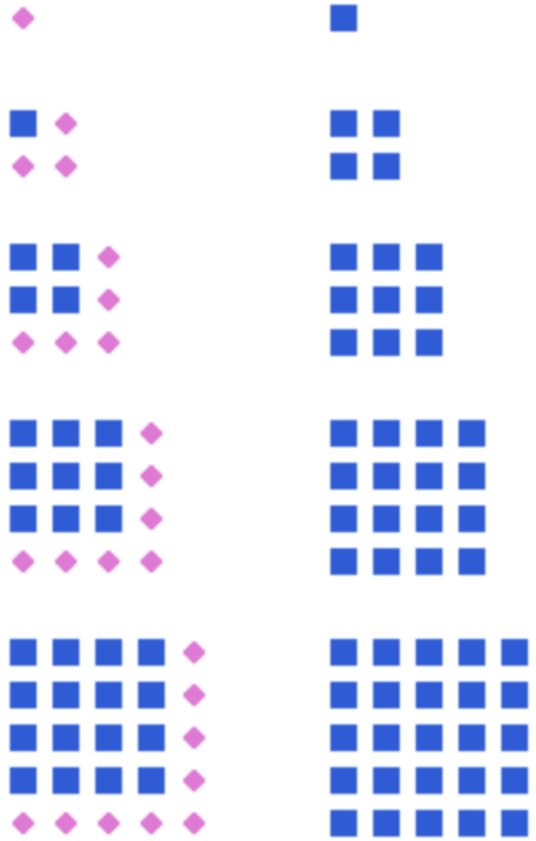
$m = 1^2 = 1$

$m = 2^2 = 4$

$m = 3^2 = 9$

$m = 4^2 = 16$

$m = 5^2 = 25$

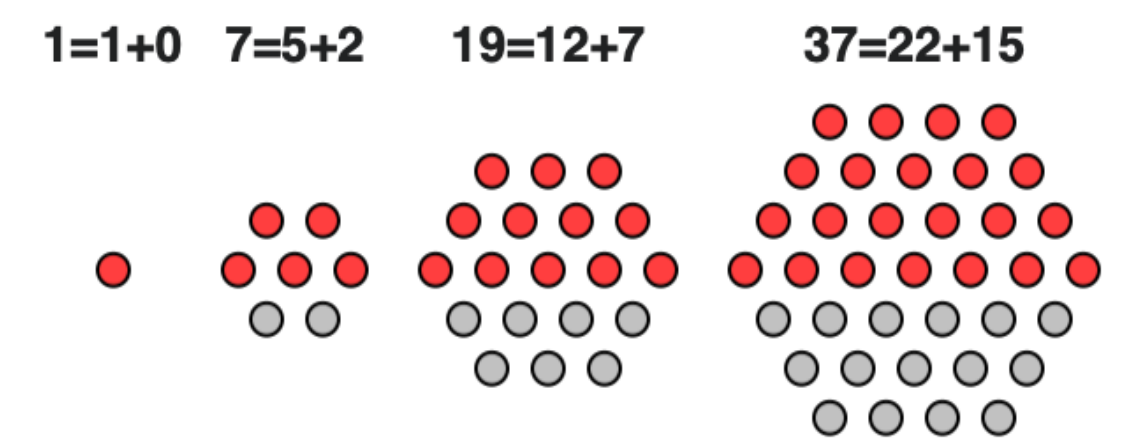


Link: Square Numbers

Pentagonal Numbers

List: 1, 5, 12, 22, 35, 51, 70, 92, 117, 145, 176, 210, 247, …

0 is not included!

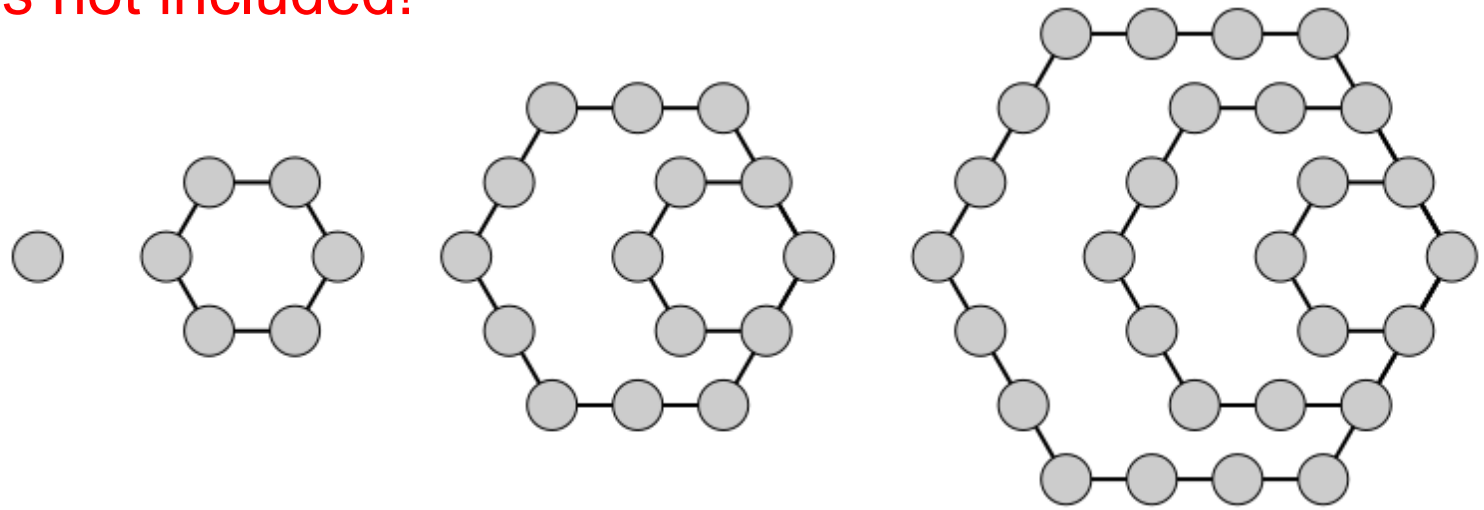


Demo: Pentagonal Numbers

Hexagonal Numbers

List: 1, 6, 15, 28, 45, 66, 91, 120, 153, 190, 231, …

0 is not included!

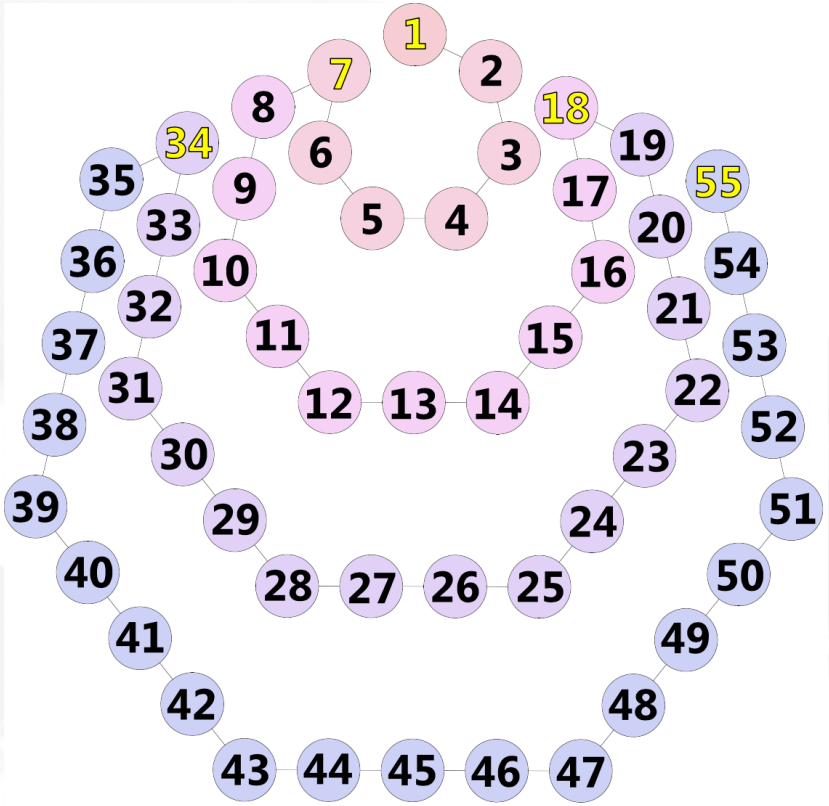


Link: Hexagonal Numbers

Heptagonal Numbers

List: 1, 7, 18, 34, 55, 81, 112, 148, 189, 235, …

0 is not included!



Link: Heptagonal Numbers

For MODE=1 : Sequential Mode

$$Y = A^B \bmod 64$$

Start : inputs ready; start of the sequential operation
DONE: result available at the output Y

Additionally, Z=0

Assume that $0^0 = 1$
Link: Zero to the power of zero

Table of Input/Output Ports (1)

Name	Mode	Width	Meaning
rst	INPUT	1	Asynchronous reset
clk	INPUT	1	Clock
MODE	INPUT	1	Circuit mode: 0 – Combinational 1 – Sequential
Start	INPUT	1	Start of the sequential operation in MODE 1
A	INPUT	6	For Mode 0: Input to the combinational operation defined by B For Mode 1: Input A to the sequential operation $Y=A^B \bmod 64$
B	INPUT	3	For Mode 0: Operation to be performed on A, as defined in the table below For Mode 1: Input B to the sequential operation $Y=A^B \bmod 64$

Table of Input/Output Ports (2)

Y	OUTPUT	6	Output of the sequential operation $Y=A^B \bmod 64$
Z	OUTPUT	1	Output of the combinational operation
DONE	OUTPUT	1	Indicator that the output Z is valid in MODE 0 and the output Y is valid in MODE 1.

Discrepencies

One of the provided models is correct.
The second model contains multiple discrepancies compared to the specification.

These discrepancies may have, for example, the following forms:

1. Incorrect output Z for a subset of allowed values of A and B in the combinational
2. Incorrect output Y for a subset of allowed values of A and B in the sequential mode.

Testbench Requirements

Your testbench should automatically compare actual outputs with expected outputs for:

1. MODE=0 and MODE=1
2. All values of the inputs A and B.

Your testbench should also report when a discrepancy is found and count a total number of errors.

Tasks

Tasks:

1. Write a testbench capable of verifying Lab1 core, using all combinations of inputs A and B
2. Write a short report describing all discrepancies between the above specification and the faulty model.

Deliverables

Deliverables:

1. VHDL code of the testbench.
2. Parts of the waveforms obtained by running your testbench in the Vivado Simulator (in the PDF format) demonstrating discrepancies between actual outputs and expected outputs.
3. All messages written by the testbench to the standard output.
4. Report describing all discrepancies you have managed to detect. For MODE=1, try to determine what is a common feature of all inputs giving incorrect outputs.