

Lab 1: Arithmetic and Logic Unit

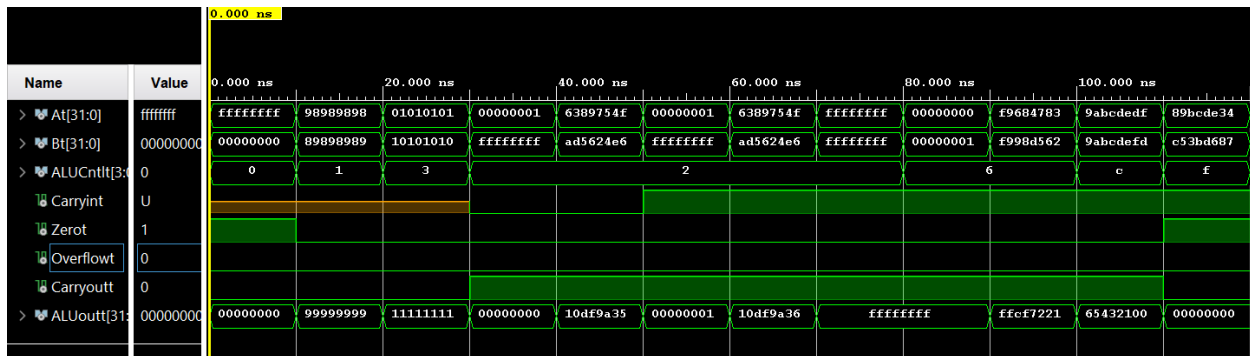
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Introduction: The purpose of this lab is to implement an ALU design using VHDL. This design will be able to perform and, or, xor, add, subtract, and nor. A test bench will be made to test these operations as well as test the various flags for zero, overflow, and carryout.

Problem Logic & Solution: I used a series of with select when statements to implement each of the operations of the ALU. I used a temp signal that is one bit larger so I can easily determine the carryout. I used with select when statements for the zero and overflow flags.



Conclusion: I was able to confirm most of my results and confirmed flags such as carryout and zero. I was surprised that the overflow was not triggered but I could not get an overflow when calculating manually so I assume my results are accurate.

Comments: Could I get a reminder on how to calculate for overflow because I'm not sure if my method was correct and I was slightly lost on overflow for subtraction, I had to refer to 331 notes but there's very little on overflow.