

Projects

Exercise 1.

The goal of this project is to design and synthesize different types of FFT architectures for different FFT sizes. One project will be assigned to you.

■ Objectives

- Test bench design: design test input as a mixture of sinusoids and find FFT using MATLAB/Python command. Then convert input and output to hexadecimal notations.
- Verilog code, verify functionality
- Synthesizable Verilog code, power-area-timing report,
- Vary pipelining levels, write report and prepare presentation.
- Project Presentations (30 minutes)
- Final Report (fully typed) (PDF preferred), presentations and Verilog codes.

■ Projects

- Frequency: 500MHz
 - Optimization: Without and with CSD
1. 8-parallel FFT - 64-points - Radix 2.
 2. 4-parallel FFT - 128-points - Radix 2.
 3. 8-parallel FFT - 64-points - Radix 2^3 .
 4. 4-parallel FFT - 128-points - Radix 2^3 .
 5. 2-parallel FFT - 16-points - Bit Serial Arithmetic Architectures - Radix 2.

■ Deadline: 30/05/2019