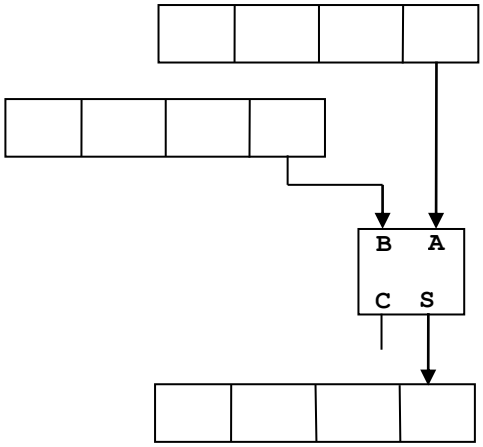
Use of Logic Circuits in the Arithmetic Logic Unit

One of the jobs that the ALU carries out is to add two binary numbers together. We will start by looking at a single bit adder, also known as a HALF ADDER.



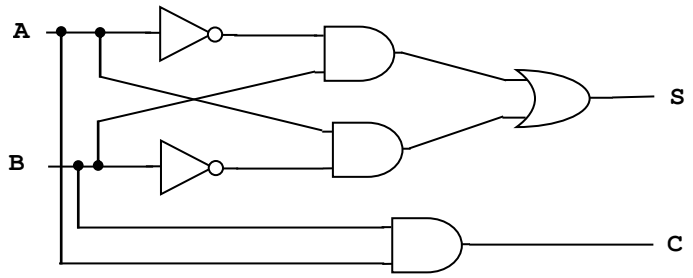
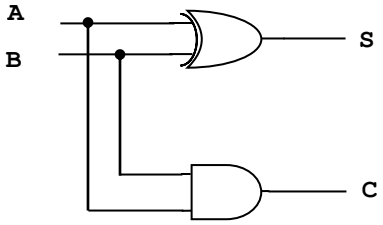
The truth table for the half adder will look like this:

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

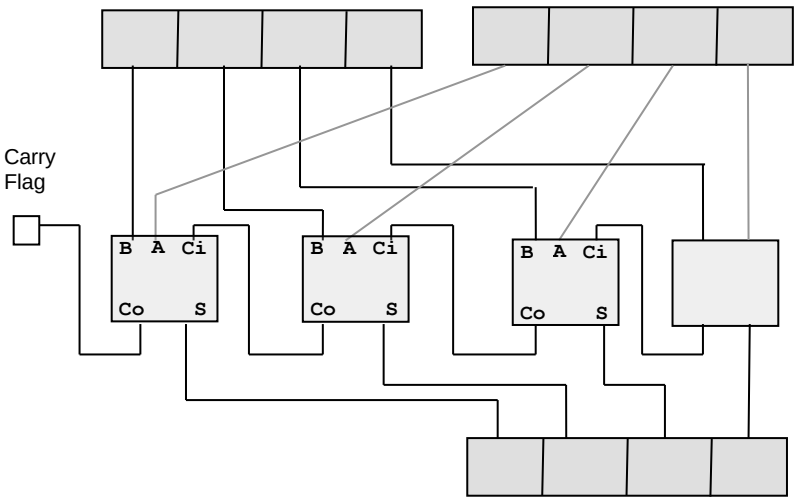
Note that there are two outputs from the half adder.

S = /A.B + A./B = A ⊕ B

C = A.B

The circuit using only AND, OR and NOT gates.	The circuit using an XOR gate.
	

That would be ok for the first bit in each register, but all of the other addition units bits need to take the carry from the previous column into account. This device is known as a FULL ADDER



So for each full adder we could design a truth table as follows:

A	B	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The full sum of products expressions for S and Cout. (Also known as CANONICAL expressions).

$$S = \overline{A}.\overline{B}.Ci + \overline{A}.B.\overline{Ci} + A.\overline{B}.\overline{Ci} + A.B.Ci$$

$$Co = \overline{A}.B.Ci + A.\overline{B}.Ci + A.B.\overline{Ci} + A.B.Ci$$

Simplifying the expression for S:

$$S = \overline{A}.(\overline{B}.Ci + B.\overline{Ci}) + A.(\overline{B}.\overline{Ci} + B.Ci)$$

Remembering that:

$$\overline{X}.Y + X.\overline{Y} = X \oplus Y$$

$$\overline{X}.\overline{Y} + X.Y = \overline{X \oplus Y}$$

$$S = \overline{A}.(B \oplus Ci) + A.\overline{(B \oplus Ci)}$$

Generalising the first equivalence above, to make it easier to spot the pattern:

$$\overline{Red}.Blue + Red.\overline{Blue} = Red \oplus Blue$$

$$S = A \oplus B \oplus Ci$$

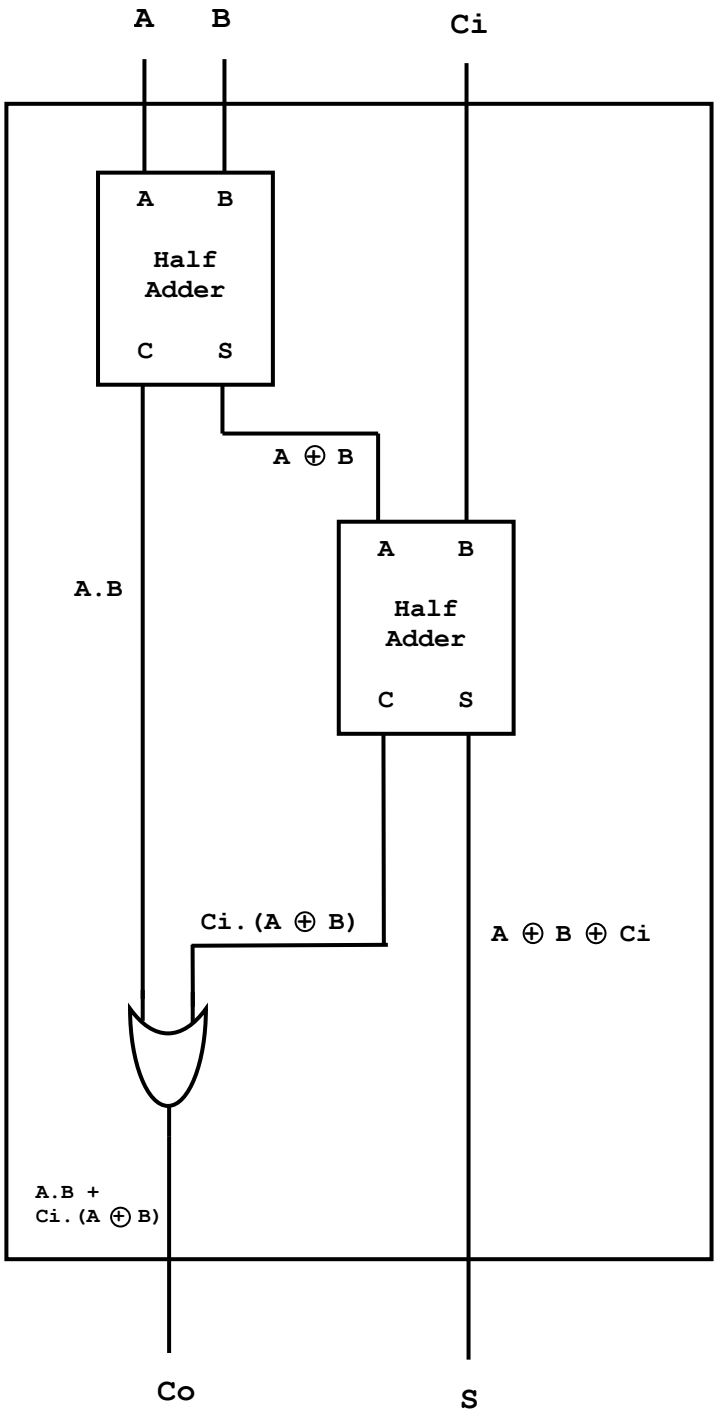
Simplifying the expression for Co

$$Co = \overline{A}.B.Ci + A.\overline{B}.Ci + A.B.\overline{Ci} + A.B.Ci$$

$$Co = Ci.(\overline{A}.B + A.\overline{B}) + A.B.(\overline{Ci} + Ci)$$

$$Co = Ci.(A \oplus B) + A.B$$

A Full Adder could be built as follows:



As shown on the diagram on the first page, these Full Adders are connected together and are used to add together the contents of two registers, the result being output into a third register.

I have ignored the issue of timing. The bits would not be added simultaneously, as it would take time for the carry to propagate along the row of adders. The timing pulses from the clock would be used to control that process.