Fibonacci sequence Circuit

PC/CP220 Project Phase III

Kevin Yejoon Lee
210872060
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Logic Equation

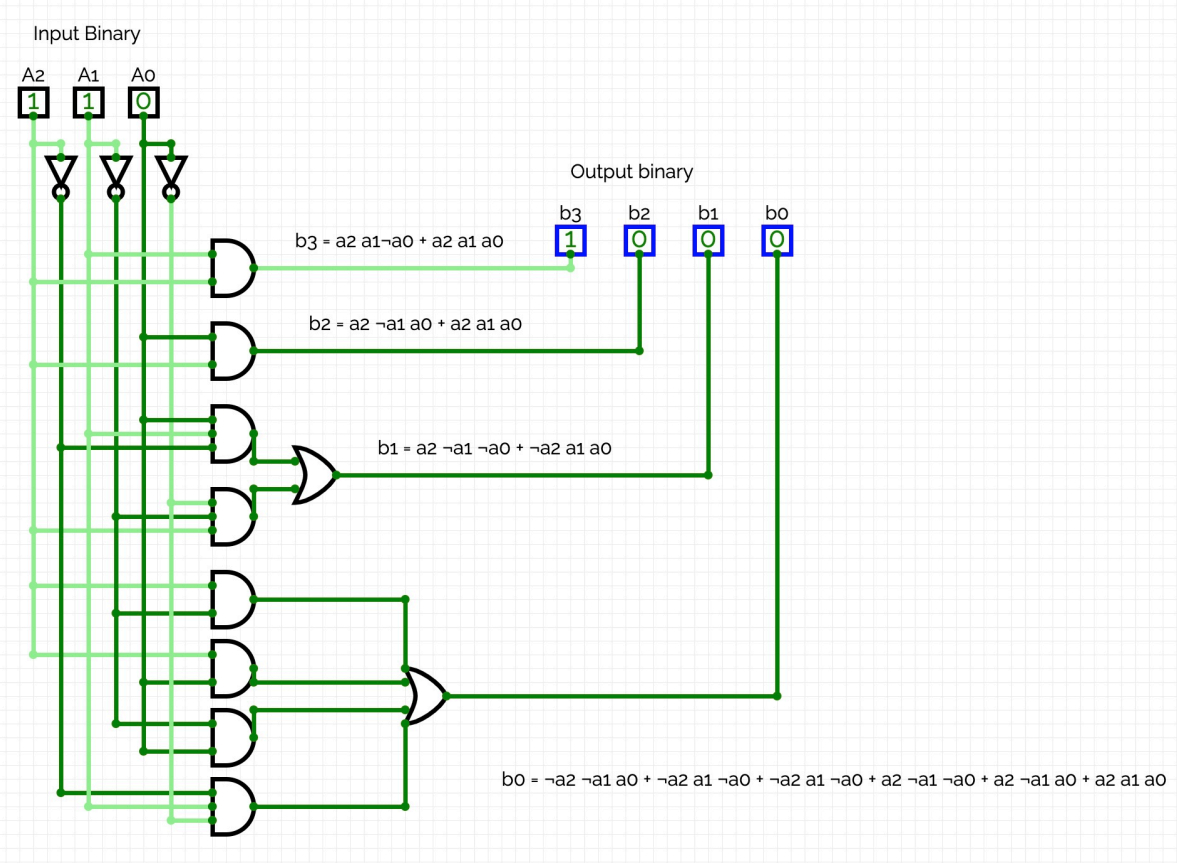
The equations for the outputs

$B_3 = a2\ a1\ \neg a0 + a2\ a1\ a0$
$B_2 = a2\ \neg a1\ a0 + a2\ a1\ a0$
$B_1 = a2\ \neg a1\ \neg a0 + \neg a2\ a1\ a0$
$B_0 = \neg a2\ \neg a1\ a0 + \neg a2\ a1\ \neg a0 + a2\ \neg a1\ \neg a0 + a2\ \neg a1\ a0\ + a2\ a1\ a0$

Circuit Diagram

Diagram of fibonacci converter

The circuit was drawn using https://circuitverse.org/ as shown in the following figure. Unlike other circuits, the output returns a binary number that represents the output fibonacci number rather than a boolean value like the prime identifier circuit. The circuit serves its purpose in finding the corresponding fibonacci number as proven in sections later on.



Circuit Outputs TT

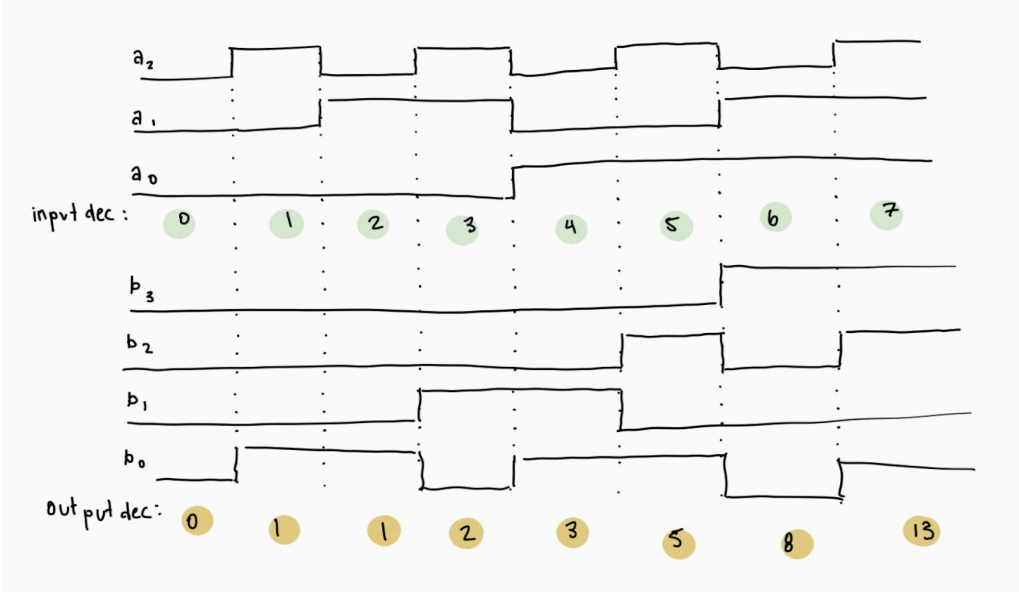
All the circuit outputs = the expected fibonacci number

a_2	a_1	a_0	b_3	b_2	b_1	b_0
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	0	1	1
1	0	1	0	1	0	1
1	1	0	1	0	0	0
1	1	1	1	1	0	1

Therefore, the circuit serves its purpose in finding the corresponding fibonacci number.

Simulation Output

All the circuit outputs = the expected fibonacci number



Parts List

List of all parts required to make circuit

In addition to the CPLD (Complex Programing Logic Device) we require,

- • DIP switch, for input
- • Resistor array for the DIP switch; probably 1kΩ or so.
- • four LED (could use debugger board but LED's could demonstrate one bit each as well)
- • Resistor for the LED's; probably 510Ω or so each. (unless using debugger board)

Extra Proof for Circuit

There is a video with attached circuit demonstrating the working circuit outputs

END OF PROJECT PHASE 3

Check list attached below

PC/CP220 Project Phase III Checklist (3.01)

A. General

1. Professionally presented
   Neat, etc. _____

2. Properly identified
   (eg. name, id) _____

3. On time
   at *beginning* of lab *with checklist* _____

4. Good grammar
   (eg. complete sentences where required) _____

5. Correct spelling
   _____

B. Content

1. *Circuit diagram is*
   consistent with equations _____

2. *All cases are simulated*
   with good explanations _____

3. *Circuit passes/fails simulation*
   noted (matches truth table) _____

4. *All input/output parts have been*
   listed (including resistors) _____

5. *<u>All</u> previous phases included*
   (updated if necessary) _____

Fibonacci sequence Circuit

PC/CP220 Project Phase II

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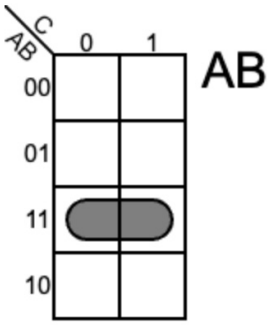
Table of Contents

TT containing only binary quantities

Each bit to be broken down into a k-map

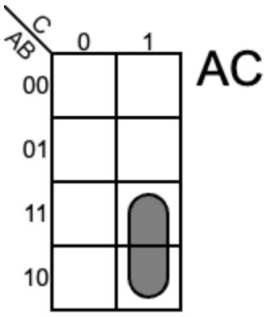
a_2	a_1	a_0	b_3	b_2	b_1	b_0
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	0	1	1
1	0	1	0	1	0	1
1	1	0	1	0	0	0
1	1	1	1	1	0	1

b_3



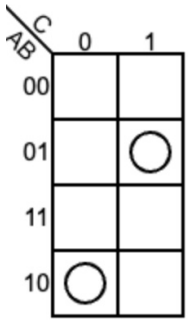
$AB\overline{C}+ABC$

b_2



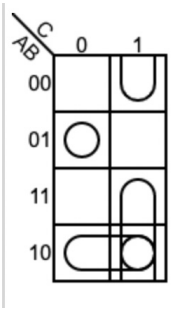
$A\overline{B}C+ABC$

b_1



$A\overline{B}\,\overline{C}+\overline{A}BC$

b_0



$$A\overline{B}+AC+\overline{B}C+\overline{A}B\overline{C}$$

SOP Formulas

Solutions to SOP

Outputs	Solution	SOP
b_3	AB	$AB\overline{C}+ABC$
b_2	AC	$A\overline{B}C+ABC$
b_1	$A\overline{B}\,\overline{C}+\overline{A}BC$	$A\overline{B}\,\overline{C}+\overline{A}BC$
b_0	$A\overline{B}+AC+\overline{B}C+\overline{A}B\overline{C}$	$\overline{A}\,\overline{B}C+\overline{A}B\overline{C}+A\overline{B}\,\overline{C}+A\overline{B}C+ABC$

Equation Testing

Each output tested in maxima

b_3	%i1)
	f:(a and b and not c) or (a and b and c);
	(%o1) a∧b∧¬c∨a∧b∧c
	
	(%i2)
	f, a=true, b=true ,c=true;
	(%o2) true
	
	(%i3)
	f, a=true, b=true ,c=false;
	(%o3) true
	
	(%i4)
	f, a=true, b=false ,c=true;
	(%o4) false
	
	(%i5)
	f, a=true, b=false ,c=false;

	(%o5) false
	
	(%i6)
	f, a=false, b=true ,c=true;
	(%o6) false
	
	(%i7)
	f, a=false, b=true ,c=false;
	(%o7) false
	
	(%i8)
	f, a=false, b=false ,c=true;
	(%o8) false
	
	(%i9)
	f, a=false, b=false ,c=false;
	(%o9) false

b_2	(%i1)
	f:(a and not b and c) or (a and b and c);
	(%o1) a∧¬b∧c∨a∧b∧c
	
	(%i2)
	f, a=true, b=true ,c=true;
	(%o2) true
	
	(%i3)
	f, a=true, b=true ,c=false;
	(%o3) false
	
	(%i4)
	f, a=true, b=false ,c=true;
	(%o4) true
	
	(%i5)
	f, a=true, b=false ,c=false;
	(%o5) false
	
	(%i6)
	f, a=false, b=true ,c=true;
	(%o6) false
	
	(%i7)
	f, a=false, b=true ,c=false;
	(%o7) false
	
	(%i8)
	f, a=false, b=false ,c=true;
	(%o8) false
	
	(%i9)
	f, a=false, b=false ,c=false;
	(%o9) false

b_1	(%i1)
	f:(a and not b and not c) or (not a and b and c);
	(%o1) a∧¬b∧¬c∨¬a∧b∧c
	
	(%i2)
	f, a=true, b=true ,c=true;
	(%o2) false
	
	(%i3)
	f, a=true, b=true ,c=false;
	(%o3) false
	
	(%i4)
	f, a=true, b=false ,c=true;
	(%o4) false
	
	(%i5)
	f, a=true, b=false ,c=false;
	(%o5) true
	
	(%i6)
	f, a=false, b=true ,c=true;
	(%o6) true
	
	(%i7)
	f, a=false, b=true ,c=false;
	(%o7) false
	
	(%i8)
	f, a=false, b=false ,c=true;
	(%o8) false
	
	(%i9)
	f, a=false, b=false ,c=false;
	(%o9) false

b_0	(%i1) f:(not a and not b and c) or (not a and b and not c) or (a and not b and not c) or (a and not b and c) or (a and b and c); (%o1) ¬a∧¬b∧c∨¬a∧b∧¬c∨a∧¬b∧¬c∨a∧¬b∧c∨a∧b∧c (%i2)

Summary

The equations for the outputs are

$B_3 = a2\ a1\ \neg a0 + a2\ a1\ a0$
$B_2 = a2\ \neg a1\ a0 + a2\ a1\ a0$
$B_1 = a2\ \neg a1\ \neg a0 + \neg a2\ a1\ a0$
$B_0 = \neg a2\ \neg a1\ a0 + \neg a2\ a1\ \neg a0 + a2\ \neg a1\ \neg a0 + a2\ \neg a1\ a0 + a2\ a1\ a0$

f, a=true, b=true ,c=true;
(%o2) true

(%i3)

f, a=true, b=true ,c=false;
(%o3) false

(%i4)

f, a=true, b=false ,c=true;
(%o4) true

(%i5)

f, a=true, b=false ,c=false;
(%o5) true

(%i6)

f, a=false, b=true ,c=true;
(%o6) false

(%i7)

f, a=false, b=true ,c=false;
(%o7) true

(%i8)

f, a=false, b=false ,c=true;
(%o8) true

(%i9)

f, a=false, b=false ,c=false;
(%o9) false

PC/CP220 Project Phase II Checklist (3.01)

A. General

1. Professionally presented
   Neat, etc. _____

2. Properly identified
   (eg. name, id) _____

3. On time
   at *beginning* of lab *with checklist* _____

4. Good grammar
   (eg. complete sentences where required) _____

5. Correct spelling
   _____

B. Content

1. *All outputs analyzed*
   (truth table) _____

2. *Karnaugh maps (or equations)*
   match truth table _____

3. *Equations tested*
   (Maple, Maxima, etc.) _____

4. *Summary statement*
   (all equations pass all tests) _____

5. *Previous phase included*
   (updated if necessary) _____

Fibonacci sequence Circuit

PC/CP220 Project Phase I

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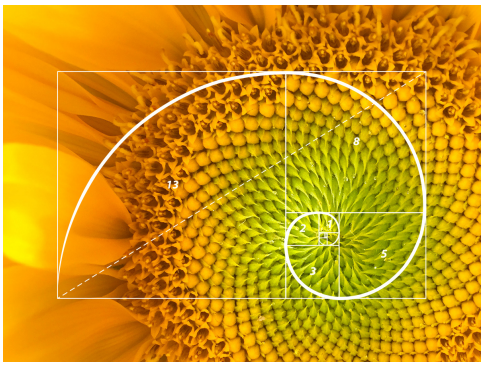
Description

They are specific numbers that we see in nature all the time, sometimes called *nature's code*. Together they are called the Fibonacci sequence.



The idea is simple: the next number is equal to the last two numbers in the sequence. If you look in nature these numbers appear everywhere. Bananas will contain three seed sections, apples five, in fact, chances are that no matter the plant you are looking at it will have 3,5,8,13 ~ pedals or seeds sections. (pine cones, snail shells, broccoli, pineapples, etc)

In nature these numbers represent the most efficient way to pack as many seeds as possible.

Inputs

The **Fibonacci sequence Circuit** will have 3 inputs, a_0 to a_2 which represent the binary representation of the number to be indexed from the fibonacci sequence. The input representing 1 will represent the first number in the sequence. The maximum decimal number these bits can represent is 7.

Outputs

The **Fibonacci sequence Circuit** will have 4 outputs b_0 to b_3 which represent the binary presentation of the number outputted at that index, the index of 3 will give an output of 2 according to the sequence. The maximum decimal number these bits can represent is 15.

Identical Output case

Table below shows two cases where output is identical

Input Decimal	$a_2\,a_1a_0$	Output	$b_3b_2b_1b_0$
1	001	1	0001
2	010	1	0001

Final Truth Table

Table below gives a summary of the circuit's behavior.

Input Decimal	$a_2\,a_1a_0$	Output	$b_3b_2b_1b_0$
0	000	0	0000
1	001	1	0001
2	010	1	0001
3	011	2	0010
4	100	3	0011
5	101	5	0101
6	110	8	1000
7	111	13	1101

PC/CP220 Project Phase I Checklist (3.01)

A. General

1. Professionally presented
   Neat, etc. _____

2. Properly identified
   (eg. name, id) _____

3. On time
   at *beginning* of lab *with checklist* _____

4. Good grammar
   (eg. complete sentences where required) _____

5. Correct spelling
   _____

B. Content

1. *Sufficient background*
   (ie. problem circuit is to solve) _____

2. *Inputs are specified*
   (eg. A_0,A_1,A_2,A_3 - binary) _____

3. *Outputs are specified*
   (eg. L_1,S_1,L_2,S_2, etc. - dashes/dots) _____

4. *Error conditions and responses*
   to them are specified
   (or stated that none exist) _____

5. *Ambiguous possibilities have been*
   eliminated (ie. don't care conditions)
   (or stated that none exist) _____