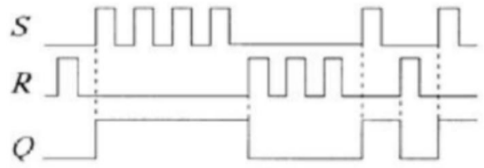
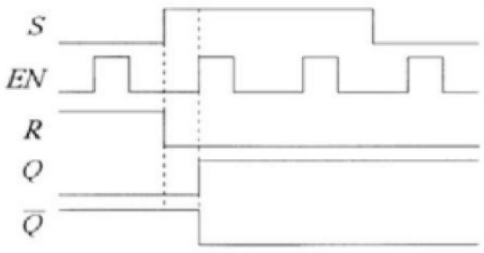
2.

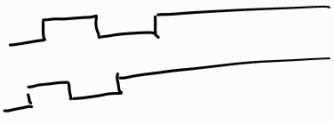


4.



8) Q(a)

Q(b)



a) the flip-flop triggers on the negative edge of the clock pulse

b) the flip-flop triggers on the positive edge of the clock pulse

20)

1. t_{PLH} (clock to Q)

- time from triggering edge of clock to LOW-to-HIGH transition of the Q output.

2. t_{PHL} (clock to Q)

- time from triggering edge of clock to the HIGH-to-LOW transition of the Q output

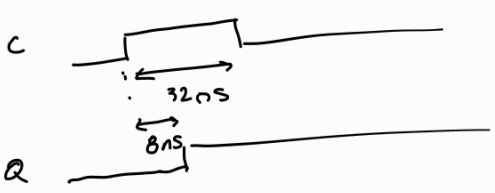
3. t_{PLH} ($\overline{PRE}$ to Q)

- time from triggering edge of clock to the HIGH-to LOW transition of the Q output

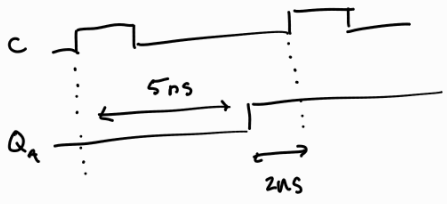
4. t_{PHL} ($\overline{CLR}$ to Q)

- time from assertion of the preset input to the LOW-to-HIGH transition of the Q output

22)



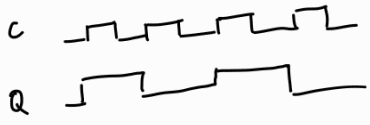
24)



$T_{min} = 5ns + 2ns = 7ns$

$f_{MAX} = \frac{1}{T_{min}} = \frac{1}{7ns} = 142.9 MHz$

25)



divide by 2

26)